# First lessons from Feb'2013 TB 

Vladislav Balagura

LLR/CNRS

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## Outline

## (1) TB'Feb13 Setup

(2) Noise level
(3) Retriggerings in $B X+n$

4 Conclusions

## Topic

## (2) Noise level

## (3) Retriggerings in $B X+n$

4 Conclusions

## Setup

First time:

- >1 LDAs (not possible in past)
- new DAQ software
- power pulsing mode in 6 out of 10 slabs
- new firmware



## Setup (cont.)

Debugging during two first TB days. Finally: 7-8 slabs out of 10 (interconnection problem, corrupted data), 2 LDAs out of 3 (one disturbed network by sending corrupted TCP/IP packets). Difficulties in starting DAQ, more debugging tools are needed.

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## Noise

Appears in two places:

- trigger thresholds (not so visible)
- energy measurement error $\leftarrow$ width of pedestal spectrum Usually better, and more attention in the past. To be studied for TB'Feb13, sign of higher level with power pulsing.


## Automatic masking of noisy channels

By default, the range of individual adjustment of trigger thresholds (per channel) is too narrow. A nontrivial modification was done in slab 9 to fix that, but due to absence of software, we did not try this possibility. Only the global trigger threshold (per chip) was adjusted. Two approaches:

- Reconstruct S-curve in full trigger threshold scan.

Unfortunately: plenty of plane events/retriggerings in successive BX at lower thresholds, S-curves are biased unless scan is done per channel (which is impossible, too much time). Thresholds are determined semi-manually

- Automatic masking: start from higher thresholds and go down, at every step mask appearing noisy channels.
Thanks to new DAQ software. After some trials run 20 sec and then mask all channels triggered $\geq 3$ times. Allow maximum two attempts at every threshold, then go down. Exclude all events with a) retriggerings in $B X+1, B X+2, \ldots$ (successive bunch crossings); b) with $\geq 32$ hits (sometimes up to 64 channels are fired at once).


## Noise: invariant patterns and fluctuations

Always noisy (masked): 32 noisy channels across all slabs (12.5\%). All with multiple connections except chip0: 47, 52,53 , chip1: $35,37,38,44$, chip2: 21 (3.1\%) (partially understood).


At lower level: noise in other channels, may change in $\leq 30$ minutes, $\sim 3 \%$ masked.

## Results (lower gain, 1.2 pF )

Several automatic threshold scans at different gains (with feedback $\mathrm{C}=1.2,2,3.2,4,6 \mathrm{pF}$ )


## Results at the highest gain ( 6 pF )

At lower gain (relative) thresholds are lower.


## MIP calibration (lower gain, C=1.2 pF)

Beam centered at chip 2. Thresholds in the best (last) DIF are reduced on purpose to see pedestal.

MIP calibration, sum of channels in chip 2, retrig. removed


## MIP calibration (the highest gain, $\mathrm{C}=6 \mathrm{pF}$ )

MIP calibration, sum of channels in chip 2, retrig. removed


## Beam spot (lower gain, C=1.2 pF)

Normalized accumulated sum of pedestal subtracted ADC


Only 5000 records per chip, slab (online), noisy channels at 1.2, retrig. removed

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## MIPs (lower gain, C=1.2 pF)

Number of successive bunch crossings (with difference $\Delta B X \leq 3$ ).


Thresholds rised manually in DIF 1,5,6

## Showers (only the highest gain)

1 GeV and 5 GeV showers


## Transverse shower profile

Order of layers: $6,1,2,5,3,8,7$ (interleaved with 4.2 mm W layers)


Only 5000 records per chip, slab (online), noisy channels at 1.2, retrig. removed

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## Conclusions

- Successful test of Si-W ECAL technological prototype in DESY in Feb'13
- new DAQ software
- 2 LDAs (not possible in the past)
- power pulsing mode in 6 out of 10 slabs
- new DIF firmware
- Observed problems
- DAQ instabilities (7-8 out of 10 slabs, 2 out of 3 LDAs, a few resets needed, lack of debugging tools)
- Noise level (esp. in trigger)
- Retriggerings in $B X+1, B X+2, \ldots$
- Next TB in DESY in July'13

