## SiECAL Technological Prototype TB Feb 2013

CALICE Collaboration Meeting @ Hamburg 22 March 2013 Yuji Sudo (Kyushu University) On behalf of SiWECAL Group.

## SiECAL Test Beam @

Test Beam for The SiECAL technological prototype at beam line 21. Main goal = Power Pulsing

DES



## Slabs

Si sensor has 324 pixels

Pixel size =  $5x5 \text{ mm}^2$ 

4 SKIROC2b ASICs in a slab = 256 ch/slab We tested 10 slabs with e<sup>+</sup> beam.

- 4 slabs in Power Pulsing (PP) mode
- 4 slabs in no-PP mode
- 2 slabs have interconnection problem.

four no-PP slabs are same setting as last summer TB. PP slabs are modified for PP mode.

- all PP slabs have no decoupling capacitance for Vref (dif 1,2,3,8)
- bigger decoupling capacitance in power supply lines (dif8)
- pin clipping (dif2)



## Program of the TB

Power pulsing studies comparison full PP/noPP/only PA in PP/LL MIP/showers

Magnetic field

- → Test of pulsed current in B field (see Nathalie's talk) Measurement of interconnection resistance
- → Test of one slab in B field (in PP config) Measurement of pedestal







- Pedestal Study
- MIP calibration
- de-synchronization
- Pedestal Study in magnetic field



#### First Pedestal Result



#### Already seen in previous Test beam but not so clear



ADC count

Badbcid==1 cut  $\rightarrow$  remove BCID+1 event Badbcid==2 cut  $\rightarrow$  remove plane event

Nohit near cut = We cut the events with a hit In a channel geometrically close to the studied channel

- Pedestal Study
- MIP calibration
- de-synchronization
- Pedestal Study in magnetic field

## MIP



1 巨 

IN

5.145

10.63

73 / 36

N

#### strange behaviors

#### DIF1 Ch43(PP)





#### DIF5 CH43(noPP)





#### MPV of MIP in PP/noPP



- Pedestal Study
- MIP calibration
- de-synchronization
- Pedestal Study in magnetic field

### De-synchronization between slabs



### **Detection efficiency**

In MIP reconstruction, we compensate the synchronization problem event by event to take into account the de-synchronization during run.



#### **Event Displays**



1 MIP

The hole just before the last layer is Due to 2 removed slabs



Start of shower

- Pedestal Study
- MIP calibration
- de-synchronization
- Pedestal Study in magnetic field

## Pedestal of Chip1 in 0 ~ 2 T magnetic field

#### **Pedestal Position**

**Pedestal Width** 





# **Other Chips**

800 1000 1200 1400 1600

400 600 800 1000 1200 1400 1600

Current [A]

Current [A]

▼: Masked, Preamp. enable

O: Masked, Preamp. disable

\*: Not masked, Preamp. enable

Chip2



Chip3

0350 00 1340



Chip4



18

Pedestal Position Pedestal Width

[350 00 1340

300

290

280

270

260

250

<sub>b</sub>10

5

3

2

0

0

200

0 200 400 600

Current [A]

0





### Conclusion

For magnetic field

We study pedestal in function of time to check pedestal stability. We plan to test in magnetic field with injected signal.

with beam

Power pulsing measurements seem promising

We have to understand

-- noise behavior, pedestal distribution

-- synchronization

Thanks to our experts: Mickael, Remi And in particular Frederic for the DAQ software ... and all participants to the test beam

### Backup

with beam :

- all PP slabs in PP mode

-- with all channels

-- without W plate

-- with a 2.1 mm W plate

-- with 4.2 mm W plates

-- with 6ch/chip (PP slab)

-- with one or two chip/slab (PP slab)

-- several PA gain settings

- only preamp in PP mode

-- normal mode

-- low leakage current mode

- all modules in no-PP mode

without beam :

- in magnetic field

