AHCAL Electronics.

Status of HBU, EBU and SM_HBU

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CALICE meeting

Annecy, Sept. 10th, 2013

HELMHOLTZ GEMEINSCHAFT

Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

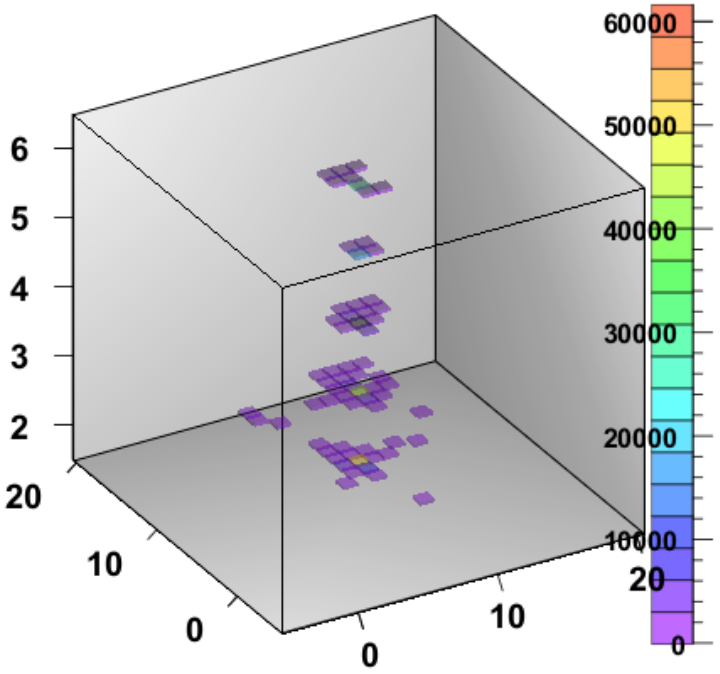
CALICE Calorimeter for ILC

AIDA

DESY

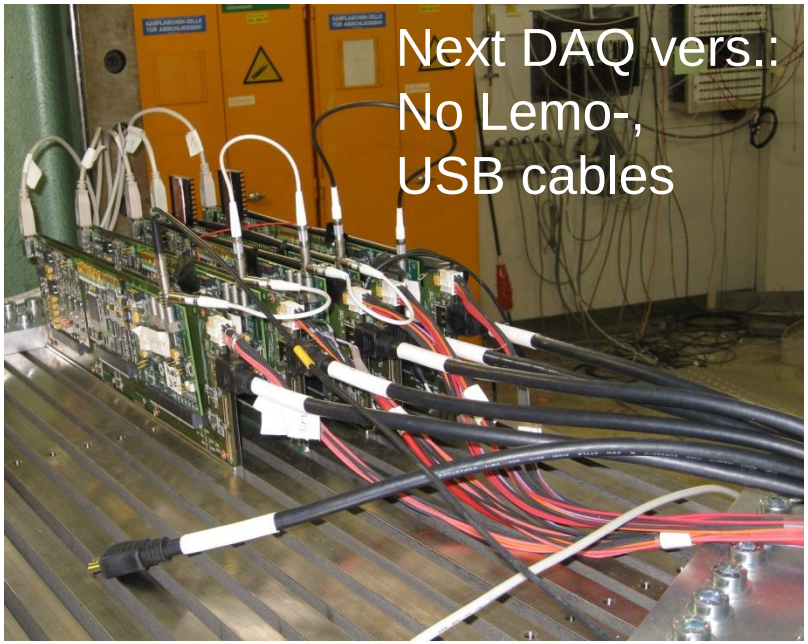
Outline

- AHCAL electronics status and results
  - Hardware status
  - Problem: Switch-On order
  - Problem: Destroyed SPIROCs
  - Beam- / Noise rate and SPIROC2d/3 considerations
- SM_HBU Status (AHCAL option)
- EBU Status (ScECAL)



Shower in 5 AHCAL layers (DESY testbeam)

AHCAL operation in ILC-like environment



- Operation for the first time in steel cassettes with final dimensions and in absorber stack.
- No increased noise, no obvious shift of MIP position with respect to lab setup.
  => dense EUDET mechanical concept validated!

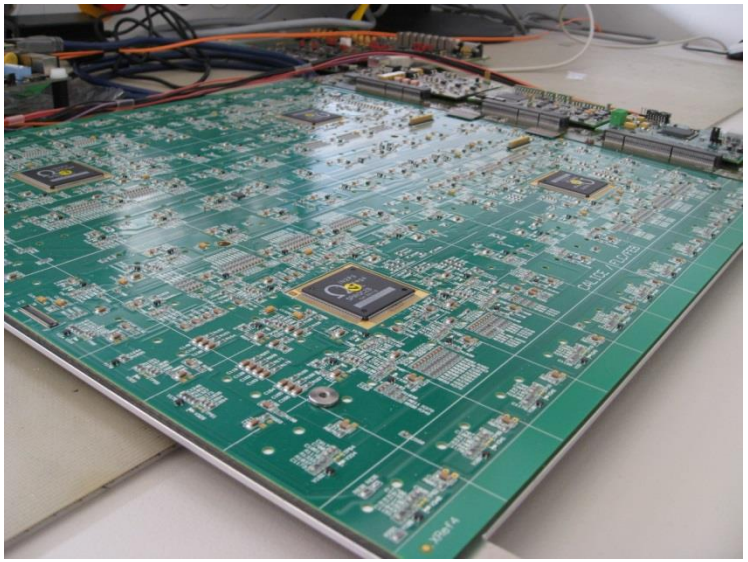
Hardware Status

- HBU2: (two production runs): 14 boards. (tiles?)
- FE-DAQ: DIF (NIU), CIB, POWER and CALIB: 20 boards.
- Flexleads (2 types, a lot in use): 14 boards (each type)
- EBU vertical: 4 boards
- EBU horizontal: 4 boards (in production, expected beginning Oct.)
- SM_HBU: 2 boards

- Delivered complete sets (HBU/EBU/SM_HBU + FE-DAQ modules) to:
  Shinshu, Mainz, NIU. One further HBU to Wuppertal.

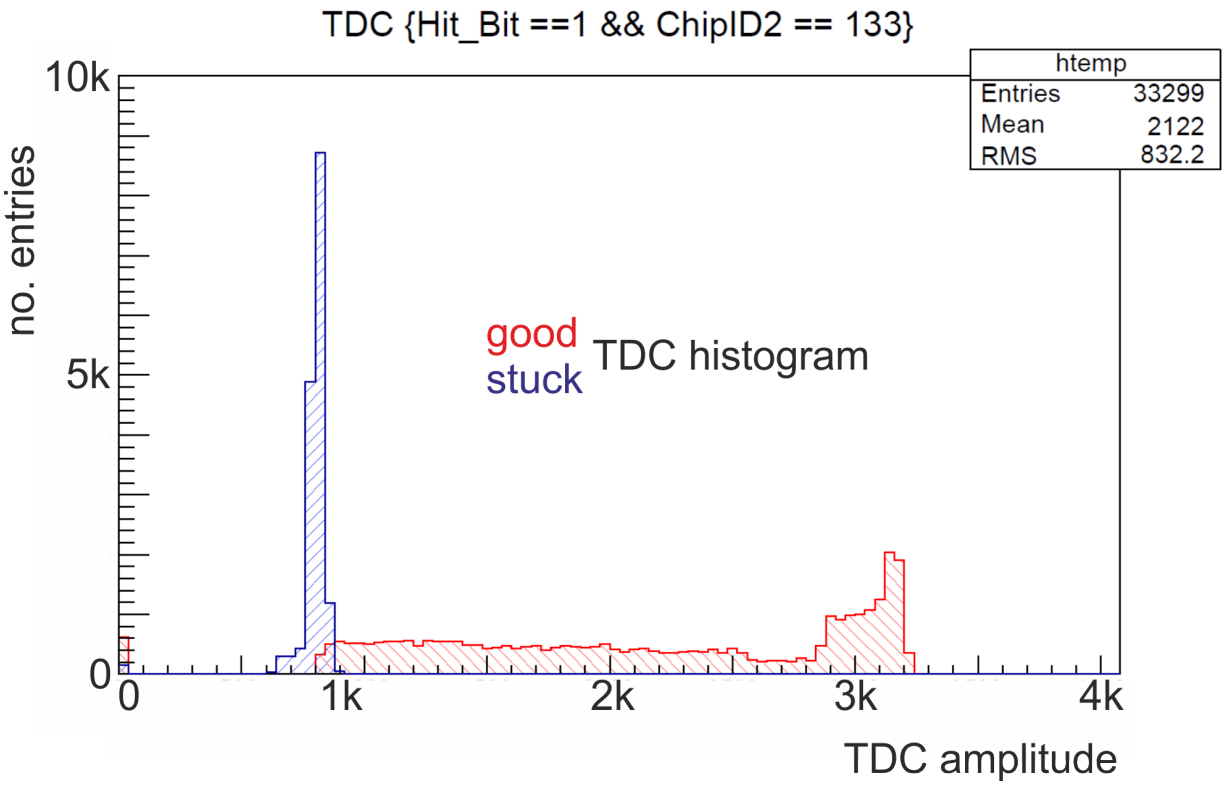
New 8 HBU2 boards

- All 8 new HBU2s have been tested and work fine.
- Problem: Significant spread of board dimensions within the 8 boards. Landmarks differ up to 0.4mm (0.1mm was specified).
- Problems during PCB assembly and with the steel cassettes (individual cassettes needed).



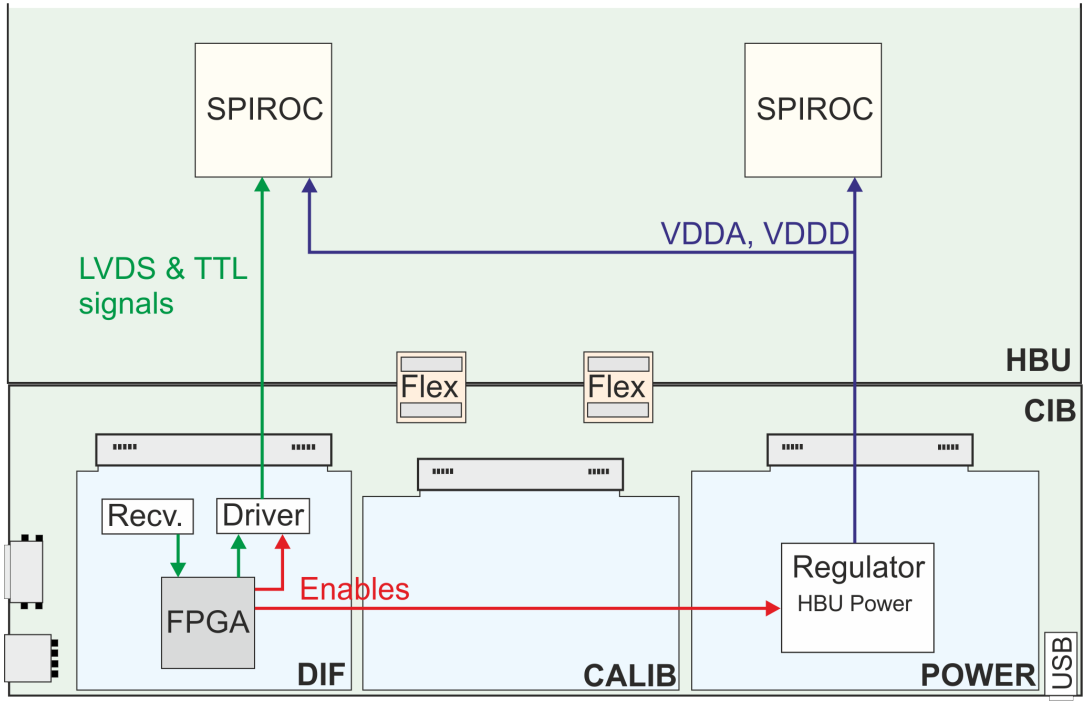
- From the discussion with PCB manufacturer: For the next order, there will be a pre-compensation process step for the inner pcb layers before the pressing operation. **This will solve the problem as it did for the first 6 HBUs.**

Detector Power-Up Problem



- Arbitrary operating conditions in multilayer setup (very seldom in single-layer setup): Stuck TDC, spontaneous noisy channels, shifted MIP position.
- SPIROC reset does not help, only re-powering helped.

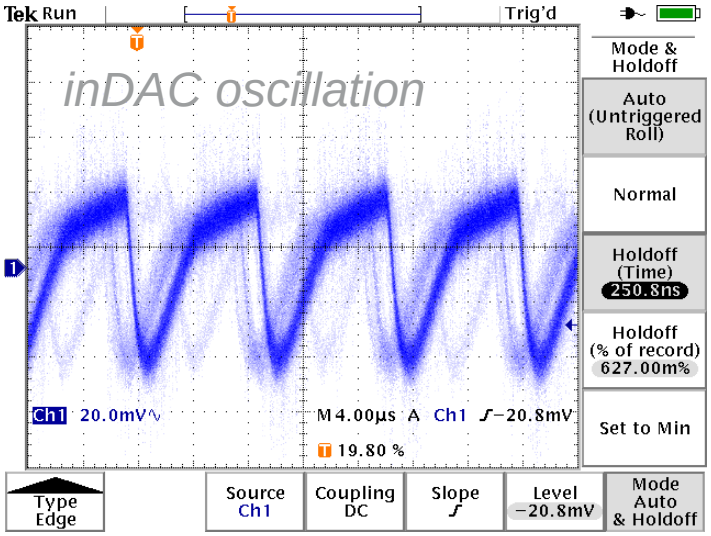
Solution for Power-Up Problem

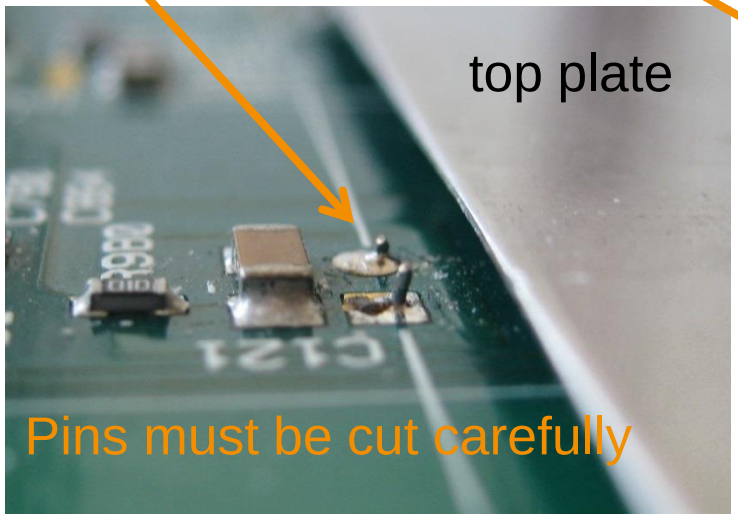


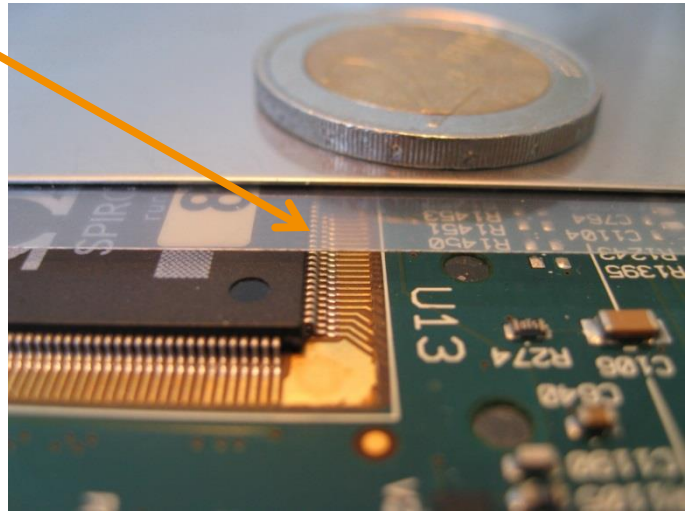
- Problem identified: After power-up and booting, the DIF FPGA sets TTL lines to SPIROCs before enabling SPIROC's power. => SPIROCs get power through protection diodes of input channels.
- New switch-on order cured the problem.

Broken SPIROCs in testbeam

- During testbeam 6 out of 20 SPIROCs on three HBU2s have been damaged.
- Damage is the same for all chips: oscillating input DACs.
- Best explanation so far: SiPM pins have damaged the isolating foil and touched the steel cassette's top plate. => Stronger foil ordered.

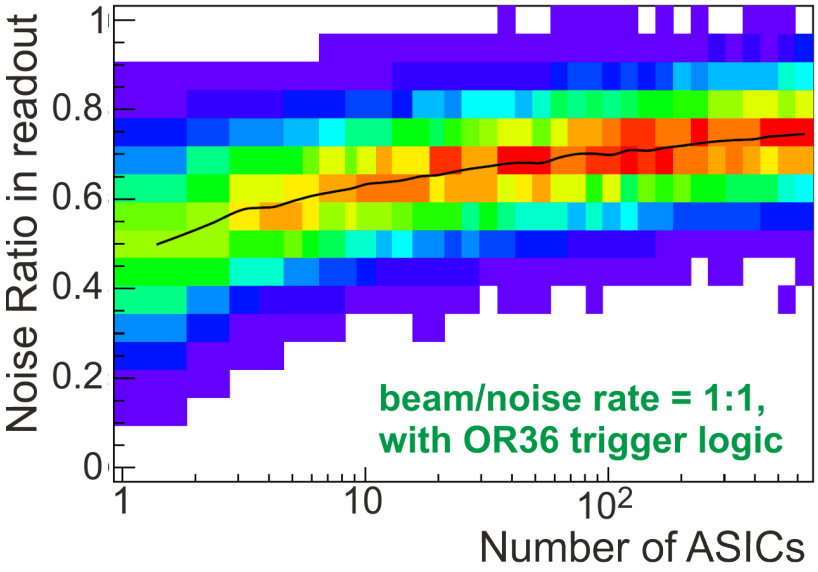


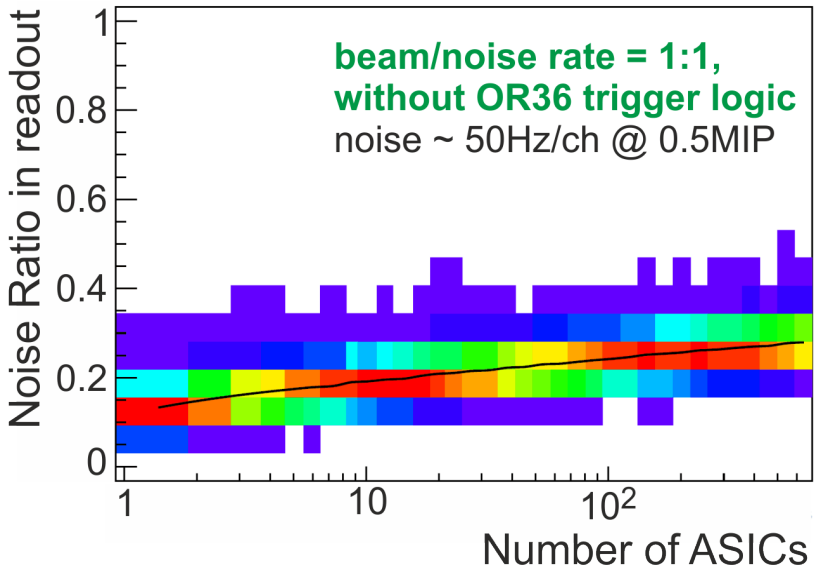




Beam rate to noise rate considerations

- Can we operate 1m³ (~600 SPIROCs) with current SiPMs and ASICs?

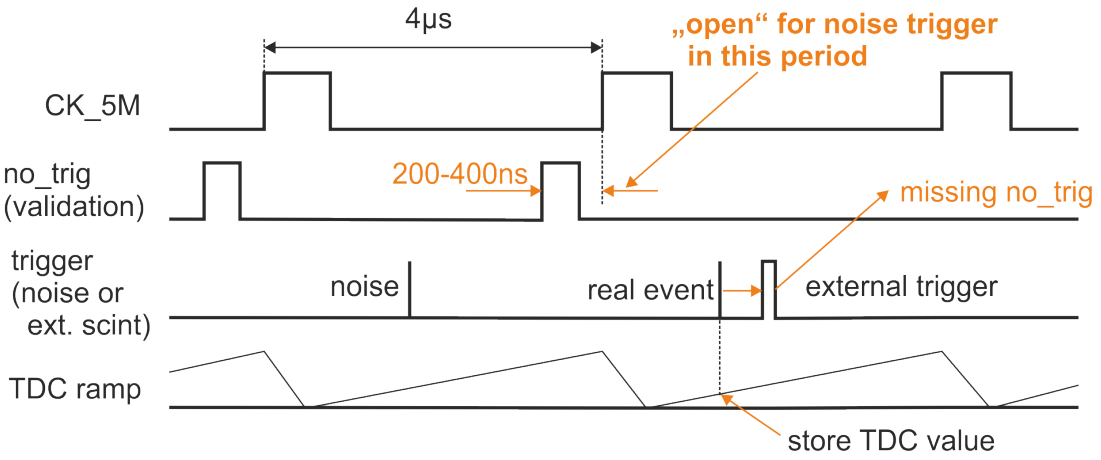




Simulations by Oskar Hartbrich

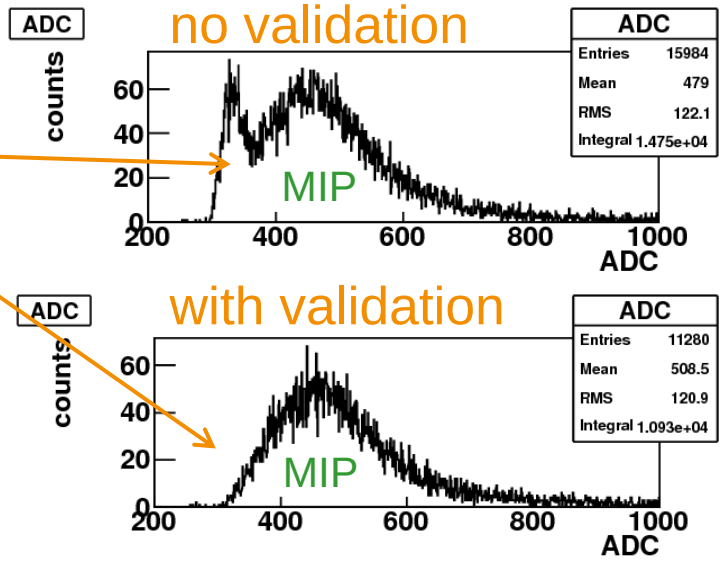
- Simulation studies of beam/noise-rate started to investigate the amount of noise events in the AHCAL detector for various operation conditions.
- Exponential distributions for noise- and beam rates assumed. Different trigger architectures and memory depths under study.
- First conclusion: First memory cell problem (ADC data “0”) must be solved (low occupancy in last layers). Was solved for SP2c already.

Trigger Validation (Testbeam mode)



- Only stores events that are validated by an external trigger signal

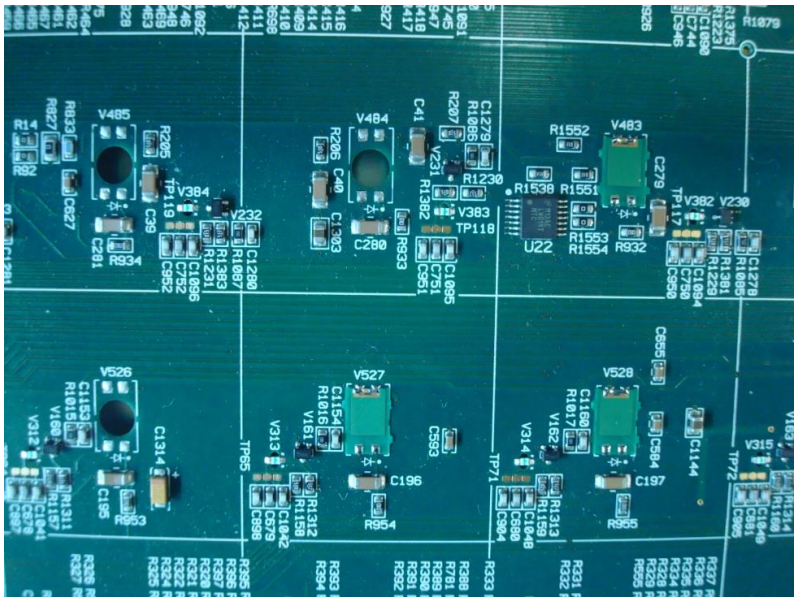
- **Validation works fine**: Histogram only shows MIP events without noise/pedestal contributions.
- Problem: Validation does not work for noise hits between no_trig and rising CK_5M edge (200-400ns). **Triggers in this period should be rejected (=> dead time).**
- Now: Factor 10 noise reduction. Improve 400ns window size.



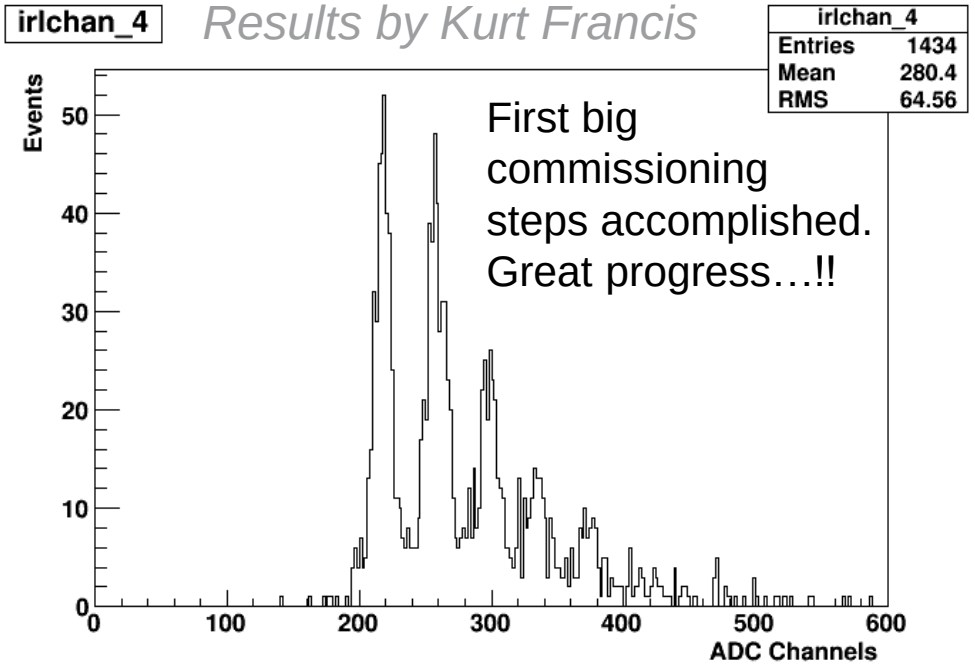
Northern Illinois University

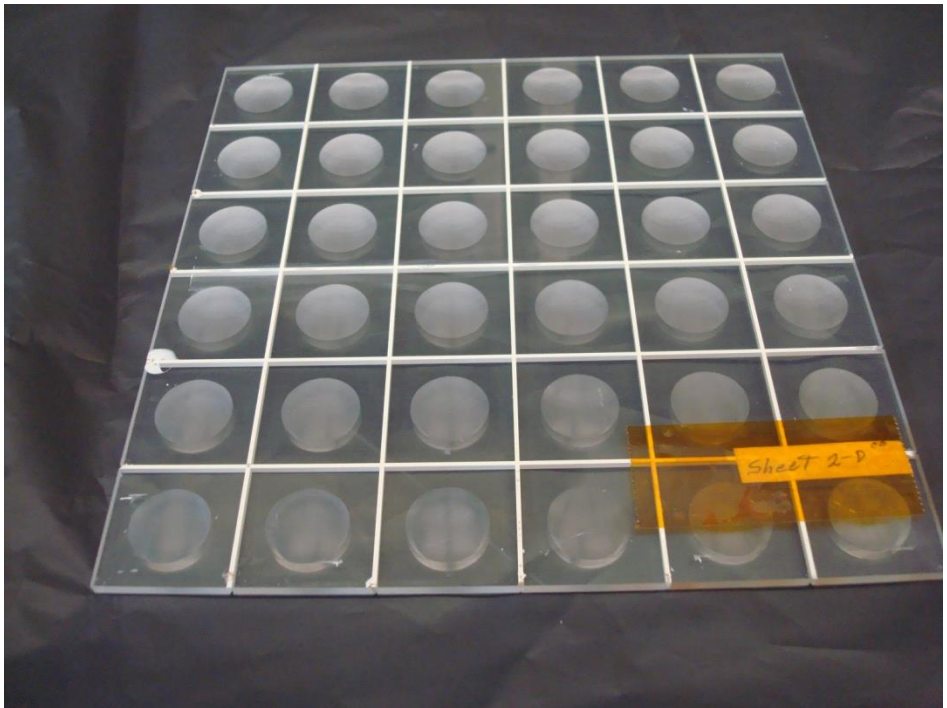
Integrated Readout Layer

- **Uses HBU2 FE**
- **Hamamatsu MPPC mounted on small flex circuits**
- **Scintillator "Megatile" with 3 x 3 cm cells optically isolated with white epoxy**
- **Cells have a concave dimple improve the uniformity of the response and to direct light through hole in board onto MPPC**
- **Easier to assemble, does not need WLS optical fiber**



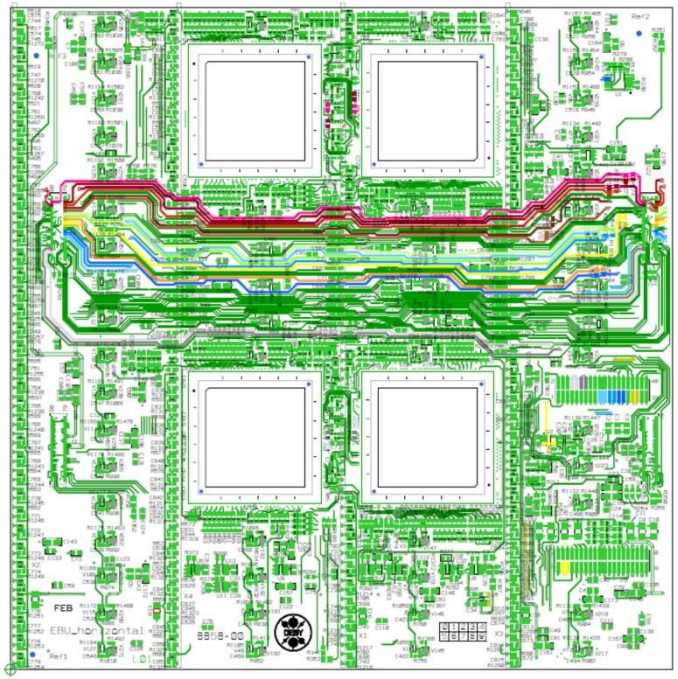
Results by Kurt Francis

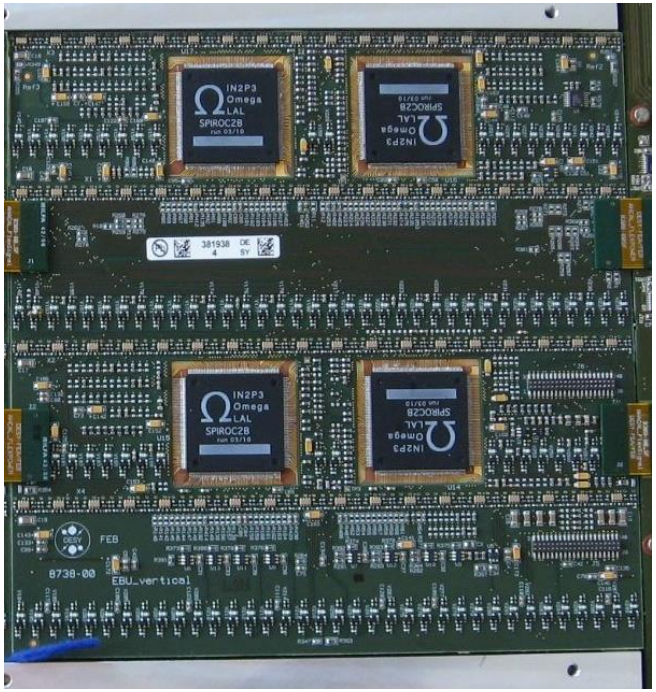




EBU status (ScECAL)

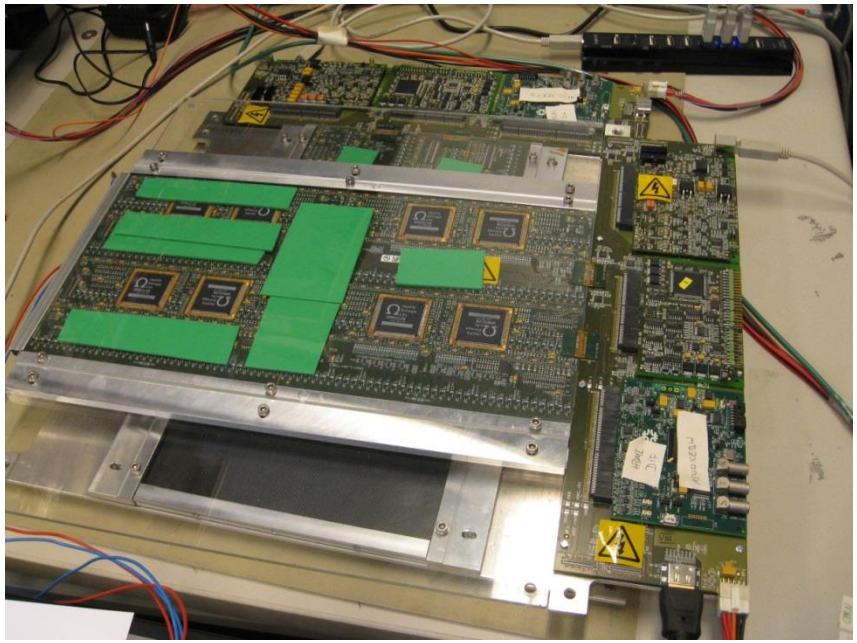
- EBU-vertical (right): 4 boards realized
- EBU-horizontal (left): 4 boards in production, expected beginning of October:
- Final ScECAL module assembly from Shinshu at DESY in close coorporation.

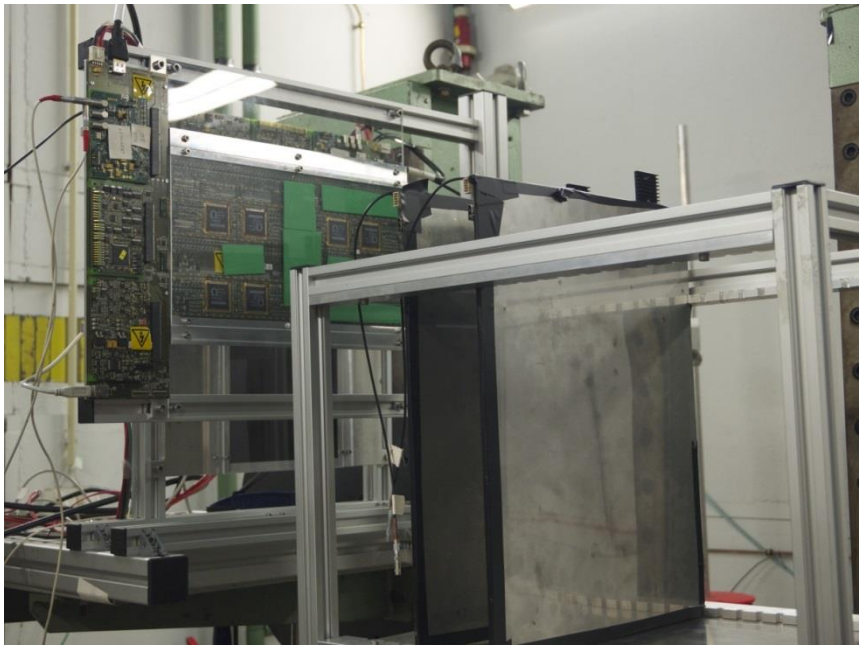




- EBU-horizontal requires long flexleads for EBU/EBU connection (in layout design).

EBU status (ScECAL)





- 2 ScECAL layers in lab, perpendicular strip orientation
- 1 setup with 2 EBUs in a row, 1 setup with 1 EBU

- Two ScECAL layers with two AHCAL layers together in DESY testbeam, operated synchronously and together by the AHCAL DAQ.
- For results see Shinshu talk.

Conclusions

- Multilayer operation of AHCAL (and ScECAL) has been established. Further modules in production.
- 2nd EBU-type in production.
- SM_HBU with big progress at NIU.
- Additional things to keep in mind for SPIROC2d / SPIROC3:
  https://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=5891:
  talk: “Experiences with the AHCAL testbeam prototype”
- Ongoing studies: Power-Pulsing with slab (6 HBU2s).

Backup Slides

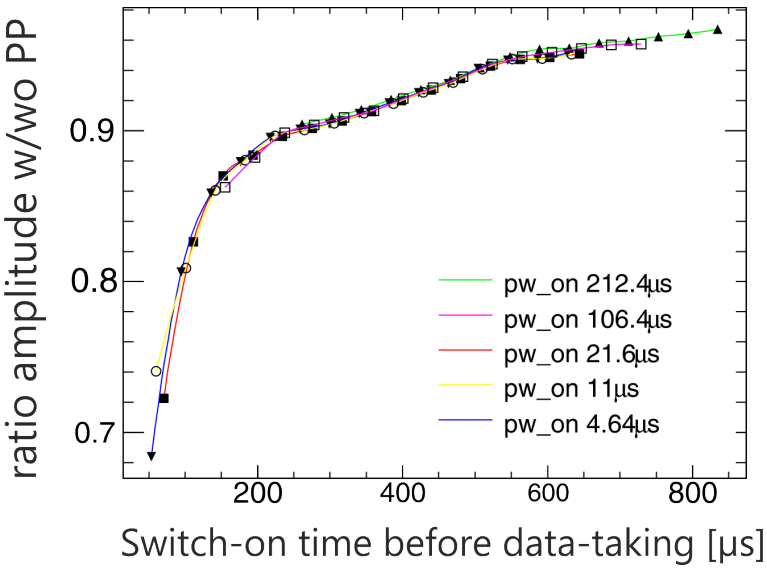
Towards the next SPIROC

Topics to keep in mind …

- Pedestal shift @ huge signals, pedestal different for internal/external trigger.
- Memory cell dependent amplitude decay. Solved by compensation caps.
- Slow-Control configuration is problematic for long slabs.
- Feedback of channel-wise trigger thresholds on the global threshold.
- Random zero events and zero-results for the first trigger.
- Poor uniformity of the input DACs.
- Holdscan is different for HG/LG.
- Trigger threshold width increases with threshold height.
- Amplitude-to-threshold relation depends on preamp. setting and pulse shape.
- TDC: Amplitude dependent time-shifts and channel-to-channel spread.
- TDC: Result depends on which ramp is used and the memory cell.
- TDC: big chip-to-chip spread of ramp slopes.

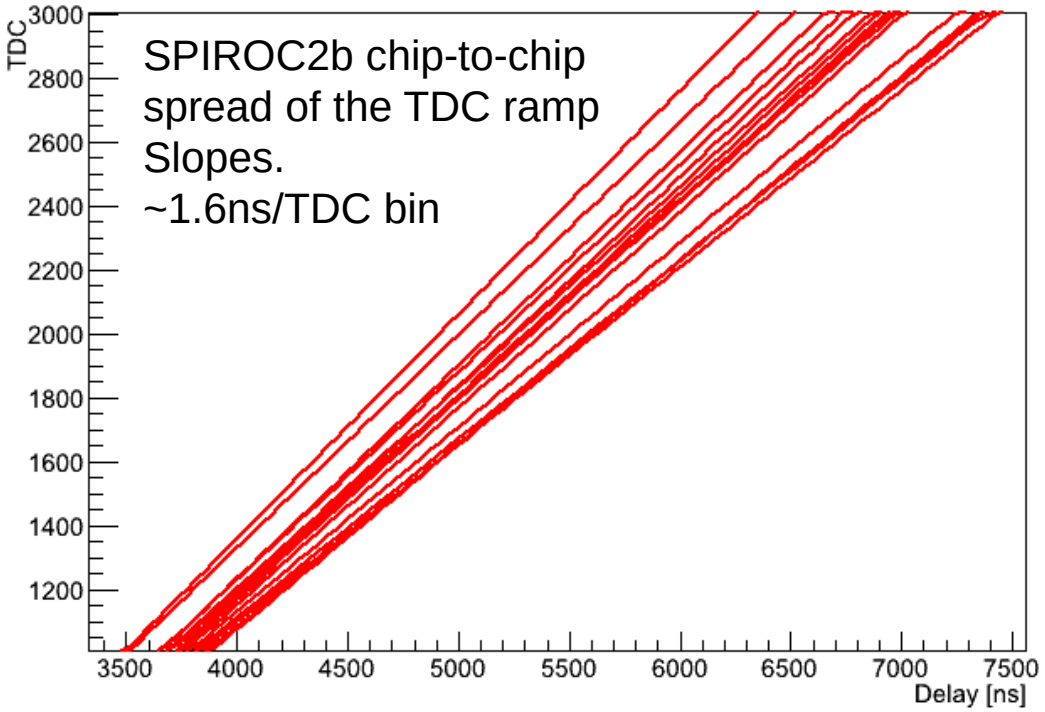
Power and Power Pulsing (PP)

- Aim: Switch on as short as possible before data taking starts (initial idea: 20µs).
- Results with charge injection show a decreased amplitude response with PP.
- Single-Pixel Spectra measurements show a reduced amplitude with PP.
- Aimed power dissipation of 20µW per channel not reached yet.

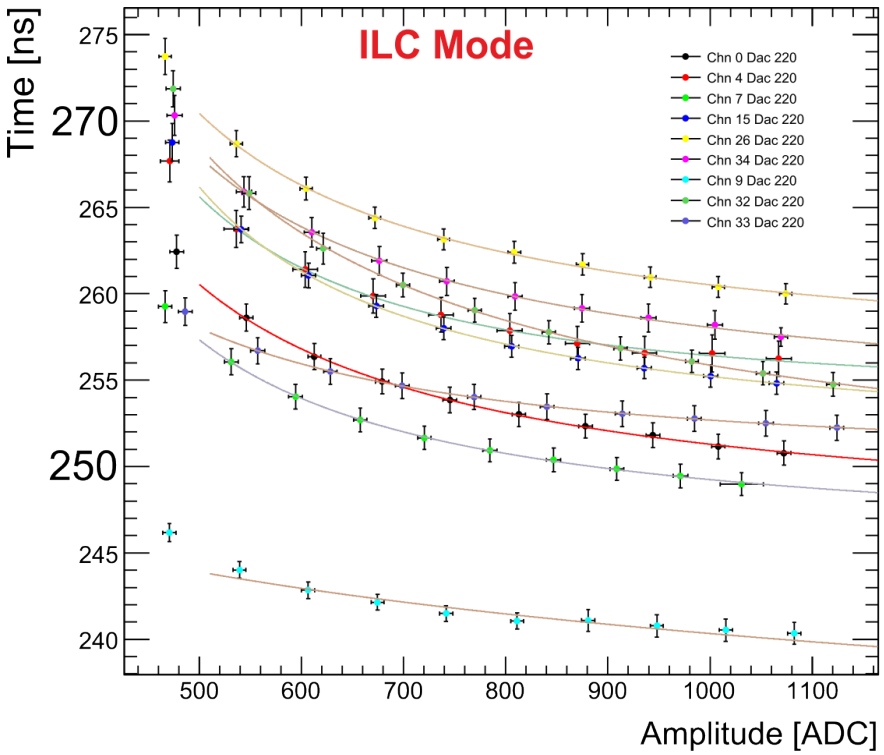


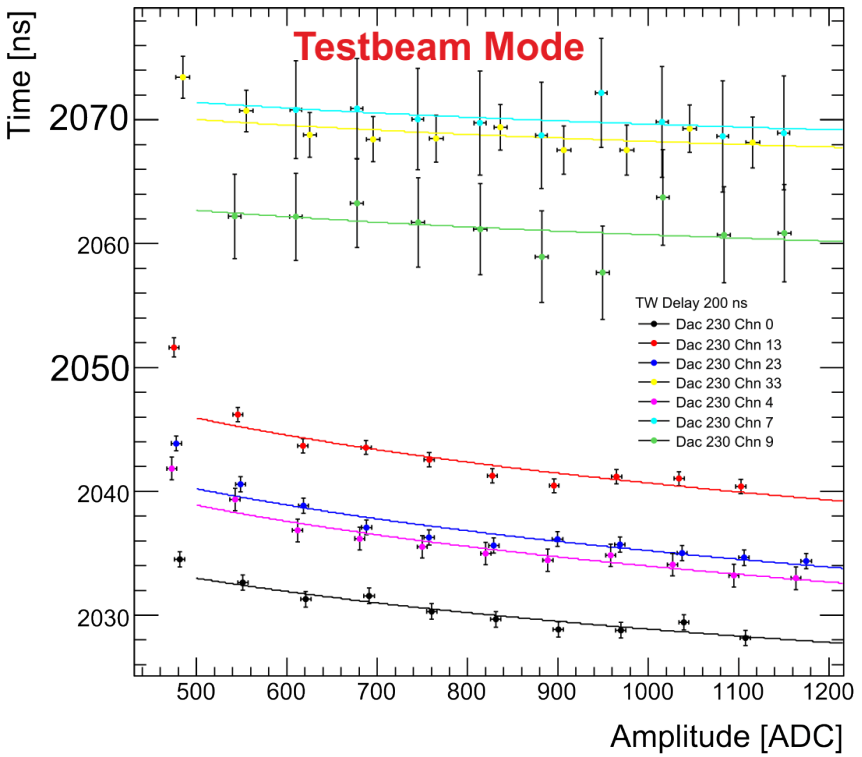
TDC Calibration – CERN Module

- Calibration of all 16 SPIROC2b ASICs of the CERN Testbeam-module with charge injection.
- Chip-to_chip spread of the TDC ramp slopes: Calibration necessary: TDC (time measurement!).



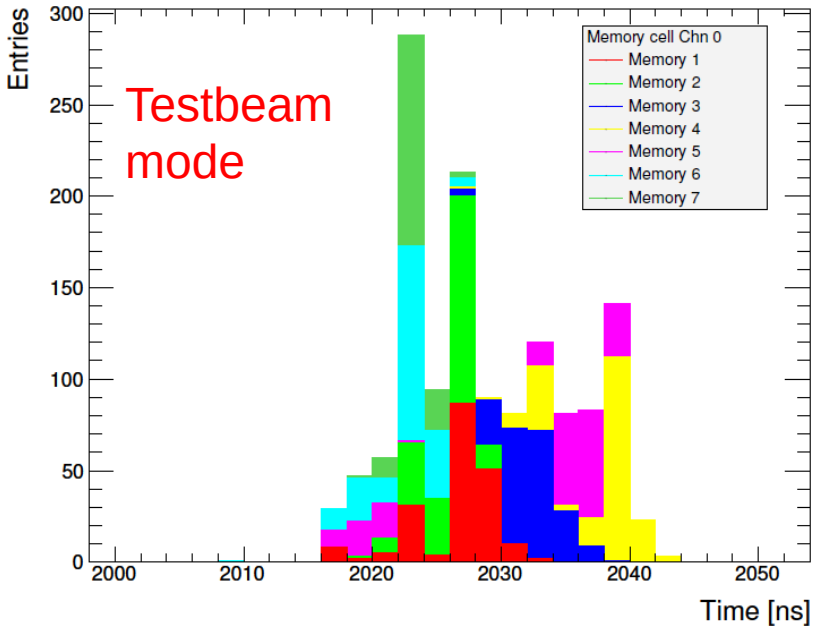
TDC: Time Walk and Channel-to-Channel Spread

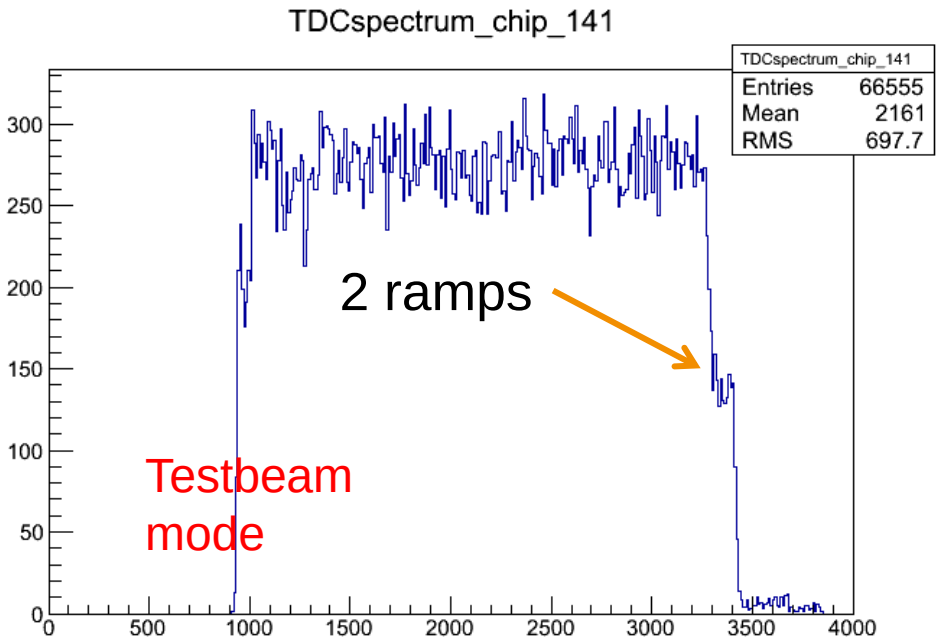




- Amplitude-dependent time-shifts and channel-to-channel differences.
- Difficult to parameterize because of different behaviours. Channel-wise TDC calibration necessary as for ADC (MIP calibration)?

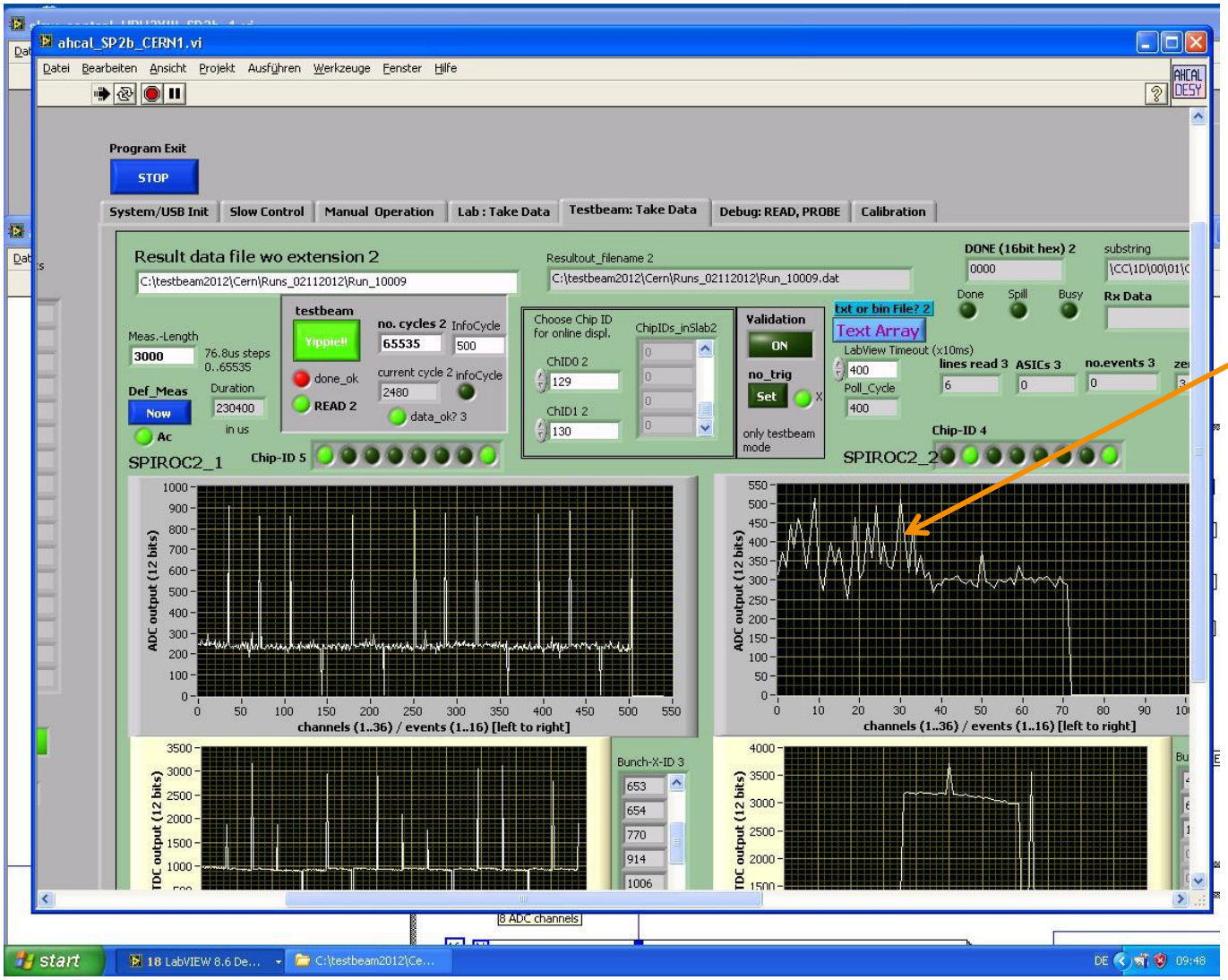
TDC: Memory Cell Dependence and „2-Ramp“ Problem





- TDC result depends on memory cell
- The SPIROC2b internal TDC ramps have different amplitudes and for a specific event it cannot be identified with which ramp the TDC result has been achieved (known problems).

Start-Run Problem

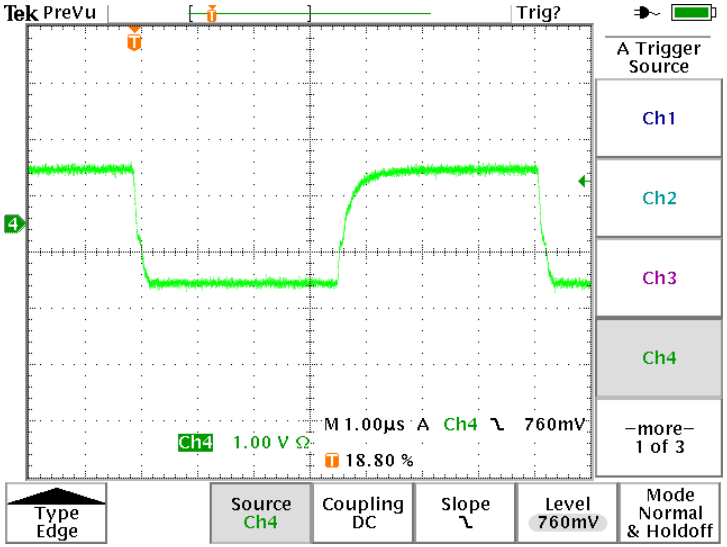


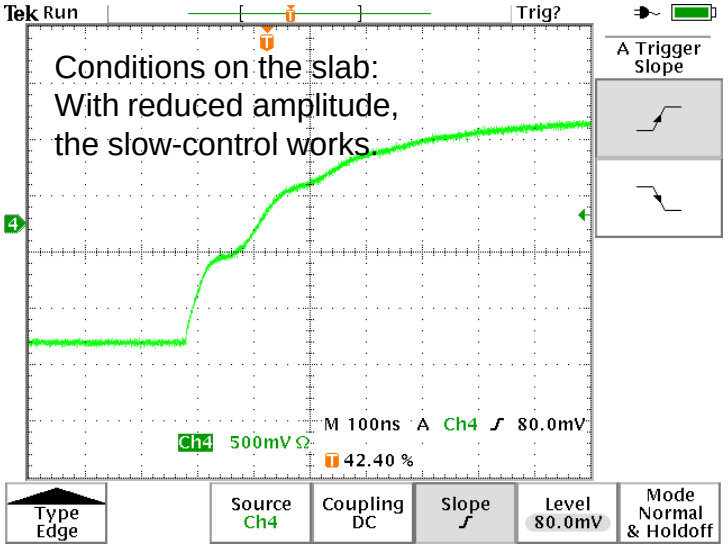
CERN testbeam

High noise on pedestal for first 1-2 readout cycles

Slow-Control Problem

- For longer AHCAL slabs, the slow-control programming is instable. Reason: Slow-control clock, special pulse-shape needed (series R, termination R, block-C)





- Although the slow-clock looks fine, the configuration does not work.
- Analysis ongoing, I2C in SPIROC3.