Sensor and readout R&D for the CLIC vertex detector

AWLC14

May 15th, 2014

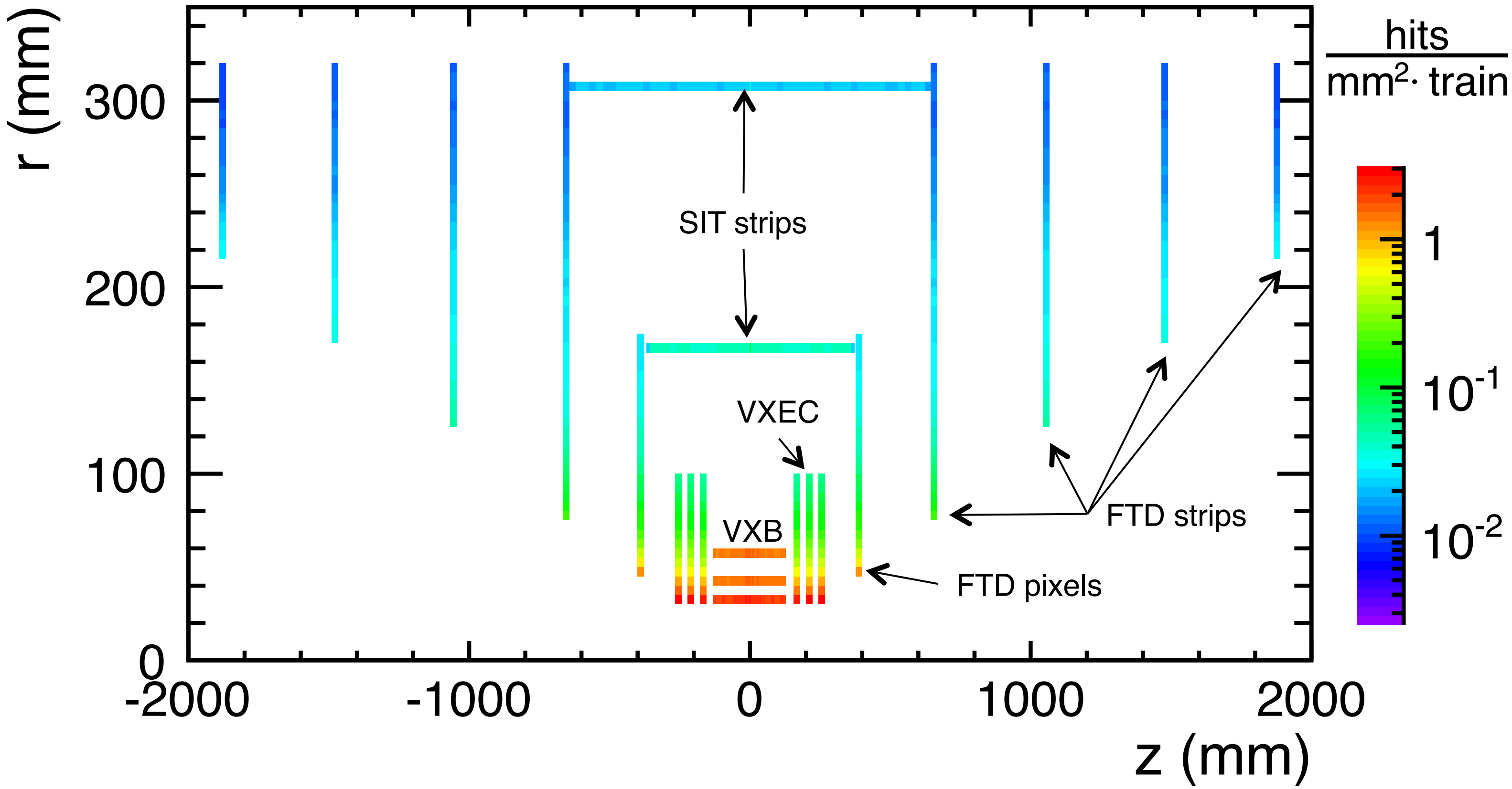
Dominik Dannheim (CERN-LCD)
on behalf of the
CLIC detector and physics collaboration

Outline

- Reminder: CLIC vertex-detector requirements
- CLICpix
- Thin-sensors in test beams
- HV-CMOS with capacitive coupling
- TSV
- Summary / Conclusions

Backgrounds in inner tracking region

CLIC_ILD incoherent pairs + $\gamma\gamma \rightarrow$ hadrons: silicon hits, no safety factors



- Train occupancies up to 3% in vertex region (including clustering and safety factors)
- moderate radiation exposure, ~10^4 below LHC

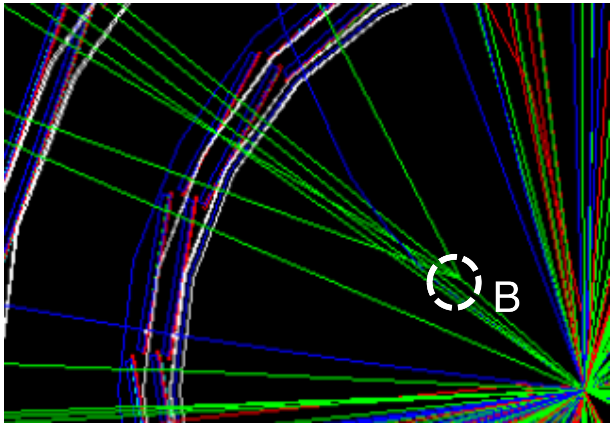
Region	Readout granularity	Max. occup.	NIEL [$n_{eq}/cm^2/y$]	TID [Rad/y]
VXB	20 µm x 20 µm	1.9 %	4×10^{10}	20k
VXEC	20 µm x 20 µm	2.8 %	5×10^{10}	18k
FTD pixels	20 µm x 20 µm	0.6%	2.5×10^{10}	5k
FTD strips	10 cm x 50 µm	290 %	1×10^{10}	700
SIT	9 cm x 50 µm	170 %	2×10^{9}	200

Vertex-detector requirements

- Efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

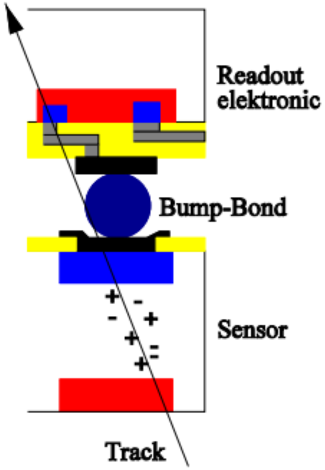
a~5 μm, b~15 μm



→ good single point resolution: σ_{SP}~3 μm
  → small pixels ~25x25 μm², analog readout
→ low material budget: X ≲ 0.2% X_0 / layer
  → corresponds to ~200 μm Si, including supports, cables, cooling
  → low-power ASICs (~50 mW/cm²), power pulsing, air-flow cooling

- Time slicing with ~10 ns accuracy, to suppress beam-induced backgrounds
  → High-resistivity sensors, fast readout
  → Hybrid concept (like for LHC detectors):
    ultra-thin sensors
    + high-performance r/o ASICs

Hybrid pixel technology

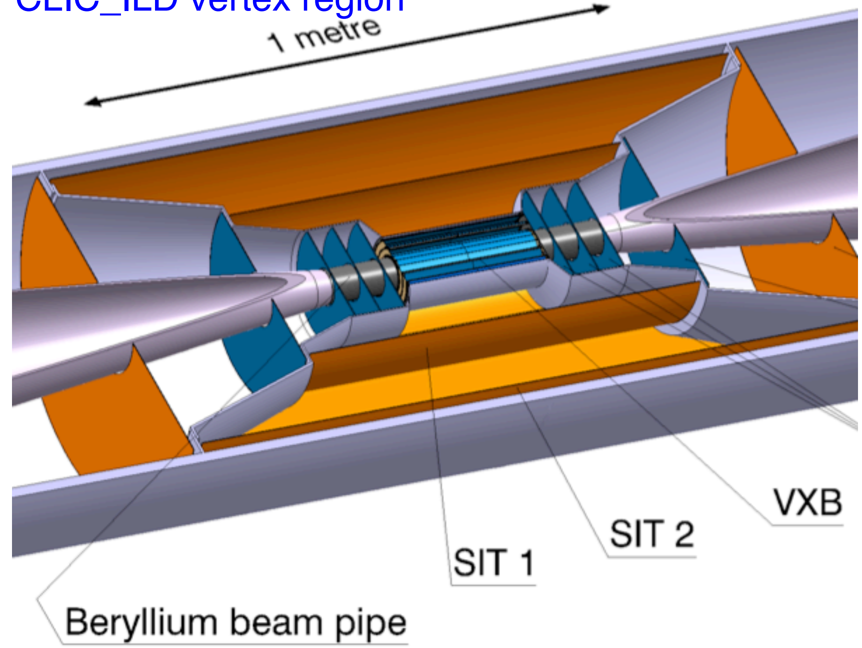


- Trigger-less readout during 20 ms gaps between trains

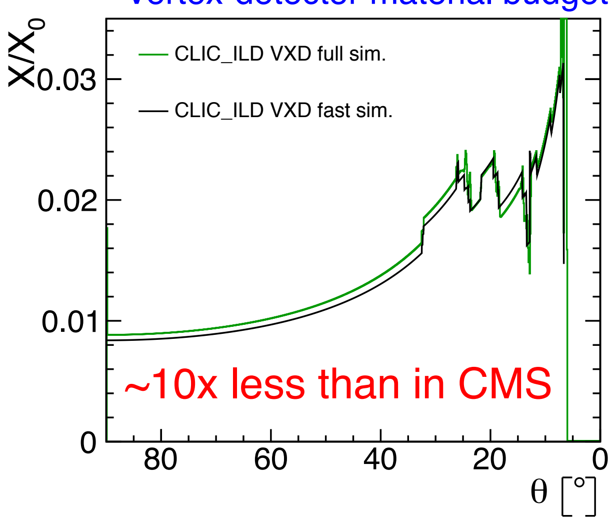
Vertex-detector concepts

- systematic optimization of geometries:
  - background occupancies
  - detector performance
- large coverage: $\theta > 7^o$ ($|\eta| < 2.8$)
- 3 double layers or 5 single layers
- ~1 m^2 area, ~2G pixels
- R_i ~ 30 mm
- beam pipes with conical sections

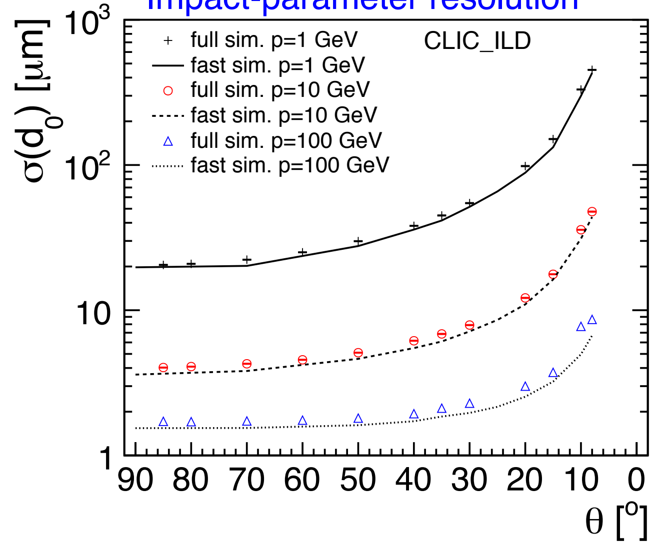
CLIC_ILD vertex region



Vertex-detector material budget



Impact-parameter resolution



Medipix/Timepix hybrid r/o chip family

Chip	Year	CMOS Process	Pitch [μm^2]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm	55x55	∫TOT or ToA or γ counting	Sequential (full frame)	HEP (TPC)
Medipix3RX	2012	130 nm	55x55	γ counting	Sequential (full frame)	Medical
CLICpix demonstrator	2013	65 nm	25x25	TOT + ToA	Sequential (data comp.)	Test chip with 64x64 pixel matrix
Timepix3	2013	130 nm	55x55	TOT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
Velopix	2015	130 nm	55x55	TOT + ToA, γ counting + ∫TOT	Data driven	LHCb (10x Timepix3 rate)
Smallpix/ Timepix4	2016	65 nm (t.b.c.)	~35x35	TOT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
CLICpix	tbd	65 nm	25x25	TOT + ToA	Sequential (data comp.)	CLIC vertex detector

TOT: Time-Over-Threshold
→ Energy
ToA: Time-of-Arrival
→ Time stamping

- Taking advantage of smaller feature sizes:
  - Increased functionality and/or
  - Reduced pixel size
  - Improved noise performance

Hybrid r/o technology: CLICPix

- **65 nm CMOS hybrid r/o chip**, targeted to CLIC vertex detectors
- based on **Timepix/Medipix** chip family, synergy with HL-LHC pixel r/o projects (**RD53** collaboration on 65 nm r/o)

- **demonstrator chip** produced with fully functional 64 x 64 pixel matrix
- **25 µm** pixel pitch
- simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel

→ front-end **time slicing < 10 ns**

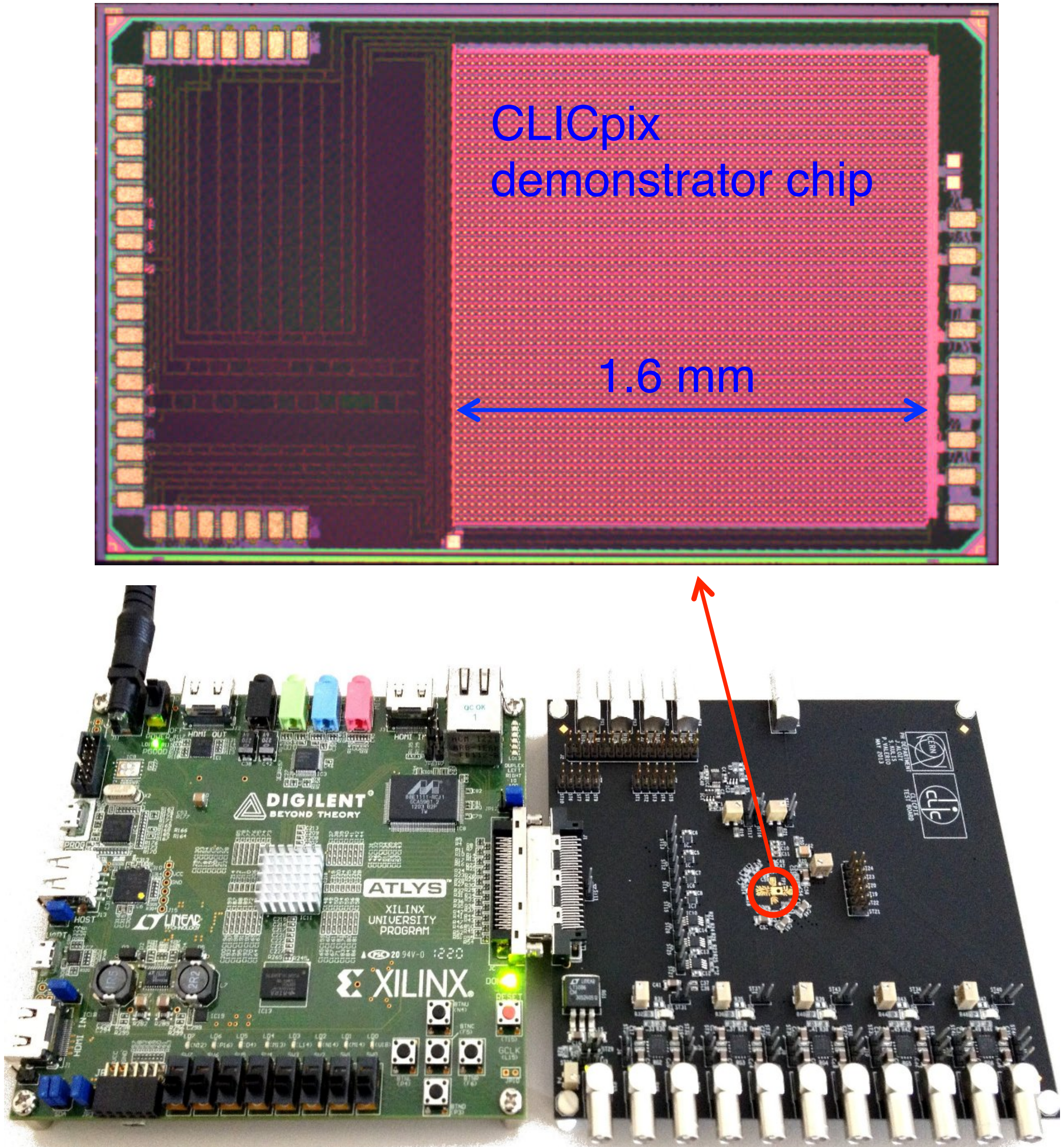
- selectable **compression** logic: pixel, cluster + column-based

→ full chip r/o in less than 800 µs (at 10% occup., 320 MHz r/o clock)

- **power pulsing scheme**

→ $P_{avg} < 50\ \mathrm{mW/cm^2}$

- **r/o tests** on prototypes:
  - chip fully functional
  - measurements confirm simulations



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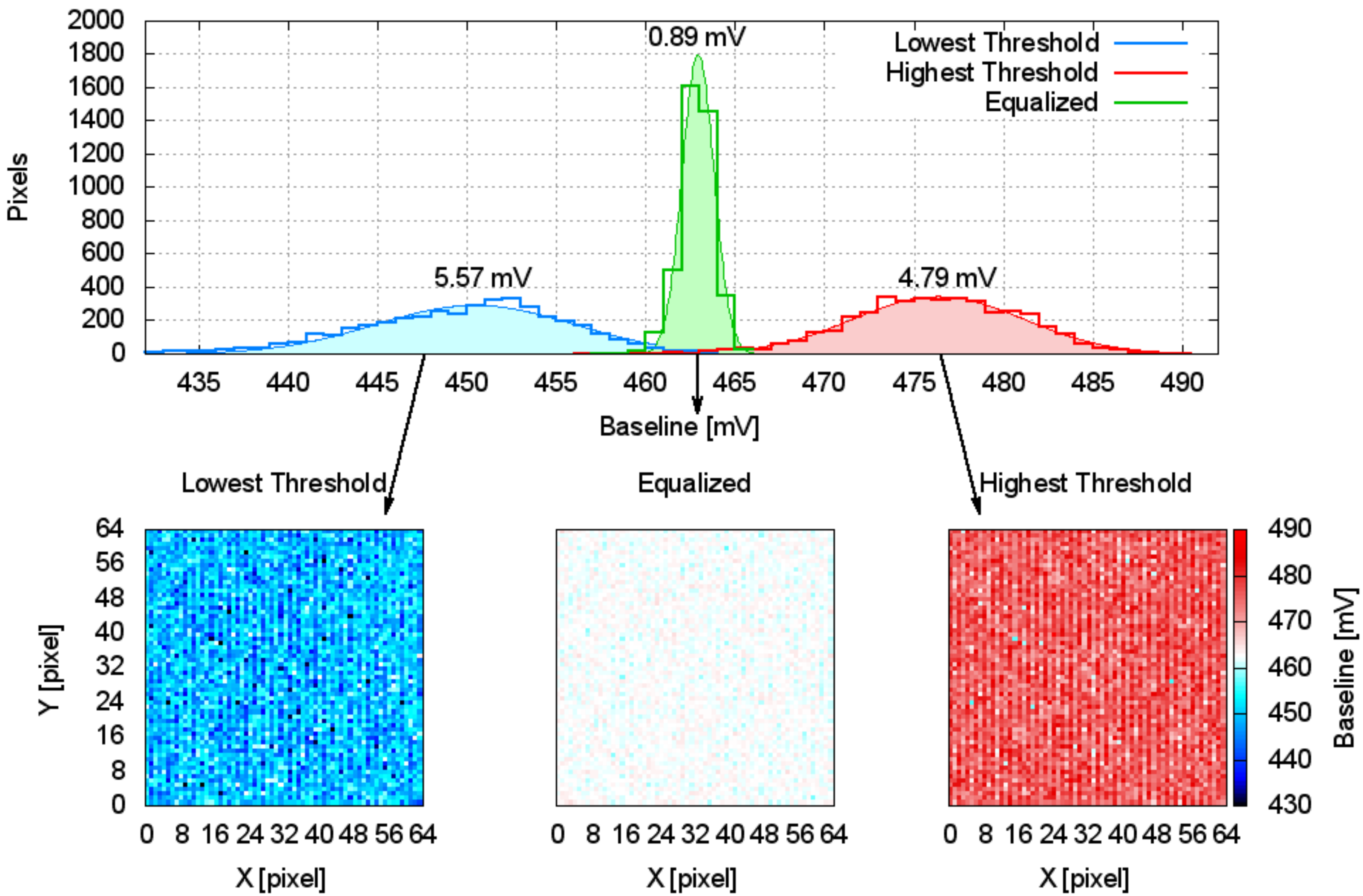
CLICpix: baseline equalization



Calibrated spread across the whole matrix is 0.89 mV RMS (~22 e^-)
For comparison: MIP signal in 50 µm silicon ~3700 e^-

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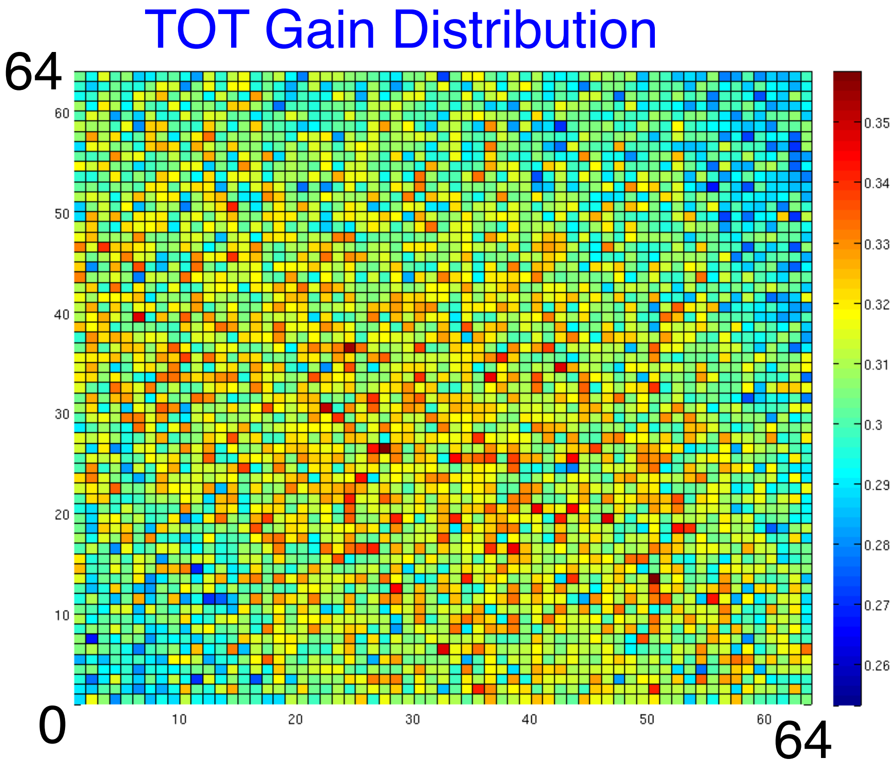
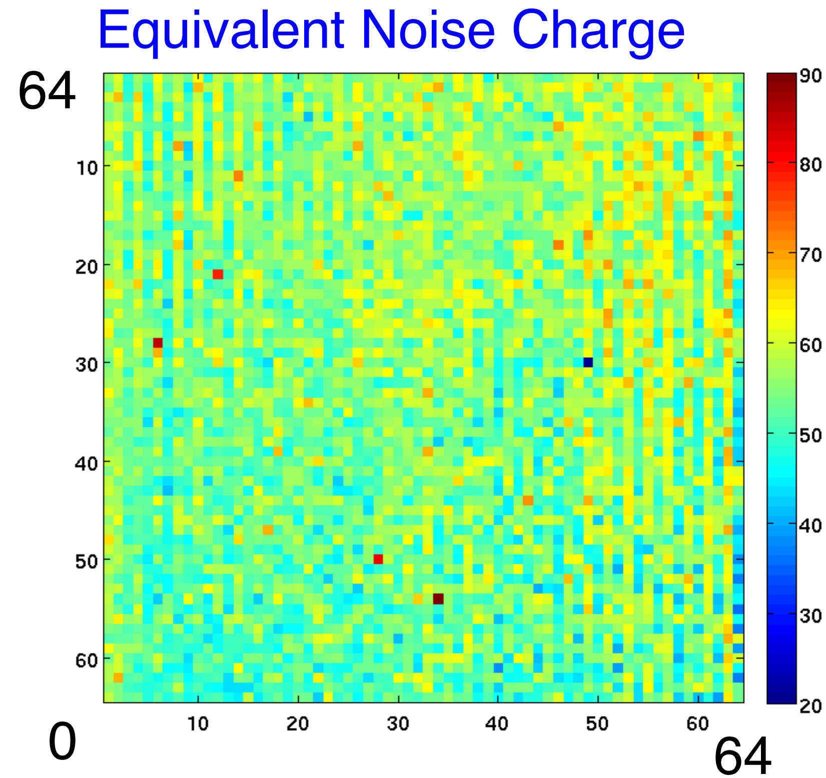
CLICpix: uniformity of gain and noise





- Uniform gain across the matrix
- Gain variation ~4.2% r.m.s. (for nominal feedback current)

- Uniform ENC across the matrix
- Mean ENC: 55 e^-, SD: 5.7 e^- (without sensor)

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CLICpix: summary

Parameter	Unit	Simulation	Measurement
Rise time	[ns]	50	-
TOA accuracy	[ns]	<10	<10
Gain	[mV/ke$^-$]	44	40 *
Dynamic range	[ke$^-$]	44 (configurable)	40 * (configur.)
Integr. nonlinearity (TOT)	[LSB]	<0.5	<0.5
ENC (w/o sensor)	[e$^-$]	~60	~55 *
DC spread σ (uncalibrated)	[e$^-$]	160	128 *
DC spread σ (calibrated)	[e$^-$]	24	22 *
Power consumption	[μW/pixel]	6.5	7

* results obtained with electrical test pulses

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- good agreement between simulations and measurements
- power pulsing works according to specifications (~100x reduction of average power)
- programmable power on/off times, front-end wake up within ~15 μs
- Radiation test: chip functional up to ~250 MRad

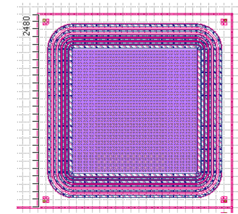
CLICpix v2

First ideas for new version of CLICpix:

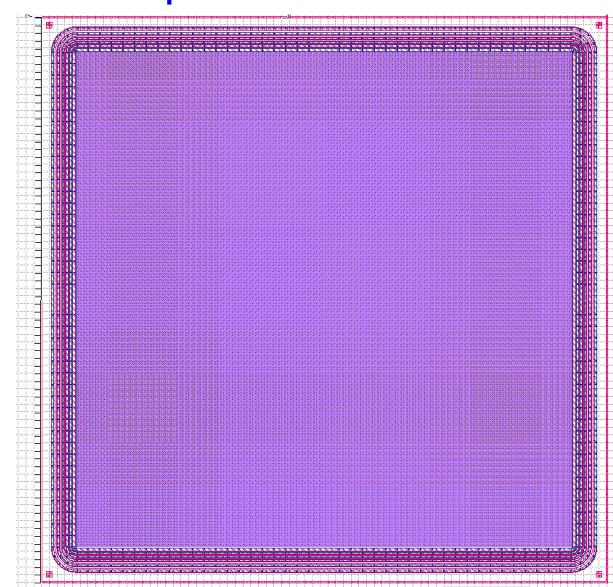
- larger pixel matrix (256x256)
- analog front-end re-design:
  sharing between adjacent pixels, to save space
  → allows for increased counter depth:
  - 5 bit TOA (instead of 4)
  - 7 bit TOT (instead of 4)
- share TOA between adjacent pixels
  (to be discussed)
  → would make space for 10 bit TOT
- on-board LDO
- PLL, band-gap blocks (RD53)
- features for daisy-chain
- bug fixes

- Launched sensor production
  for 256 x 256 CLICpix
  (in anticipation of new chip version)

CLICpix sensor 64x64



CLICpix sensor 256x256



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Thin-sensors

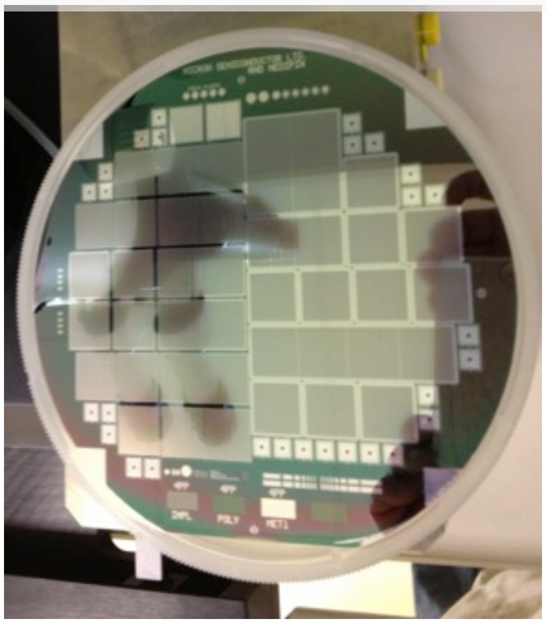
Micron + IZM and VTT/Advacam

Timepix planar sensor assemblies (55 µm pitch)

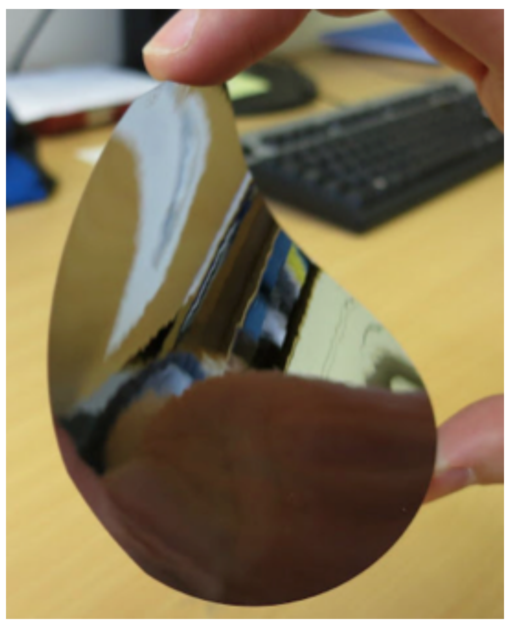
- Test feasibility of ultra-thin sensors and assemblies
- Assemblies delivered: 50-300 µm sensor thickness, 100-750 µm ASIC thickness
- sensors matching 25 µm^2 CLICpix footprint → 2014
- thinnest assembly: 100 µm sensor on 100 µm ASIC
- ultimate goal: 50 µm sensors on 50 µm ASICs

Micron/IZM assembly: 100 µm sensor on 100 µm Timepix ASIC

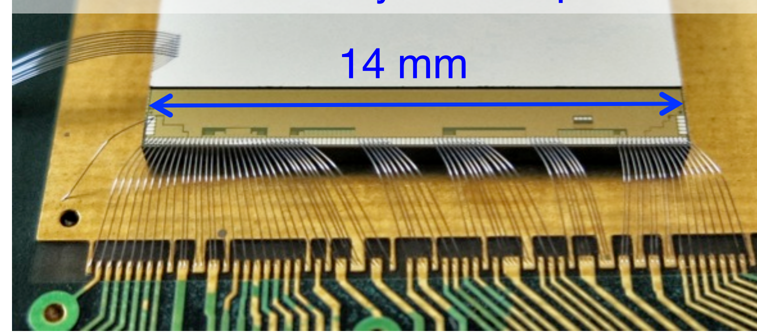
Micron sensor wafer 200 µm

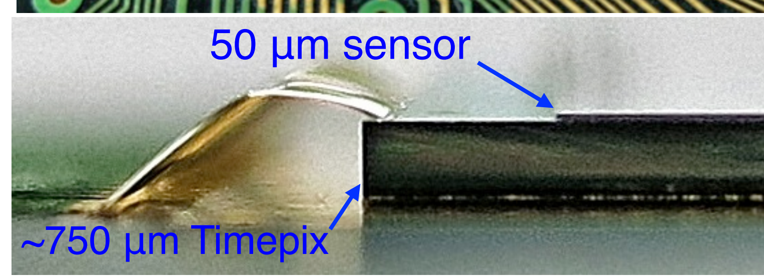


50 µm dummy wafer

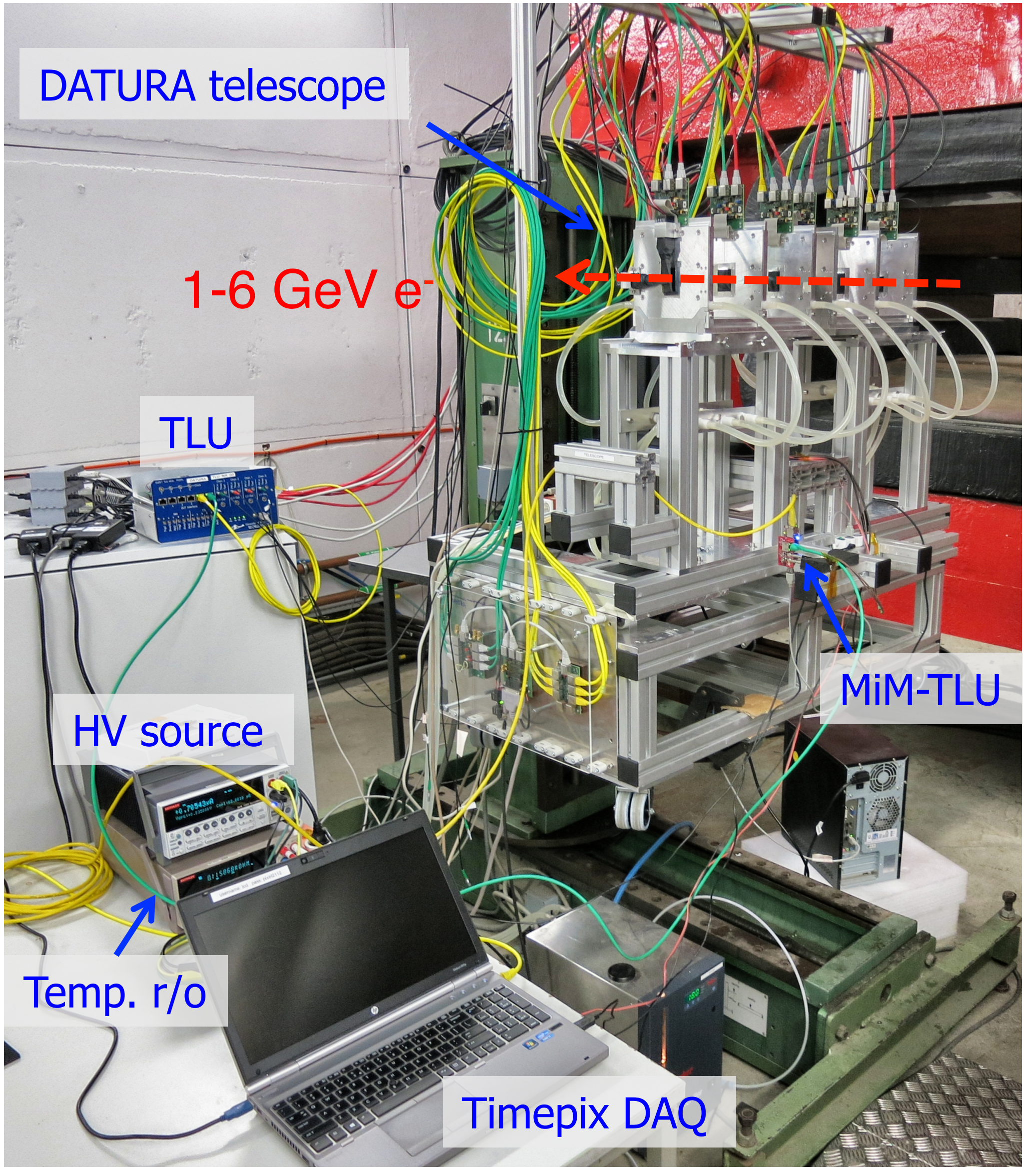


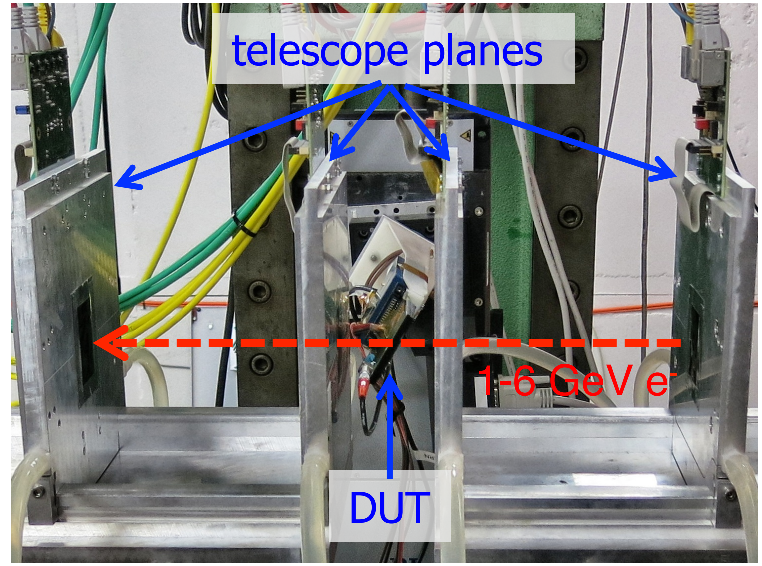
Advacam assembly with 50 µm sensor

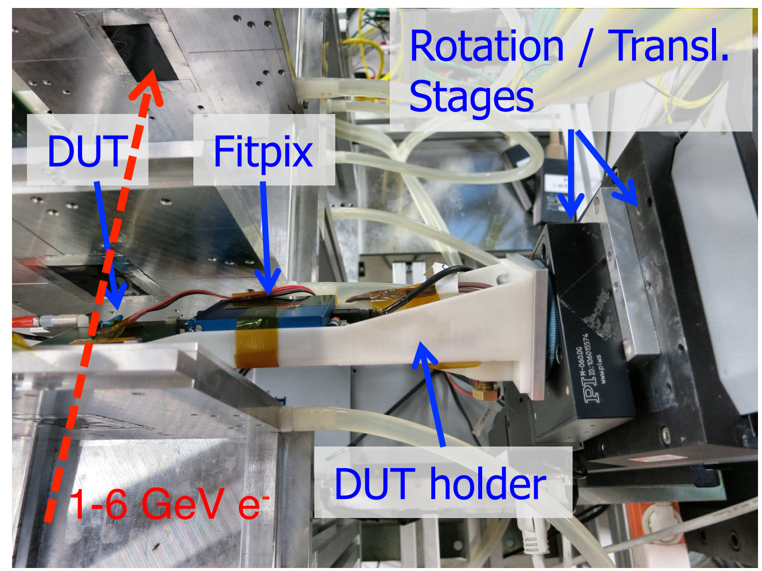




Test beam setup at DESY

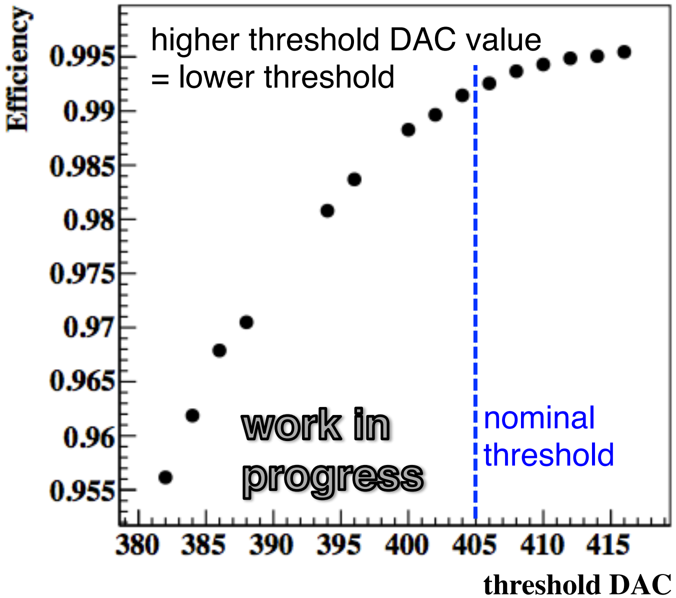






Thin-sensor assemblies in test beam

Threshold scan Advacam 50 µm active edge



Measurements in DESY II 5.5 GeV e^- beam

Assemblies with Advacam p-in-n sensors:

- 50 µm thick, 55 µm pitch
- 20 µm or 50 µm active edges
- Overall Efficiency > 99% (no fiducial cuts)
- Efficiency extends beyond last pixel row
- 80% of all tracks result in 1-hit clusters

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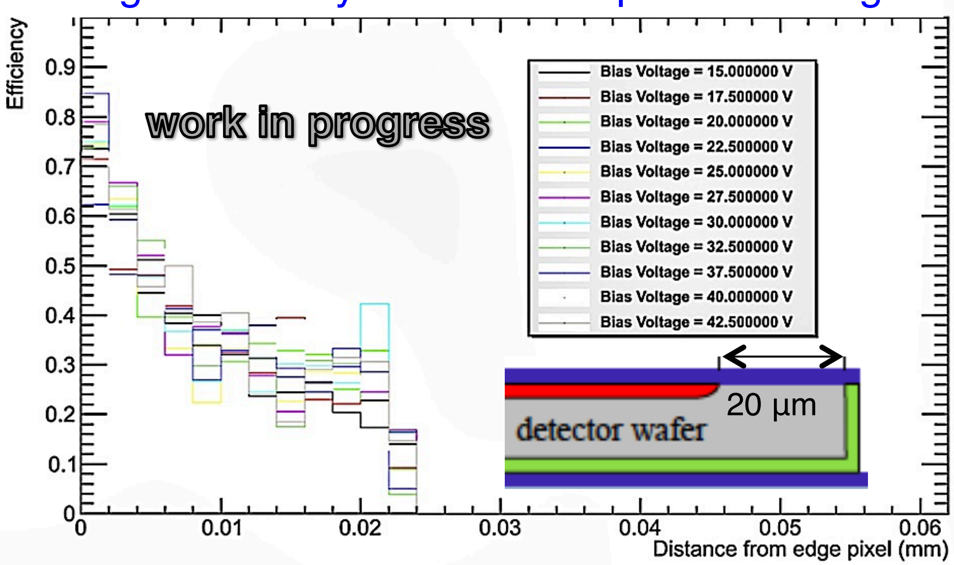
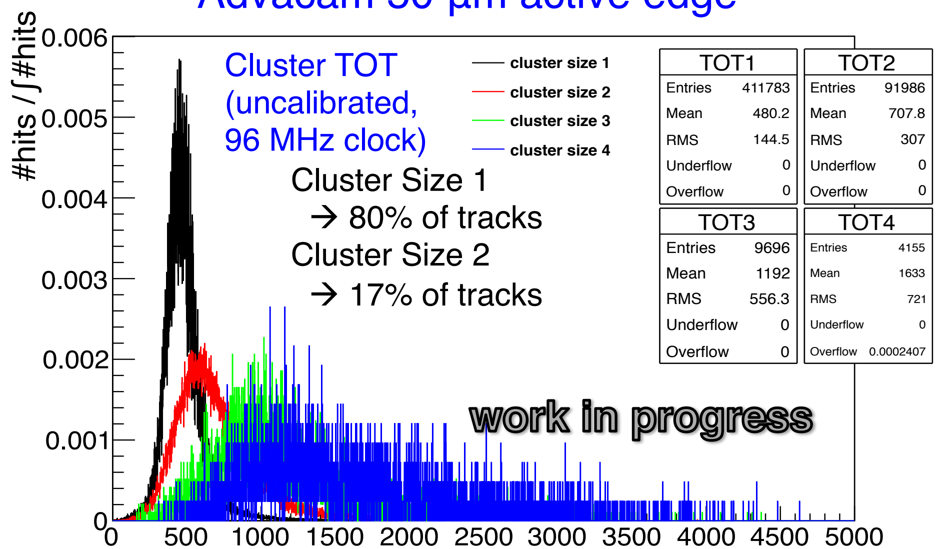
Edge efficiency Advacam 20 µm active edge



Advacam 50 µm active edge



Charge sharing: track position inside pixels

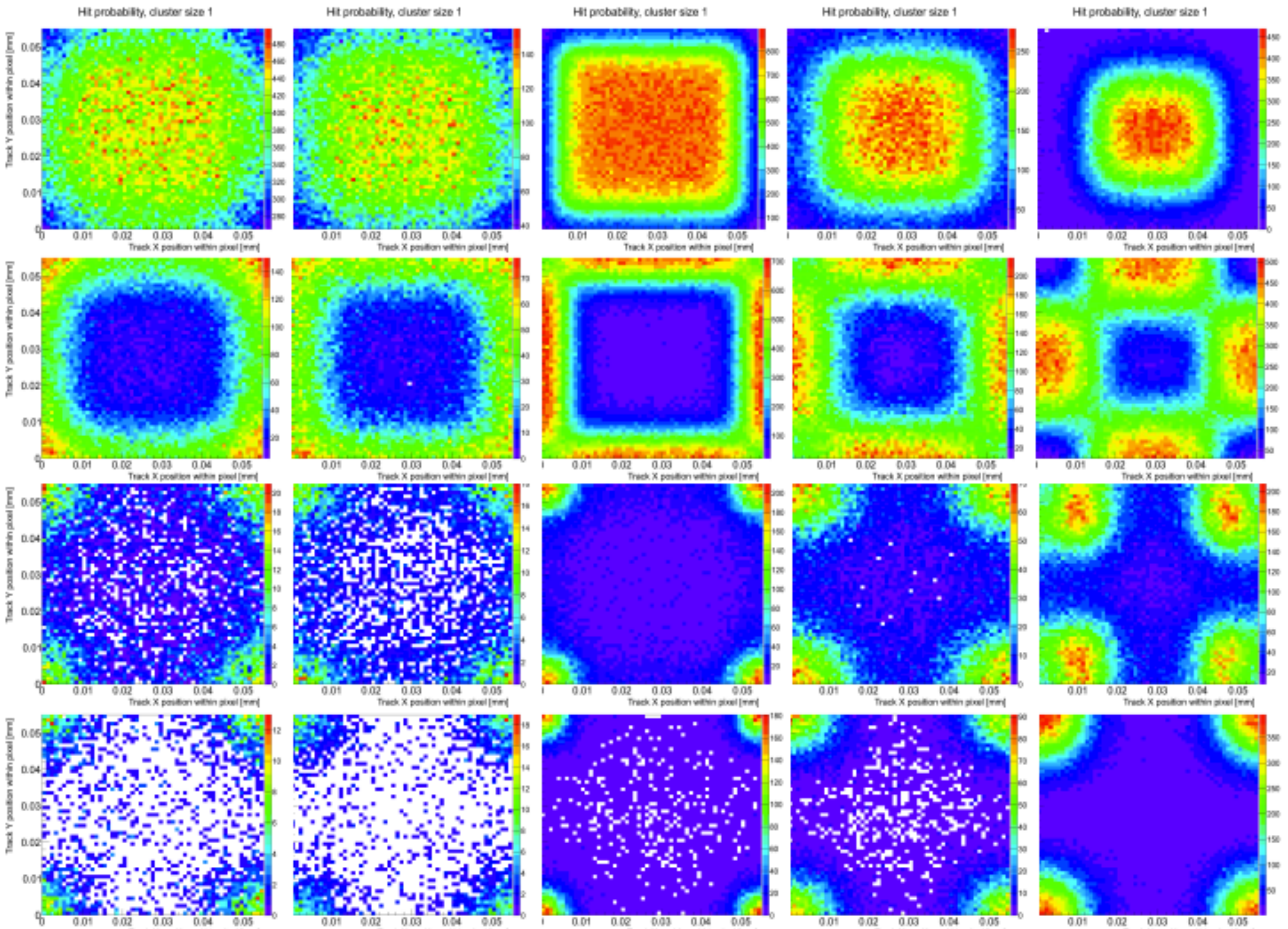
Thickness: 50 um 100um 150um 200um 500um

Cluster size 1

Cluster size 2

Cluster size 3

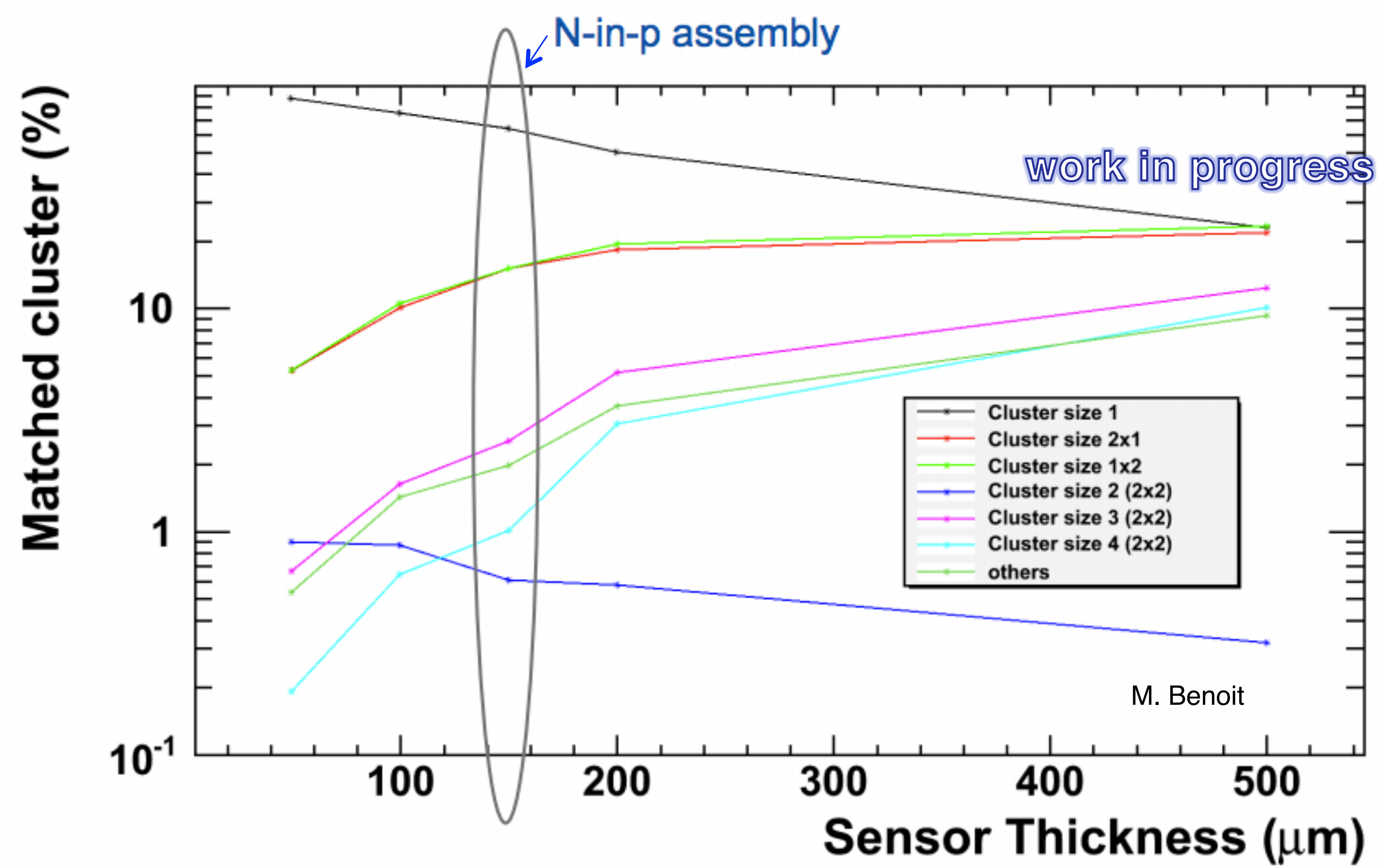
Cluster size 4



work in progress

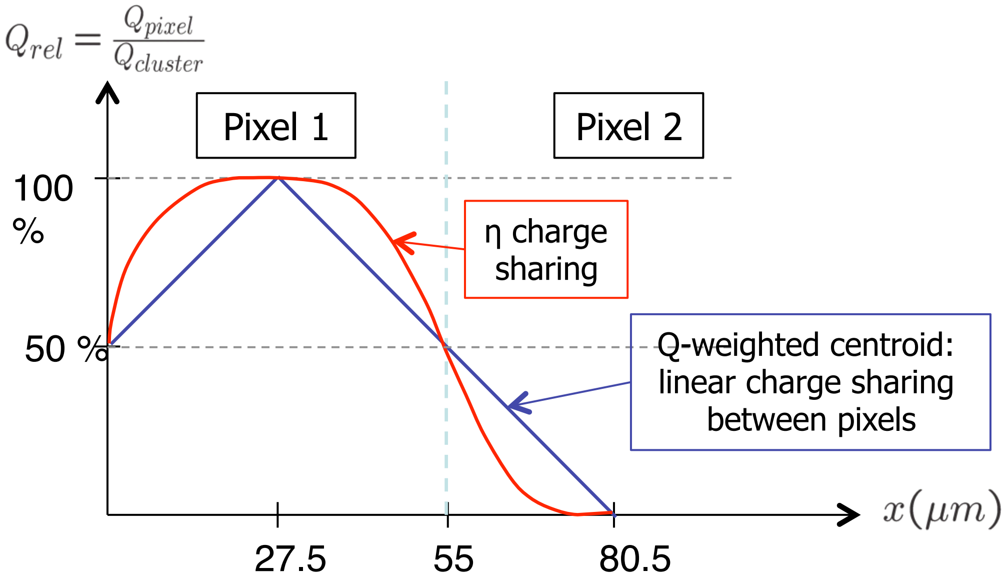
M. Benoit

Cluster size: dependence on thickness



- more multi-hit clusters for thicker sensors
- can use results to extrapolate to final CLIC sensors (25 μm pitch, 50 μm thickness)

Charge sharing: η correction



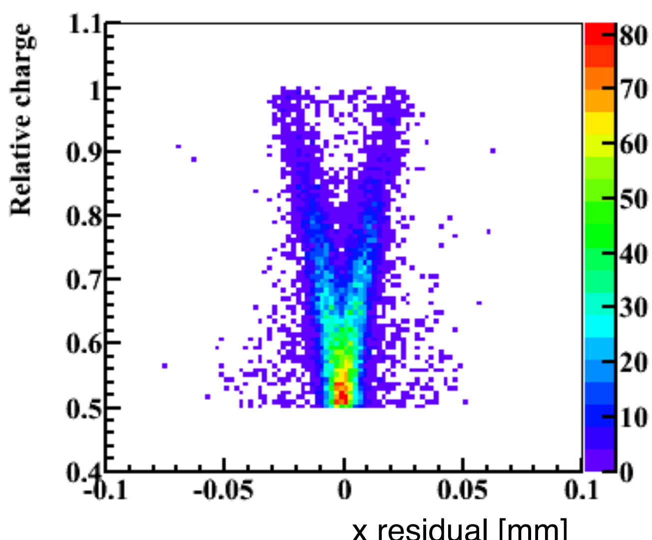
- Non linear charge sharing between pixels, parameterized by η function:

$$\eta(x) = Q_{cluster} \times \frac{erf(\frac{x}{\sigma})+1}{2} \qquad if\; x < pitchX/2$$

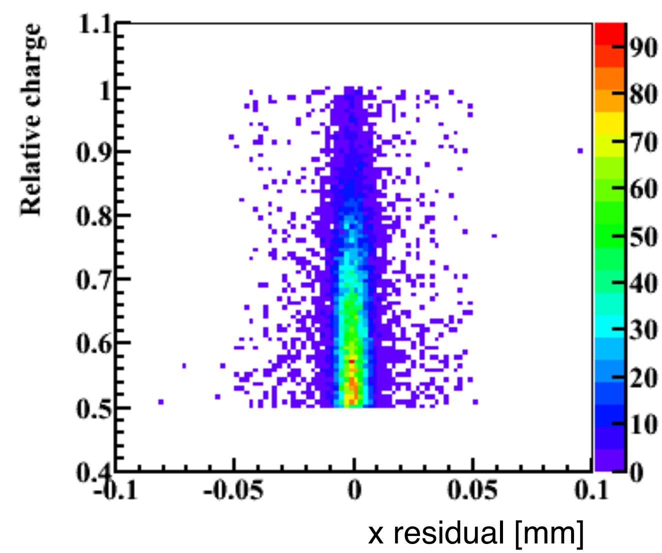
$$\eta(x) = Q_{cluster} \times \frac{erf(\frac{pitchX-x}{\sigma})+1}{2} \qquad if\; x > pitchX/2$$

- Single parameter σ describing diffusion of charge cloud in electric field
- Obtain σ from minimization of position resolution

Linear interpolation



η correction



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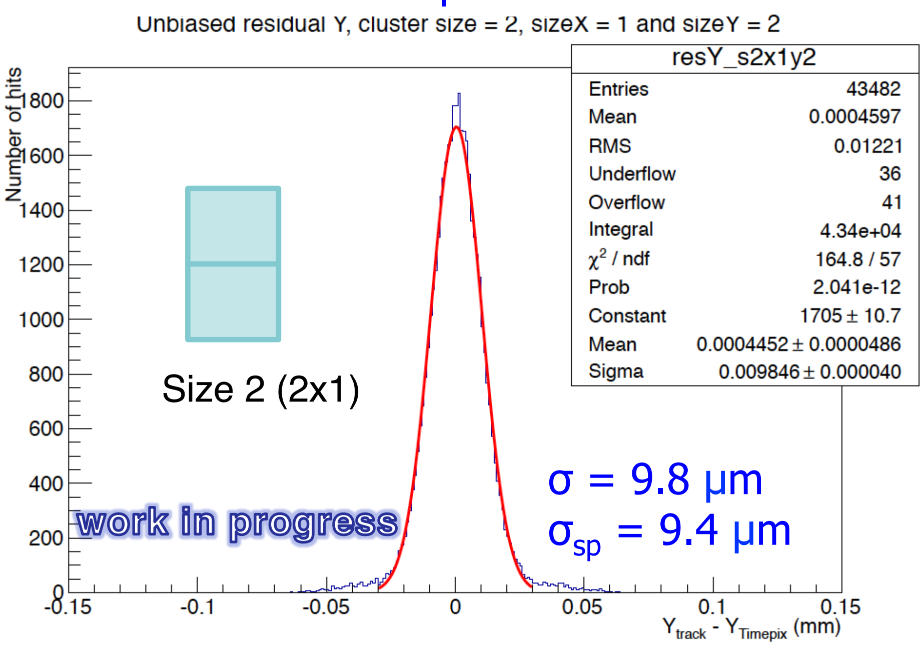
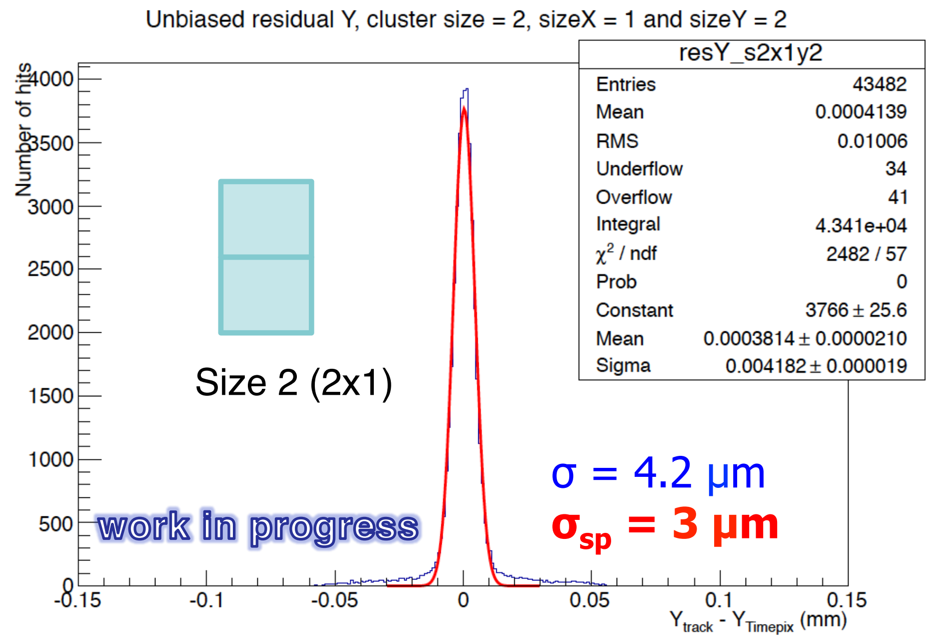
Resolution with eta correction

- Resolution for Advacam assembly (50 µm thick sensor, 20 µm active edge)
- Comparison linear interpolation / η correction
  for 2-hit clusters (17% of all tracks):
  σ_{SP}~9 µm for linear interpolation
  σ_{SP}~3 µm with η correction
- Note: selection bias of 2-hit clusters not unfolded

Linear interpolation



η correction



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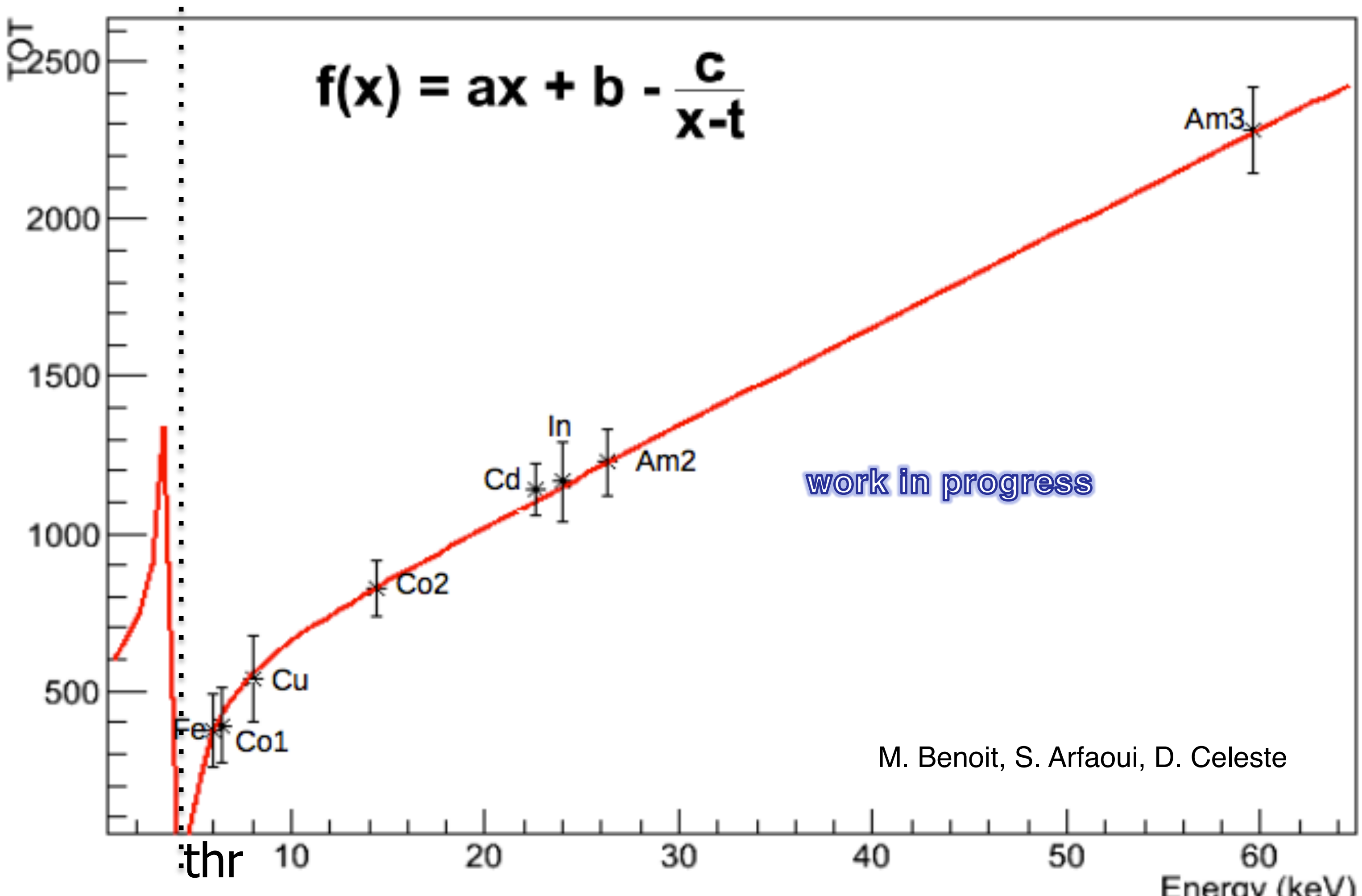
Timepix calibration

- Calibration of non-linear Timepix energy response with radioactive sources + fluorescence
- Parameterization with 4 parameters per pixel

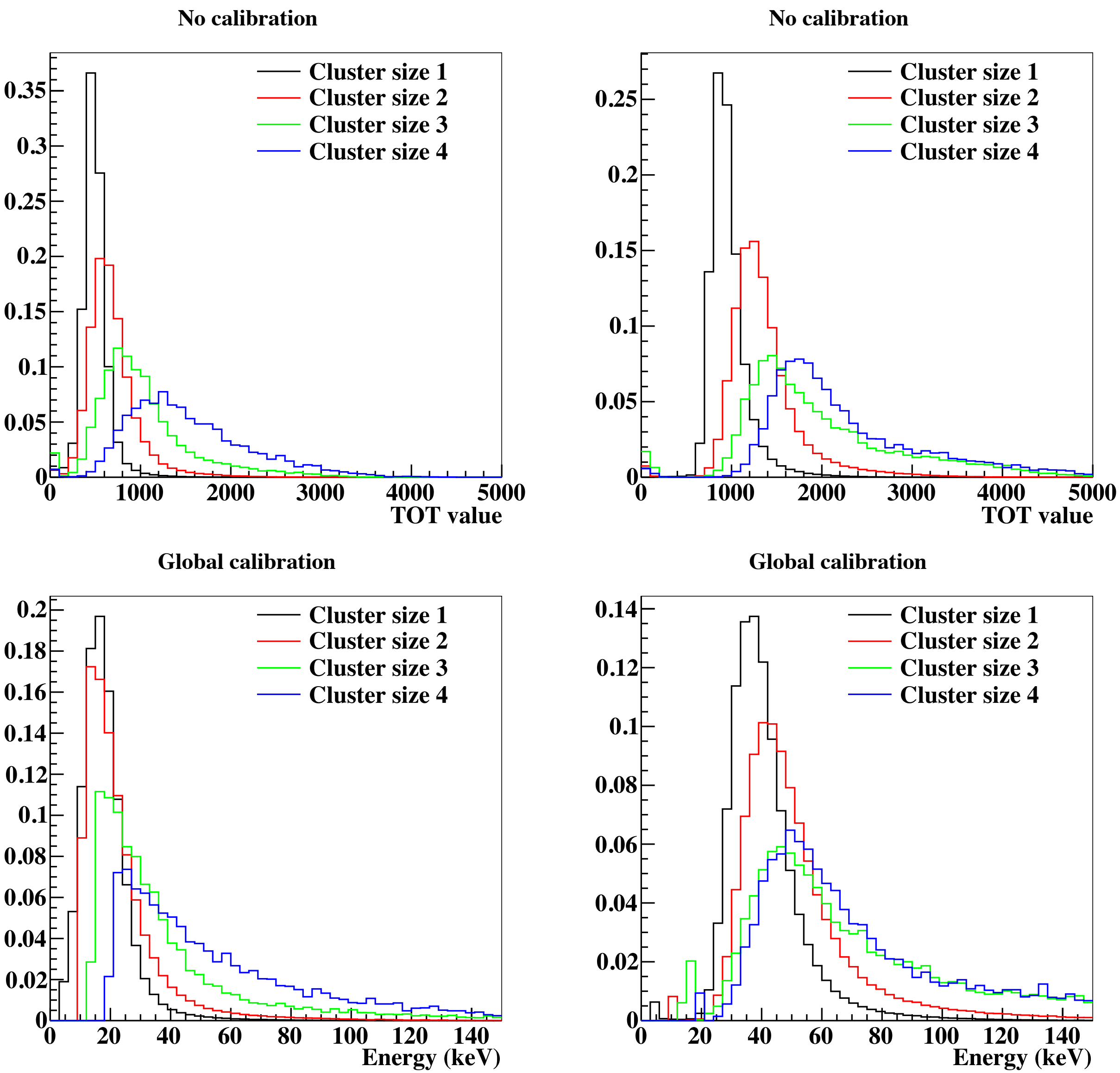
→ Improves accuracy of position determination with charge-weighting methods

Experimental TOT(E) for one pixel (« Surrogate function »)



Calibration applied to test-beam data

A06_W0110 50um thick   L04_W0125 100um thick

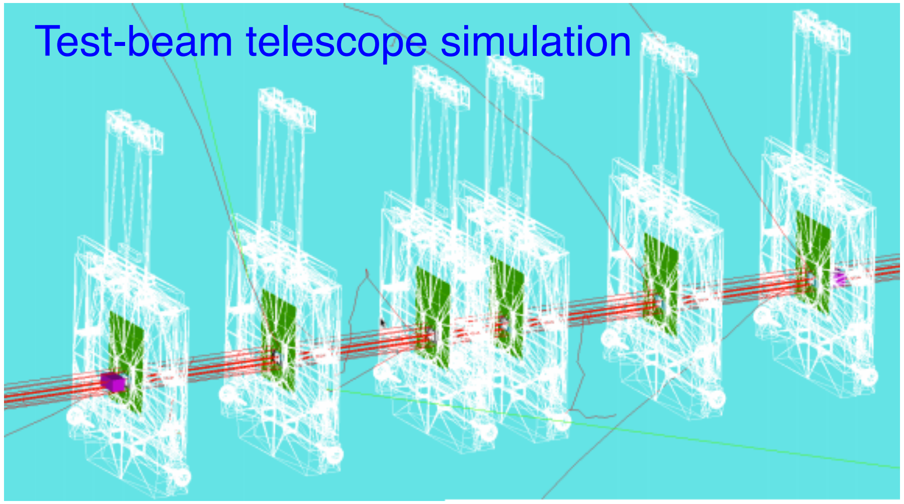


- apply global per-sensor calibration to TOT cluster-energy measurement in test-beam data
- as expected: improved agreement of energy measured for different cluster sizes
- remaining shift of peaks due to sub-threshold charge lost in neighboring pixels

S. Redford

Geant4 simulation

- ALLPix general purpose pixel detector simulation and digitisation framework
  - fully customizable geometry
  - used for simulation of test-beam and lab measurements (work in progress)
  - used as digitizer test bench for ATLAS and CLICdp
  - extrapolation of test-beam results to small-pitch pixels
  - interface to r/o simulation (SystemVerilog) under development → generate cluster topologies for benchmarking of readout ASIC architectures (RD53 project)



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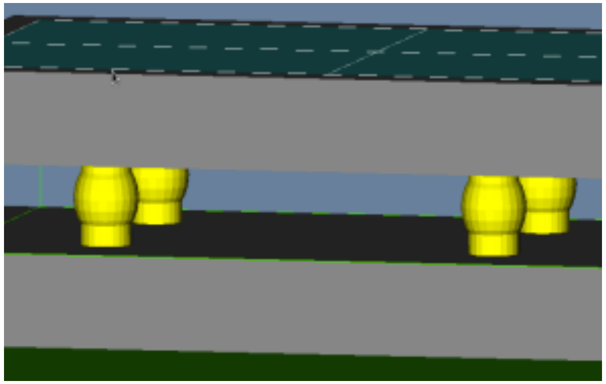
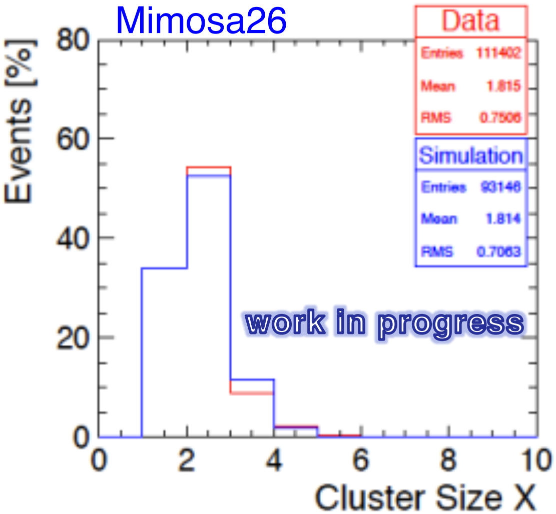
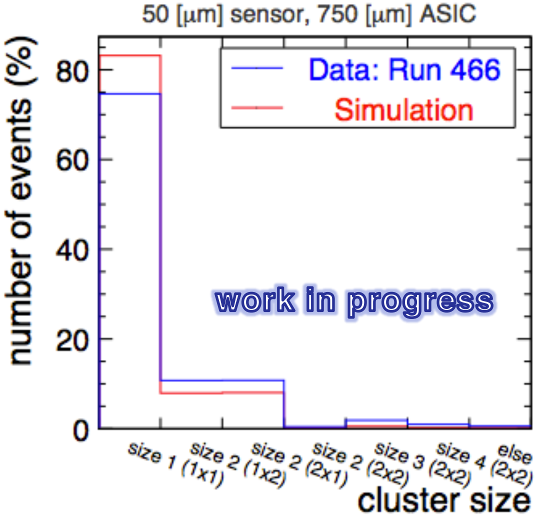
Hybrid assembly with bump bonds



Cluster-size distribution Mimosa26

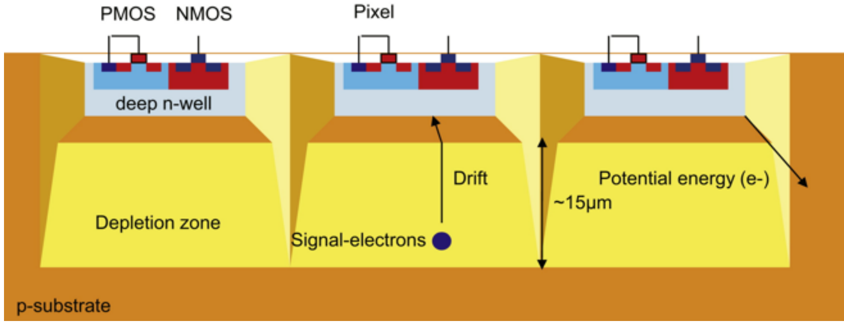


Cluster-size distribution DUT



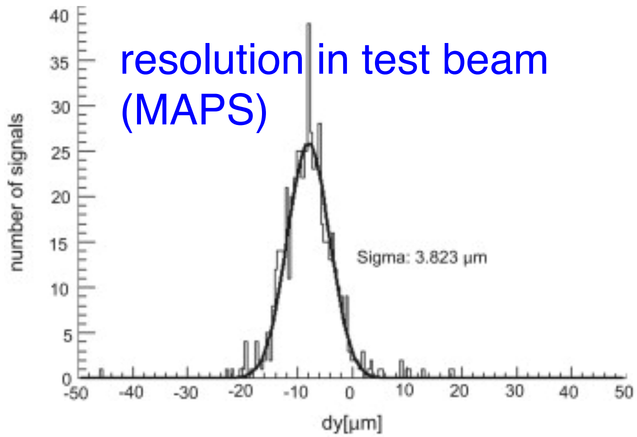
Integrated / hybrid technology: HV-CMOS

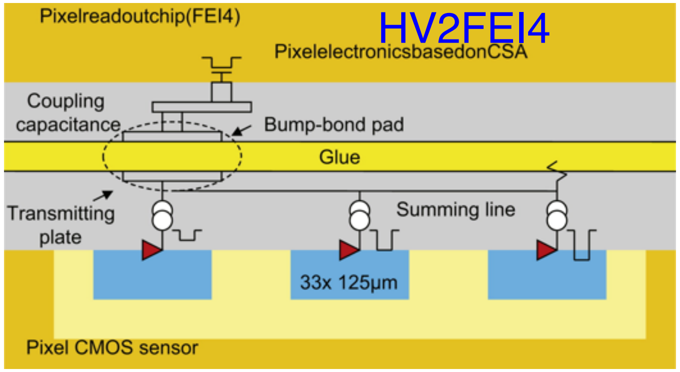
HV-CMOS MAPS:
- 180 nm High-Voltage CMOS process: Vbias~100 V → depletion layer ~10-20 µm
- integrated sensors with fast signal collection
- baseline technology for Mu3e at PSI

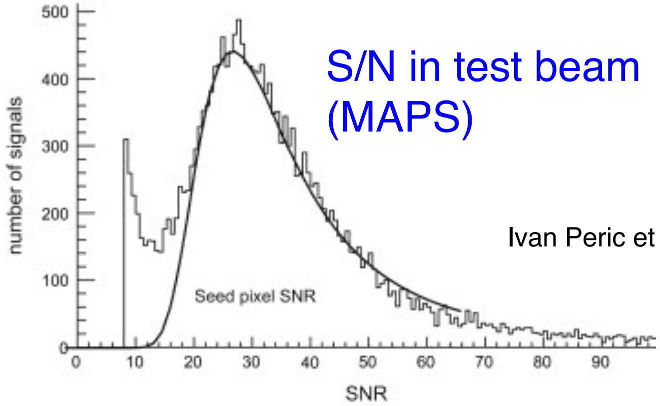


Hybrid option:

Capacitive Coupled Pixel Detector (CCPD)
- HV-CMOS chip as integrated sensor+amplifier
- capacitive coupling from amplifier output to r/o chip through layer of glue → no bump bonding!
- test chip for ATLAS FEI4 and Timepix produced
- proof of principle measurements







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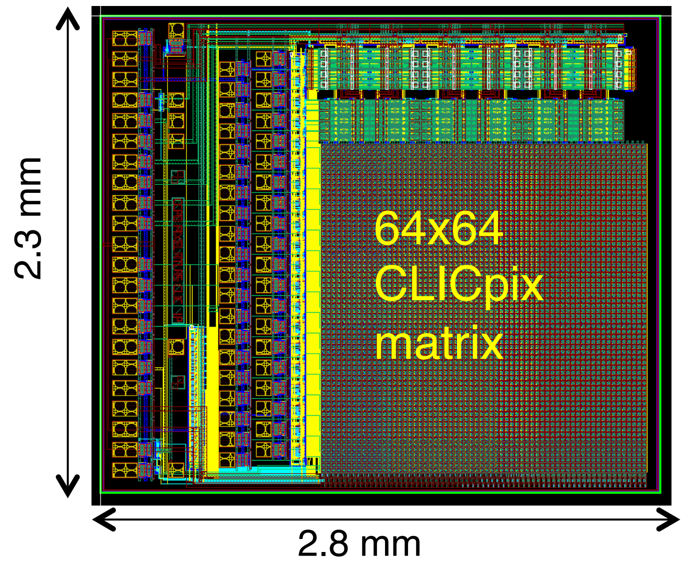
Heidelberg, CERN, CPPM, Bonn, Geneva, Glasgow

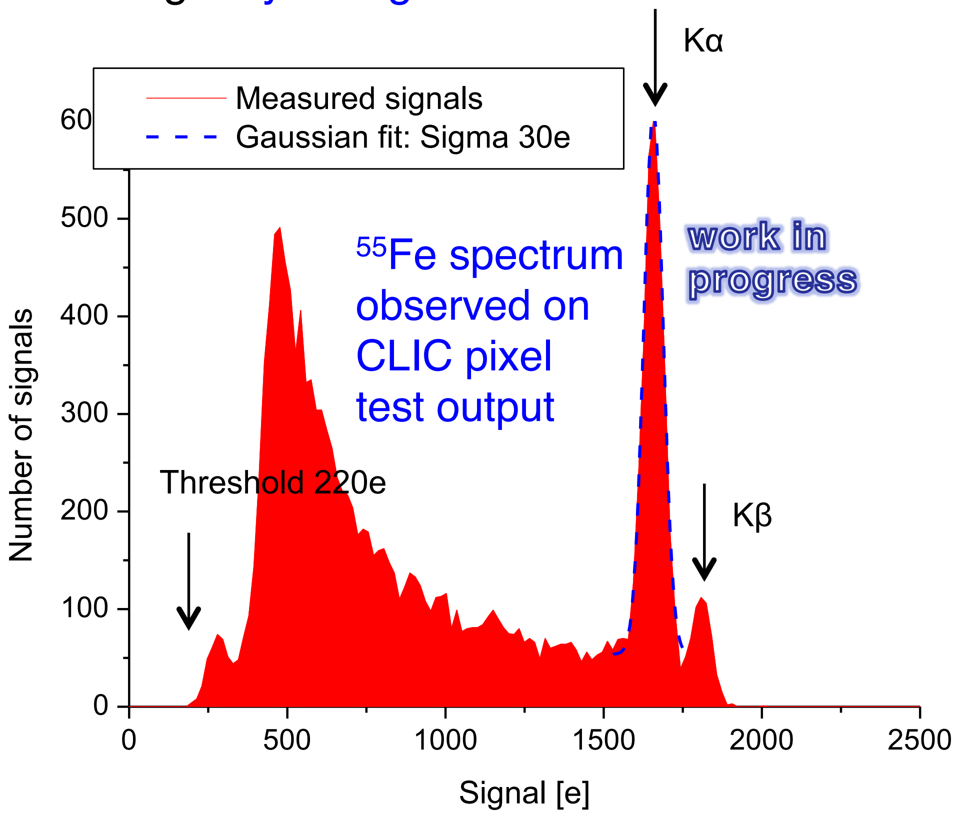
HV-CMOS active sensor with capacitive coupling

HV-CMOS active sensor with capacitive coupling

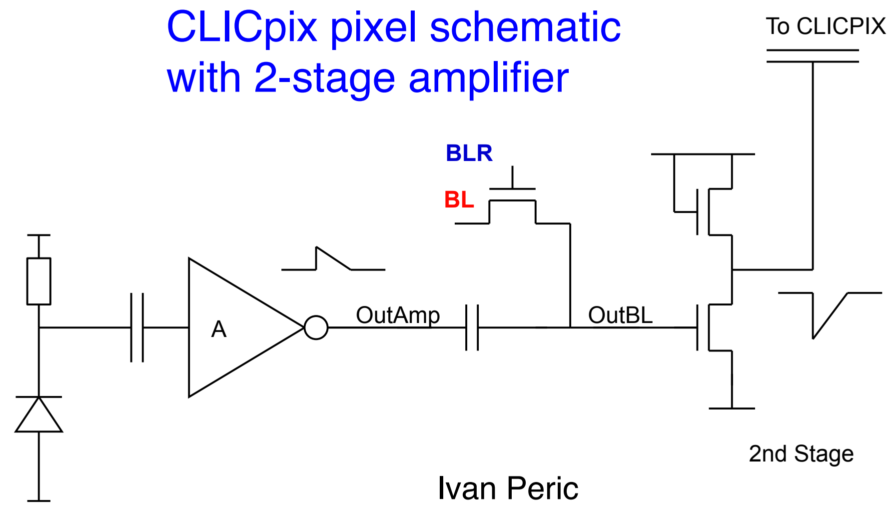
- combined prototype for ATLAS (FEI4) and CLIC
- AMS H18 180 nm HV process
- CLICpix 64x64 matrix (25 µm pitch)
- first tests with ^{55}Fe source: chip functional, good S/N
- assemblies with CLICpix ASIC are in production: test feasibility of low-mass low-cost AC interconnect through layer of glue

CCPDV3





CLICpix pixel schematic with 2-stage amplifier



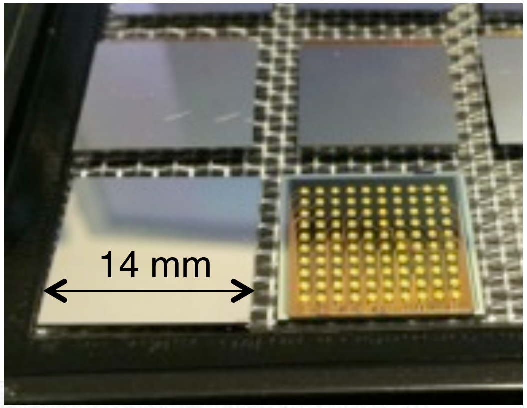
Ivan Peric

Through-Silicon Vias (TSV)

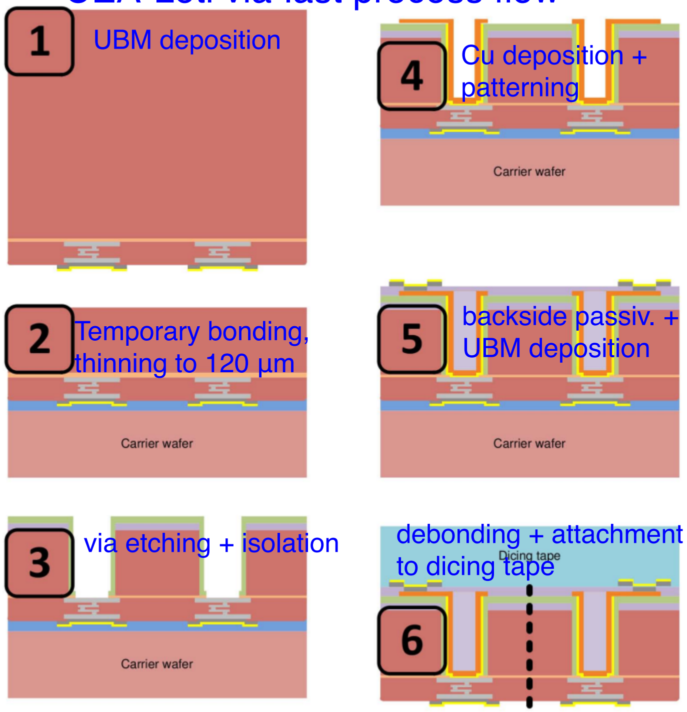
Through Silicon Via (TSV): vertical electrical connection passing through Si wafer
→ eliminates need for wirebonds
→ 4-side buttable chips
→ increased reliability, reduced material budget

Example: Medipix TSV project (ALICE, CLIC, ACEOLE and AIDA) with CEA-Leti and Advacam

- 130 nm Medipix(RX) wafers, via-last process
- successful completion of first phase: demonstrate feasibility
- on-going second phase: demonstrate good yield
- launched third phase: TSV with Timepix3 50 µm thickness

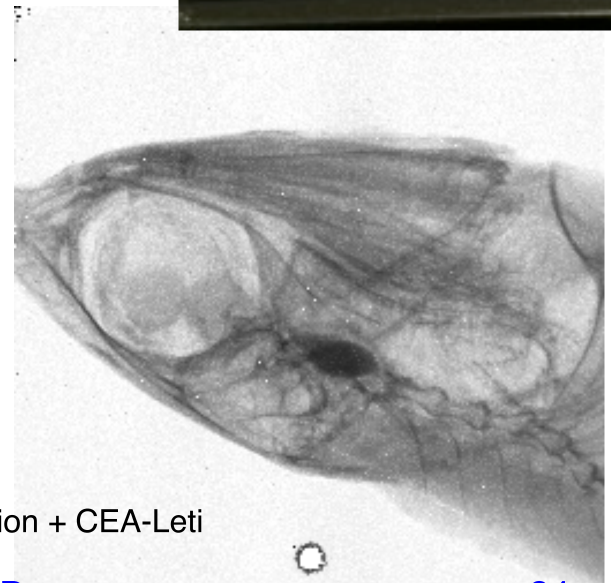


CEA-Leti via-last process flow



- 60 µm TSV diameter
- wafers thinned to 120 µm
- 5 µm copper layer for TSV

First Medipix3 Image taken with TSV assembly (fish head):



Medipix Collaboration + CEA-Leti

http://iopscience.iop.org/1748-0221/6/11/C11018/pdf/1748-0221_6_11_C11018.pdf

Summary and Conclusions

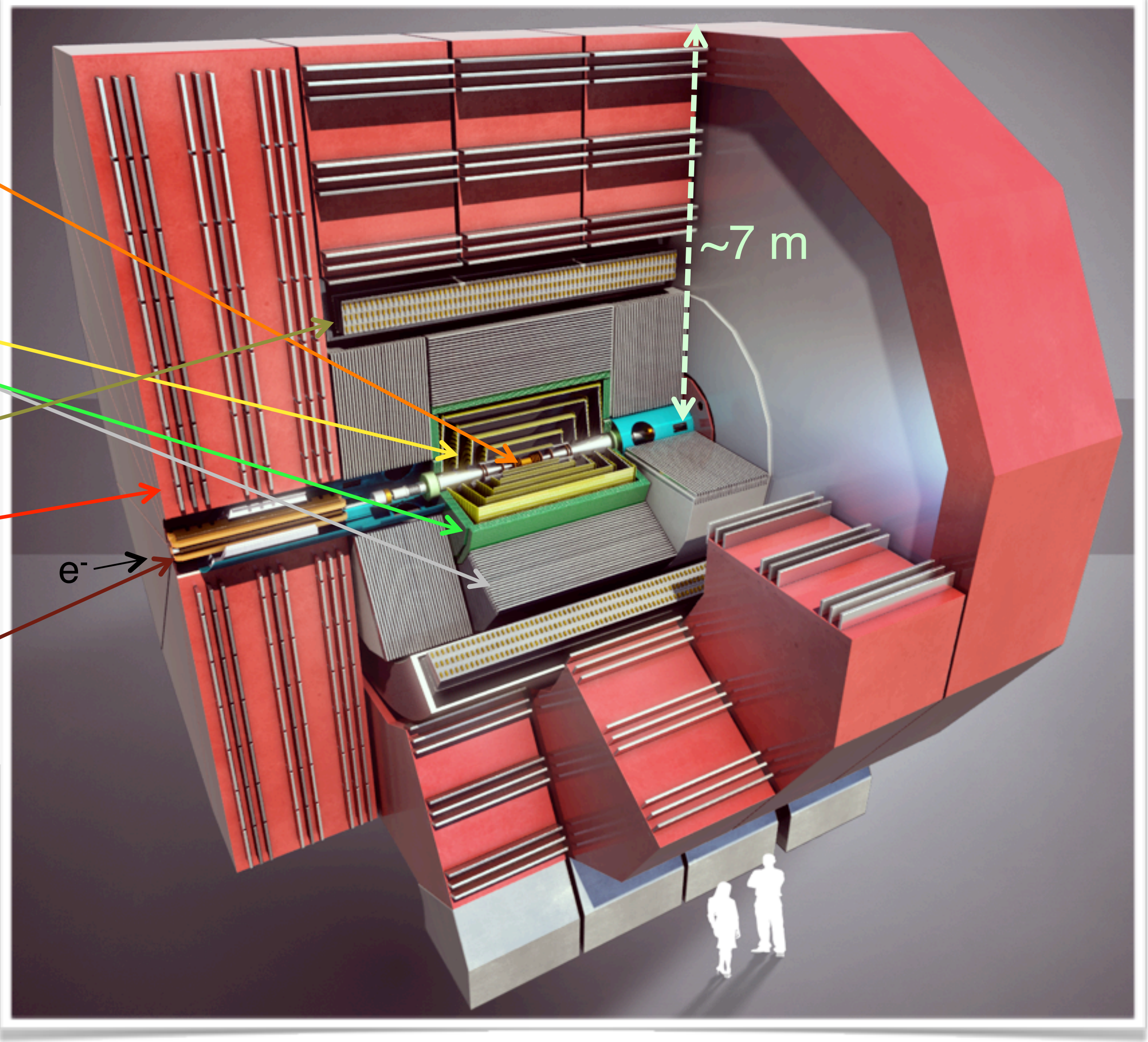
- Challenging requirements for CLIC vertex detector
  → focus on hybrid pixel concepts
- CLICpix prototype functional, sensor procurement in progress
- Good performance of thin Timepix assemblies in test beams
- New HV-CMOS prototype CCPDV3, assemblies in production
- Progress with TSV assemblies

Thanks to everyone who provided material for this talk!

Additional material

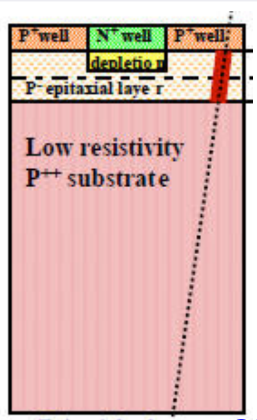
CLIC detector concept

- low-mass **vertex detector** with ~25x25 µm² pixels
- **silicon tracker**
- fine-grained **PFA calorimetry**, 1+7.5 Λ_i
- 4-5 T **solenoid**
- **return yoke** with muon ID
- complex **forward region** with final beam focussing

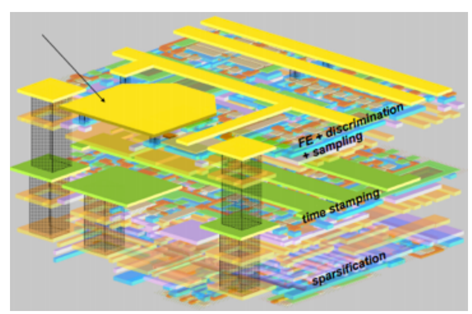


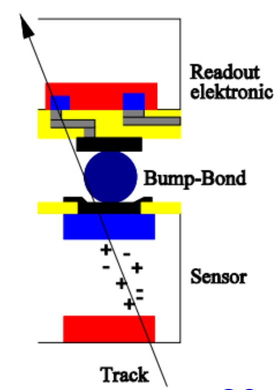
Pixel-detector technologies

	Monolithic	3D-integrated	Hybrid
Examples	FPCCD, MAPS, HV-CMOS	SOI, MIT-LL, Tezzaron, Ziptronix	Timepix3/CLICpix
Technology	Specialised HEP processes, r/o and sensors integrated	Customized niche industry processes, high density interconnects btw. tiers	Industry standard processes for readout; depleted high-res. planar or 3D sensors
Interconnect	Not needed	SLID, Micro bump bonding, Cu pillars	
granularity	down to 5 µm pixel size		~25 µm pixel size
Material budget	~50 µm total thickness achieveable		~50 µm sensor + ~50 µm r/o
Depletion layer	partial	partial or full	full → large+fast signals
timing	Coarse (integrating sensor)	Coarse or fast, depending on implementation	Fast sparsified readout, ~ns time slicing possible
R&D examples	ILC, ALICE, RHIC	ILC, HL-LHC	CLIC, ATLAS-IBL, HL-LHC



Epitaxial substrate

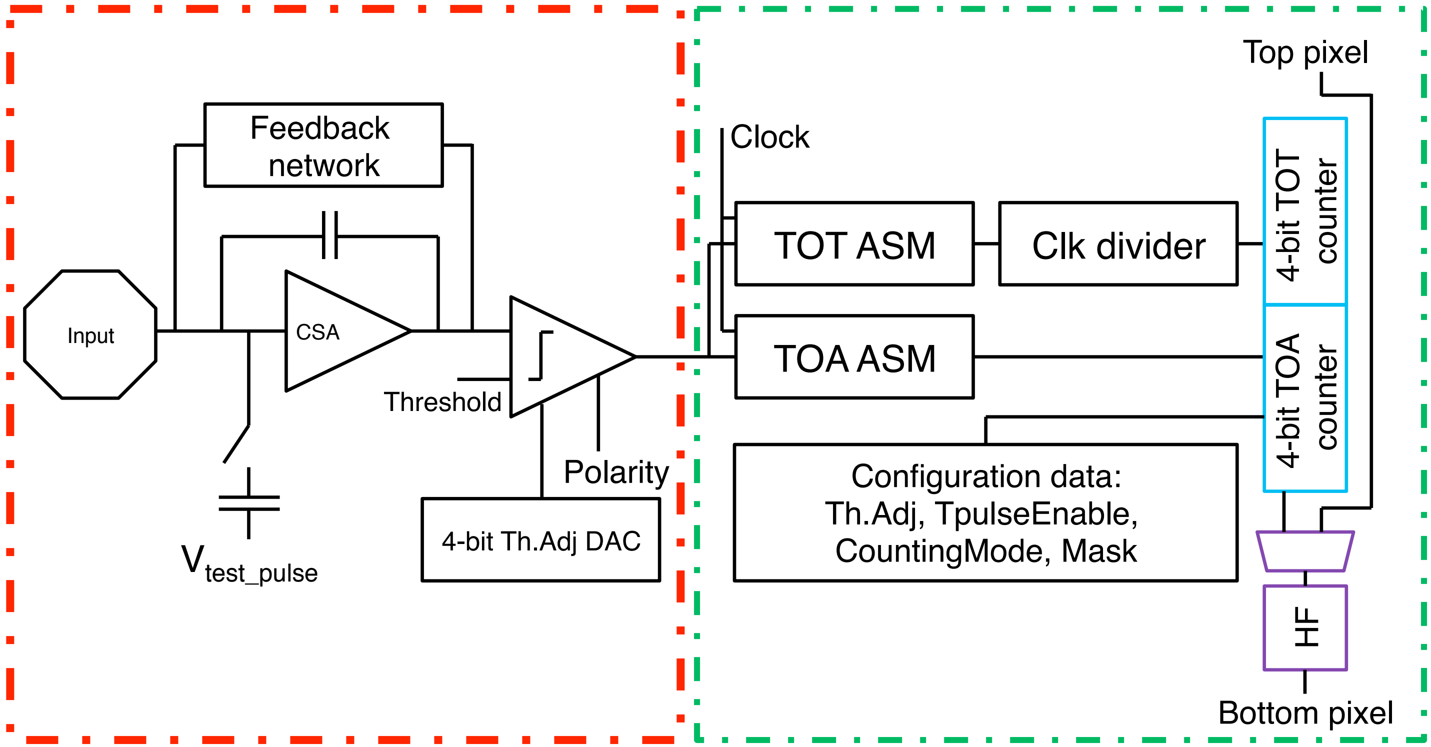




LC pixel R&D examples

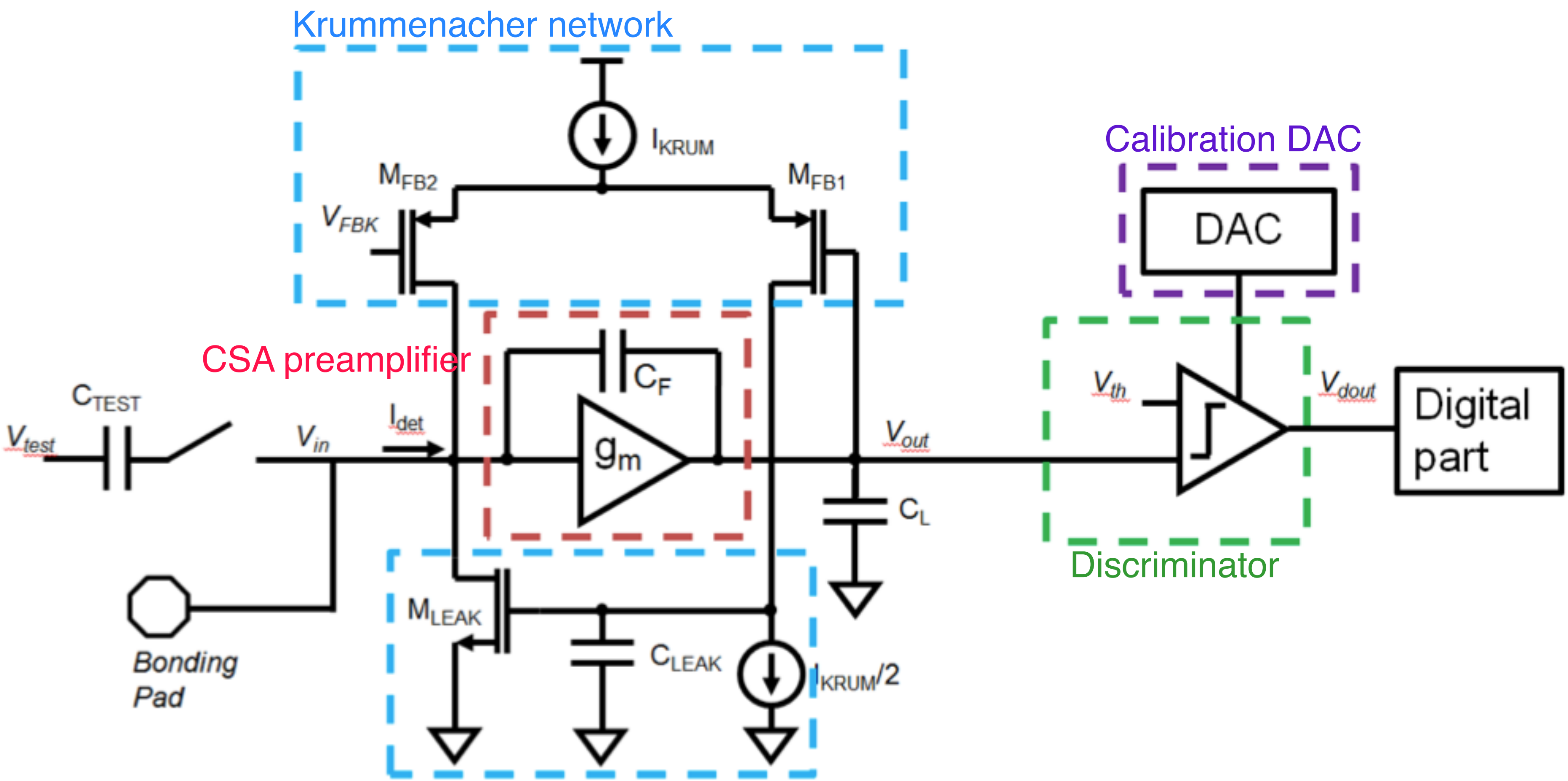
Project	Technology	Target experiments	Groups
Mimosa	**fully integrated** CMOS MAPS Tower Jazz 0.18 um	ALICE, CBM, BES-3, ILD@ILC	IPHC Strasbourg
Arachnid / Cherwell		generic vtx / tracking / calo, ALICE ITS	Bristol, Birmingham, Queen Mary, RAL, Daresbury
Chronopix	**fully integrated** CMOS MAPS IBM 90 nm	SiD@ILC	Oregon
FPCCD	**integrated sensor**, separate r/o, Hamamatsu CCDs	ILD@ILC	KEK, Tohoku
DEPFET	**integrated sensor**, separate readout, MPG-HLL DEPFET	Belle II, ILD@ILC	Bonn, MPI Munich, Barcelona, Santander, others
VIP2b / SDR / MAMBO4	**3d integrated / SOI** Tezzaron + STM 130 nm, MIT LL	generic technology tests, Super-Belle, SiD@ILC	FNAL, KEK, OKI, INFN, others
HV-CMOS CCPD	**active sensor**, 180 nm CMOS	HL-ATLAS, CLIC	Heidelberg, CERN, CPPM, Bonn, Geneva
CLICpix	**hybrid r/o**, 65 nm CMOS	CLIC, SiD@ILC	CERN

CLICpix pixel architecture

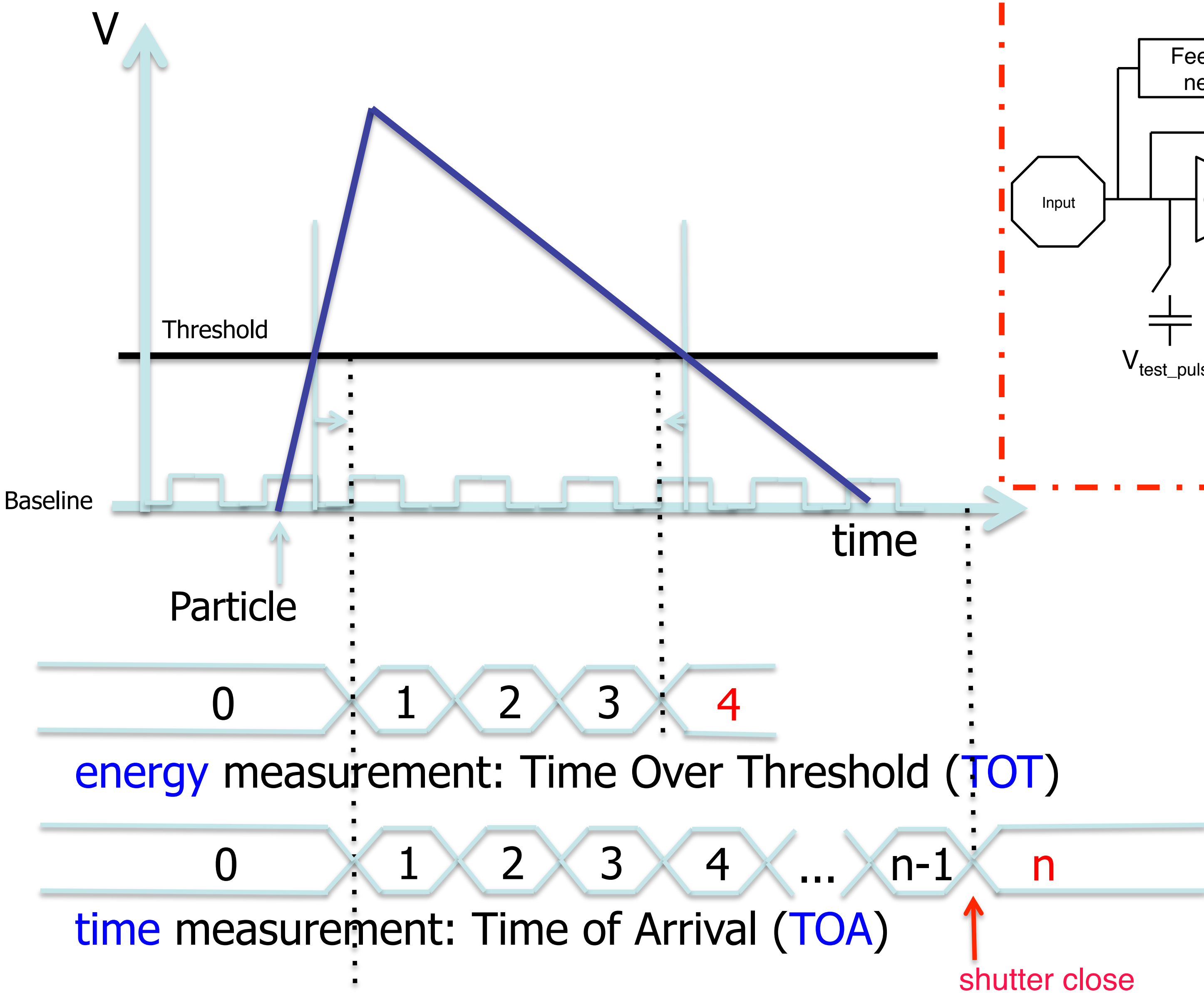


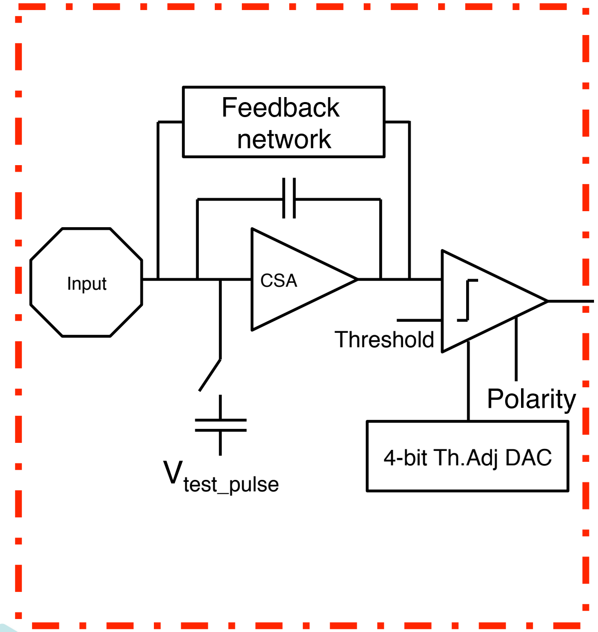
- The analog front-end shapes photocurrent pulses and compares them to a fixed (configurable) threshold
- Selectable polarity (positive / negative signals)
- Digital circuits simultaneously measure Time-over-Threshold and Time-of-Arrival of events and allow for zero-compressed readout

CLICpix analog frontend



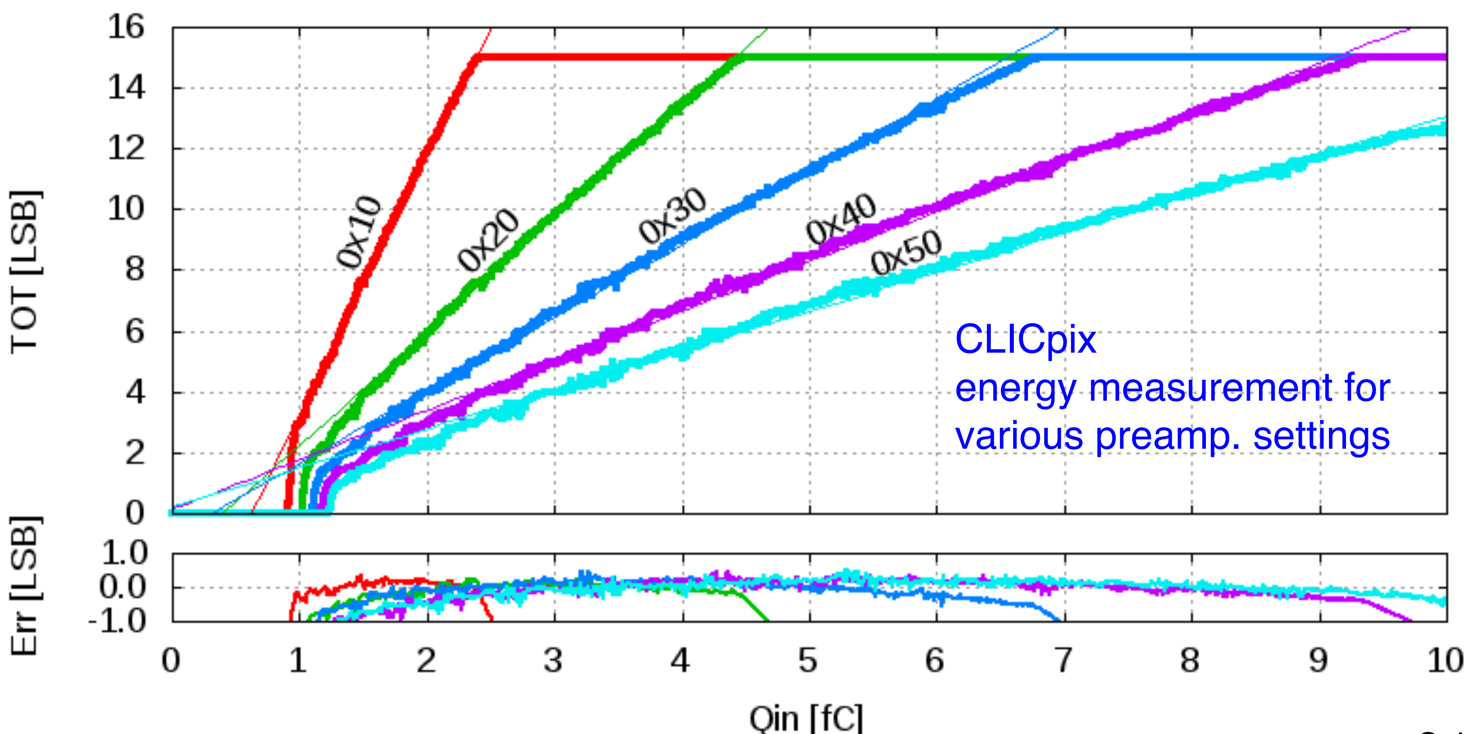
CLICpix: time and energy measurement





CLICpix: energy measurement

- Measure charge released in each pixel
  → Improve position resolution through interpolation
- Time-Over-Threshold (TOT) measurement (4-bit precision)
- Calibration measurement using external test pulser:

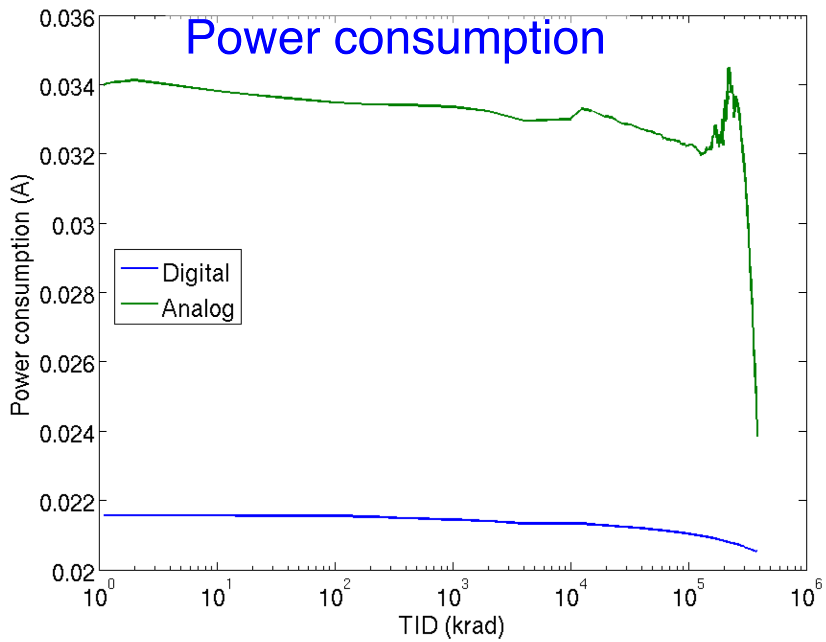


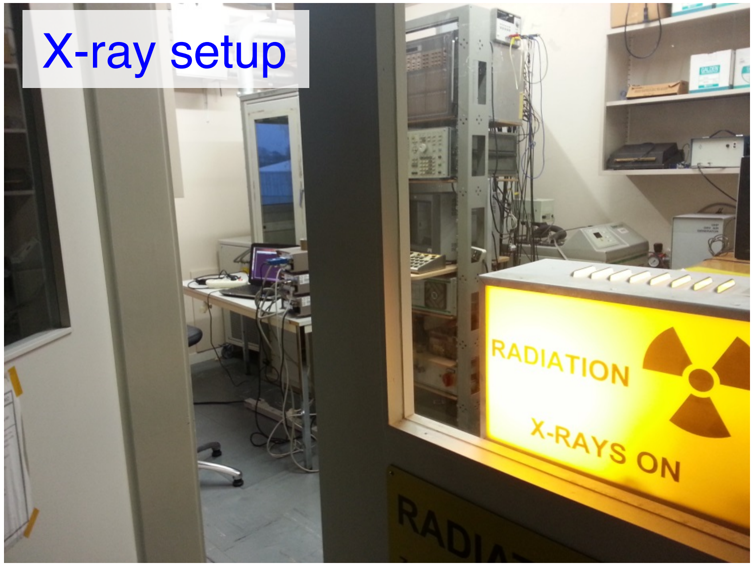
S. Kulis, P. Valerio

CLICpix: radiation qualification

- Moderate radiation-tolerance requirements at CLIC: <100 kRad TID
- However: building blocks can be re-used for RD53 (~1 GRad required)
- Results of radiation testing useful for gaining deeper understanding of the chip

→ performed radiation test up to 1 GRad (up to 150 kRad/minute) in calibrated X-ray setup





- No significant changes observed in sub-MRad range relevant for CLIC
- For >250 MRad: PMOS switches in current mirror fail

→ Break-down of analog power (note: band gap foreseen for final chip, instead of current mirror)

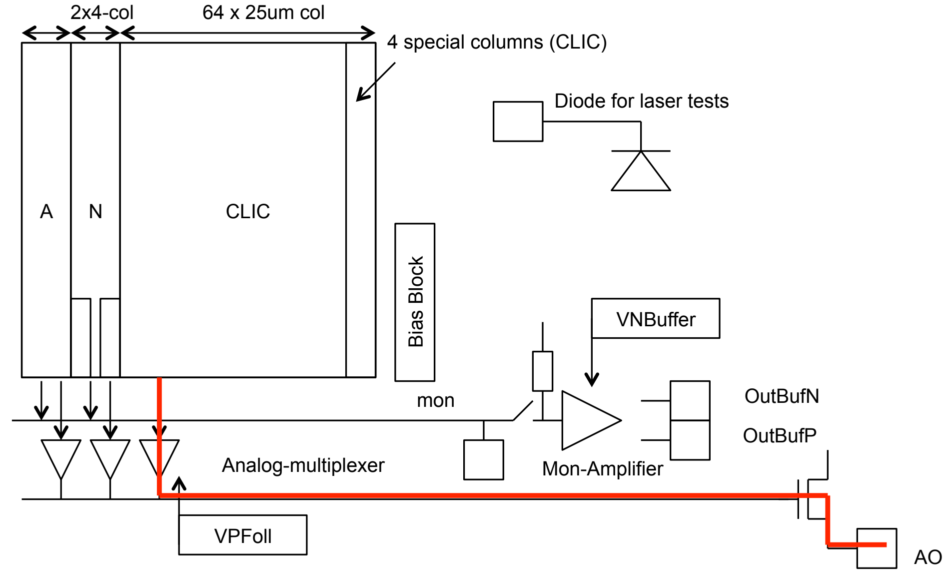
- digital components kept working normally

S. Kulis, P. Valerio

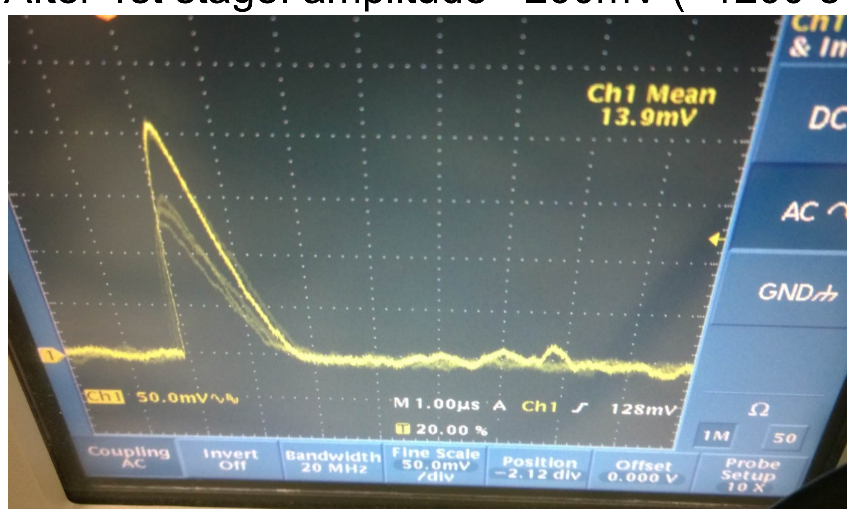
CCPDV3: first tests

- Measured signal at test output for 1st and 2nd amplification stage
- X-rays froms ^{55}Fe source
- V_{bias}=30 V
- no baseline adjustment performed
- chip is functional, signal as expected

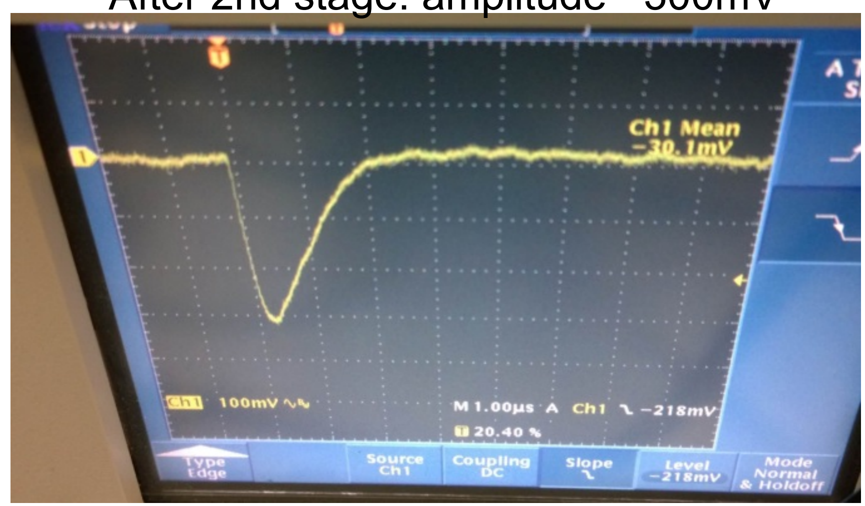
- Assemblies with CCPDV3 glued to CLICpix and corresponding test board are in production



After 1st stage: amplitude ~200mV (~1200 e-)

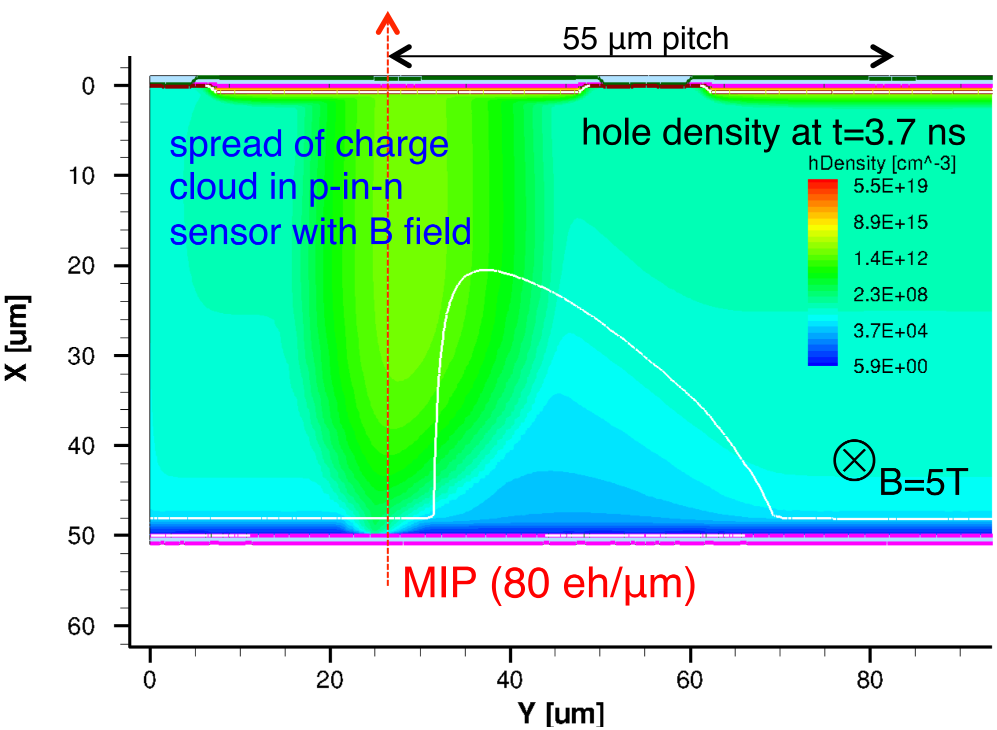


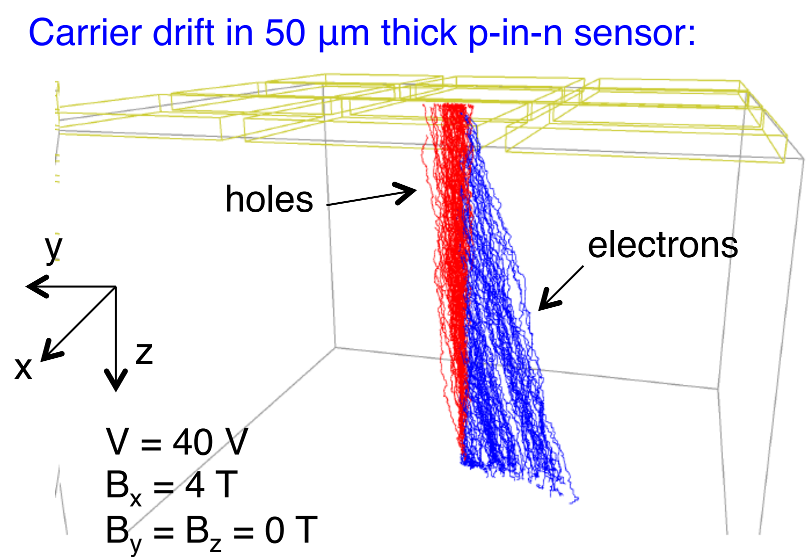
After 2nd stage: amplitude ~300mV



Silicon simulations

- TCAD and MC simulations of charge propagation in silicon sensors
  → effect of sensor layout and material
  → effect of E and B fields (Lorentz angle)
  → comparison with lab and test-beam measurements
  → tuning of digitization models for full-detector simulation





M. Benoit, N.A. Tehrani

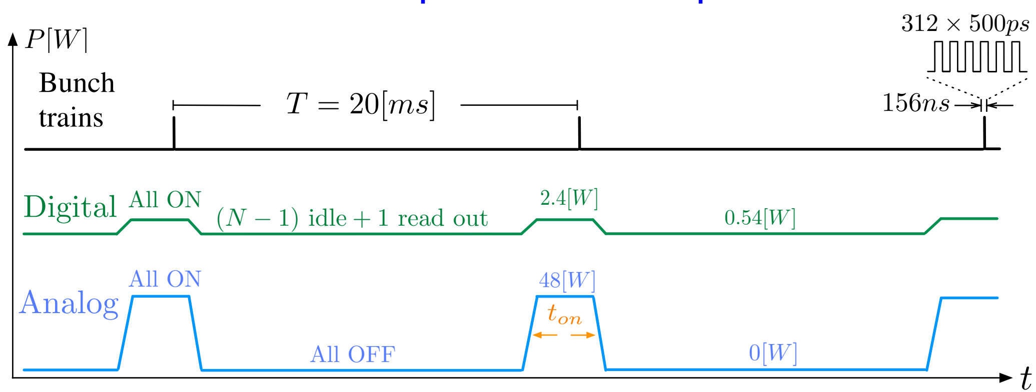
CLICpix power-pulsing + delivery requirements

Small duty cycle of CLIC machine allows for power reduction of readout electronics: turn off front end in gaps between bunch trains

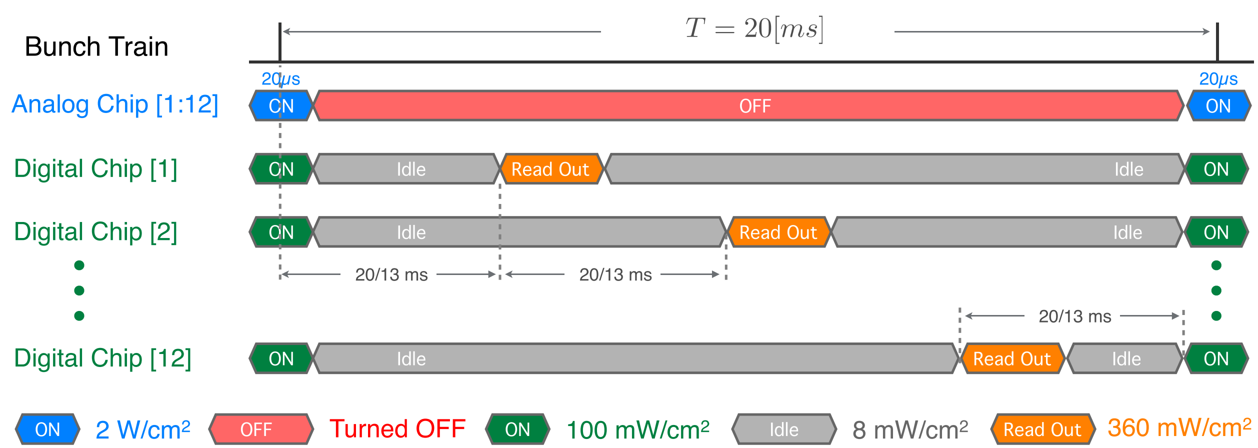
Challenging requirements:

- Power budget **<50 mW/cm²** average (air-flow cooling limit)
- High peak current **> 40A/ladder**
- Different timing **analog/digital** electronics
- High magnetic field **4-5 T**
- Material budget **< 0.1% X_0** for services+supports
- Regulation **< 5% (60 mV)** for analog part

Vertex-detector power consumption



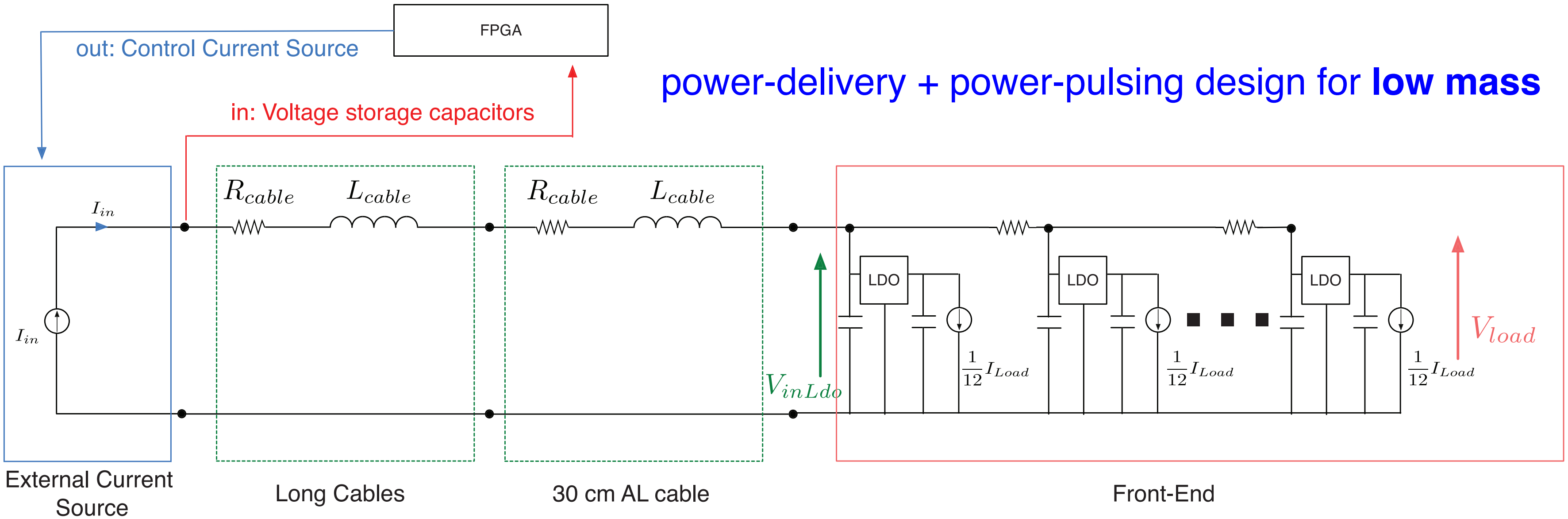
CLICpix powering states



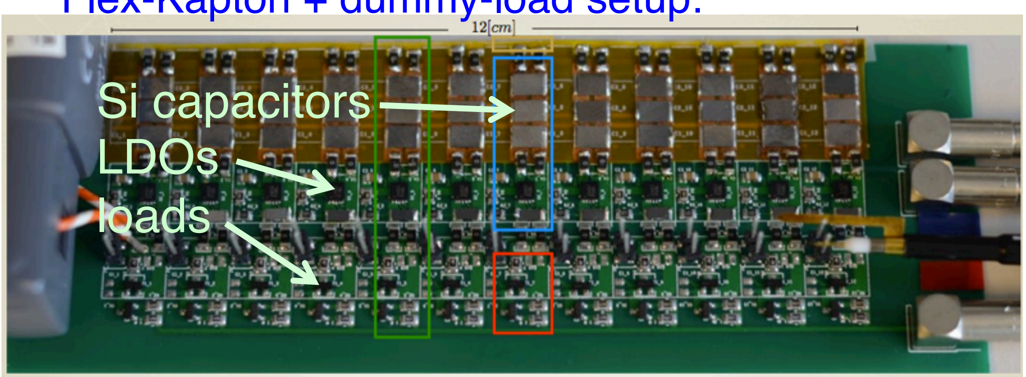
C. Fuentes, X. Llopart, P. Valerio

CLICpix power-pulsing + delivery concept

power-delivery + power-pulsing design for **low mass**



Flex-Kapton + dummy-load setup:

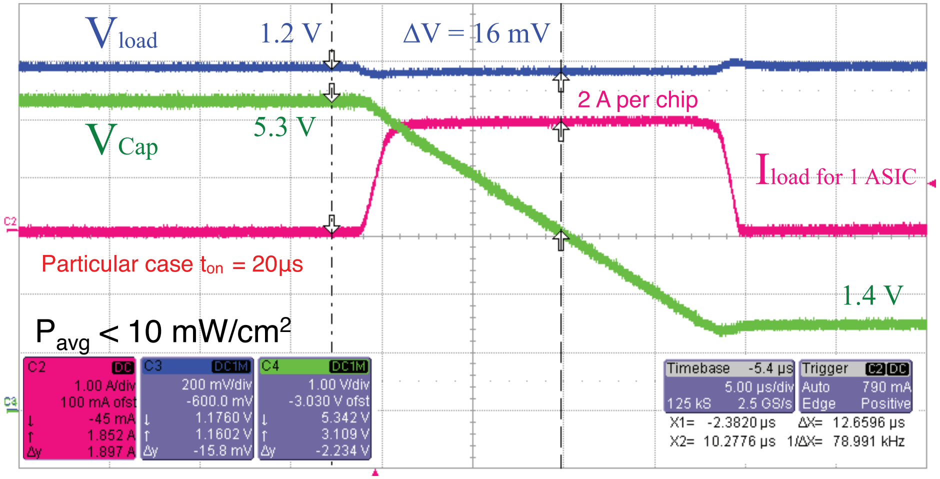


- Power pulsing with local energy storage in Si capacitors and voltage regulation with Low-Dropout Regulators (LDO)
- FPGA-controlled current source provides small continuous current
- Low-mass Al-Kapton cables
- Prototypes for analog + digital powering of CLICpix ladder

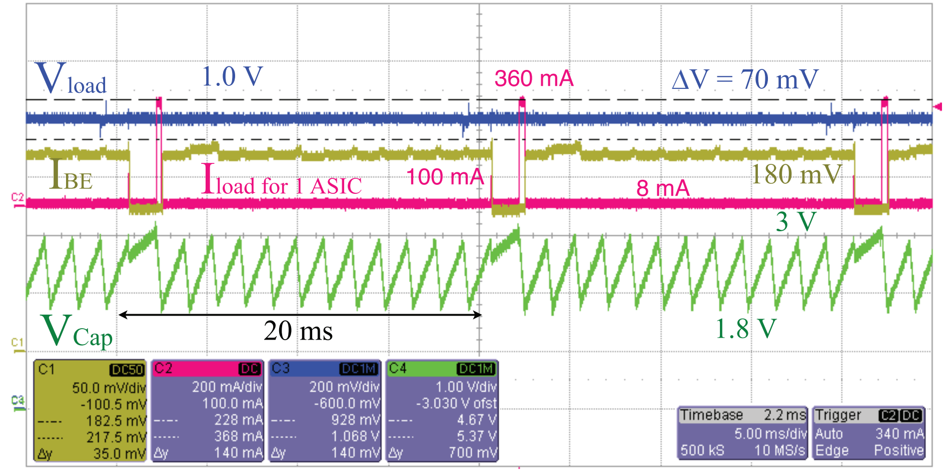
C. Fuentes

CLICpix power-pulsing + delivery results

analog power

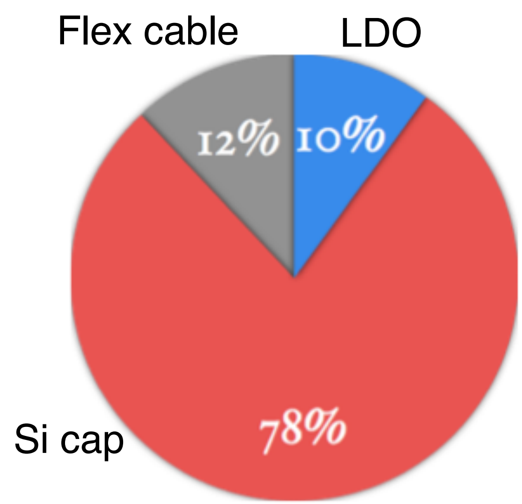


digital power



- Measurements on prototypes for digital and analog powering of ladders:
  - I_{ladder}<300 mA; P<45 mW/cm²
  - Voltage stability: ΔV~16 mV (analog), ~70 mV (digital)
  - ~0.1% X_0 material contribution, dominated by Si capacitors
  - Can be reduced to ~0.04% X_0 with evolving Si capacitor technology: 25 µF/cm² → 100 µF/cm²

material budget



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X/X0~0.104%