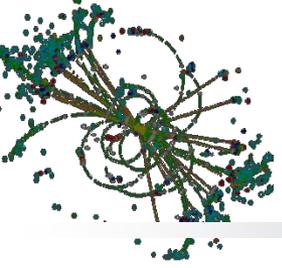


Chronopixel R&D status – May 2014

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University of Oregon, Eugene

In collaboration with J.E.Brau, D.M.Strom (University of Oregon, Eugene, OR), C.Baltay, W.Emmet, D.Rabinovitz (Yale University, New Haven, CT)

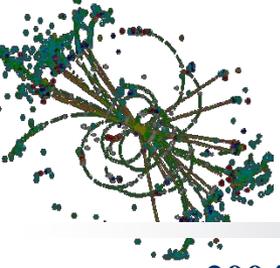
EE work is contracted to Sarnoff Corporation



Outline of the talk



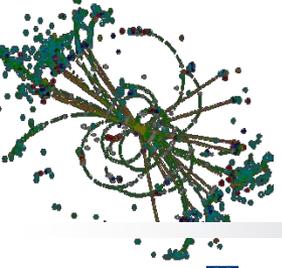
- Very brief reminder of Chronopixel concept:
 - ↳ **Chronopixel** is a **monolithic CMOS** pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and **record the time** (time stamp) **of each hit**.
- Project milestones.
- Summary of prototypes 1 and 2 tests.
- Changes in prototype 3
- Sensor options discussion
- Conclusions and plans
 - ↳ We **have learned** a lot from 2 prototypes, **solved many problems**, and have **very interesting** tests of prototype 3 coming **this summer**.



Timeline



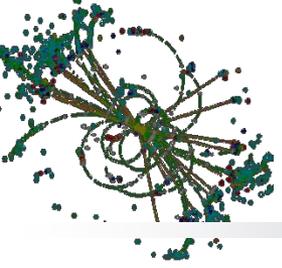
- **2004 – talks with Sarnoff Corporation started.**
 - ↵ Oregon University, Yale University and Sarnoff Corporation **collaboration formed.**
- **January, 2007**
 - ↵ Completed design – Chronopixel
 - ❖ **2 buffers, with calibration**
- **May 2008**
 - ↵ **Fabricated 80 5x5 mm chips**, containing 80x80 **50 μm** Chronopixels array (+ 2 single pixels) each
 - ↵ **TSMC 0.18 μm ⇒ ~50 μm pixel**
 - ❖ Epi-layer only 7 μm
 - ❖ Low resistivity (~10 ohm*cm) silicon
- **October 2008**
 - ↵ Design of **test boards** started at SLAC
- **September 2009**
 - ↵ Chronopixel chip **tests started**
- **March 2010**
 - ↵ **Tests completed**, report written
- **May 2010**
 - ↵ **contract** with Sarnoff for developing of second prototype **signed**
- **September 2010**
 - ↵ **Second prototype design started**
- **October 2010 - September 2011**
 - ↵ Sarnoff works **stalled**
- **February 2012**
 - ↵ **Submitted** to MOSIS for production at **TSMC**. (48x48 array of **25 μm** pixel, **90 nm** process)
 - ↵ **Modification** of the **test stand** started as all signal specifications were defined.
- **June 6, 2012**
 - ↵ **11 packaged chips** delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
 - ↵ Tests at SLAC started
- **March 2013**
 - ↵ Test results are discussed with Sarnoff and prototype 3 design features defined
- **July 2013**
 - ↵ **Contract with Sarnoff signed**
- **April 2014**
 - ↵ **Design submitted for fabrication**
- **July 2014**
 - ↵ **Scheduled packaged chip delivery**



Prototype 1 summary



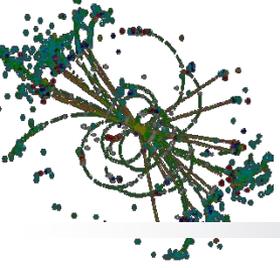
- Tests show that general **concept is working**.
- **Mistake was made in the power distribution** net on the chip, which led to only **small portion of it is operational**.
- Calibration circuit **works as expected in test pixels**, but for unknown reason **does not work in pixels array**.
- Noise figure with “soft reset” is within specifications ($0.86 \text{ mV}/35.7 \mu\text{V}/e = 24 \text{ e}$, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is **2.7 times larger** required (250 e).
- Sensors leakage currents ($1.8 \cdot 10^{-8} \text{ A}/\text{cm}^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz .
- No problems with **pulsing analog power**.
- Pixel size was $50 \times 50 \mu\text{m}^2$ while we want $15 \times 15 \mu\text{m}^2$ or less.
- However, CMOS electronics in prototype 1 could allow high charge collection efficiency only if encapsulated in **deep p-well**. This requires **special process, not available for smaller feature size**.



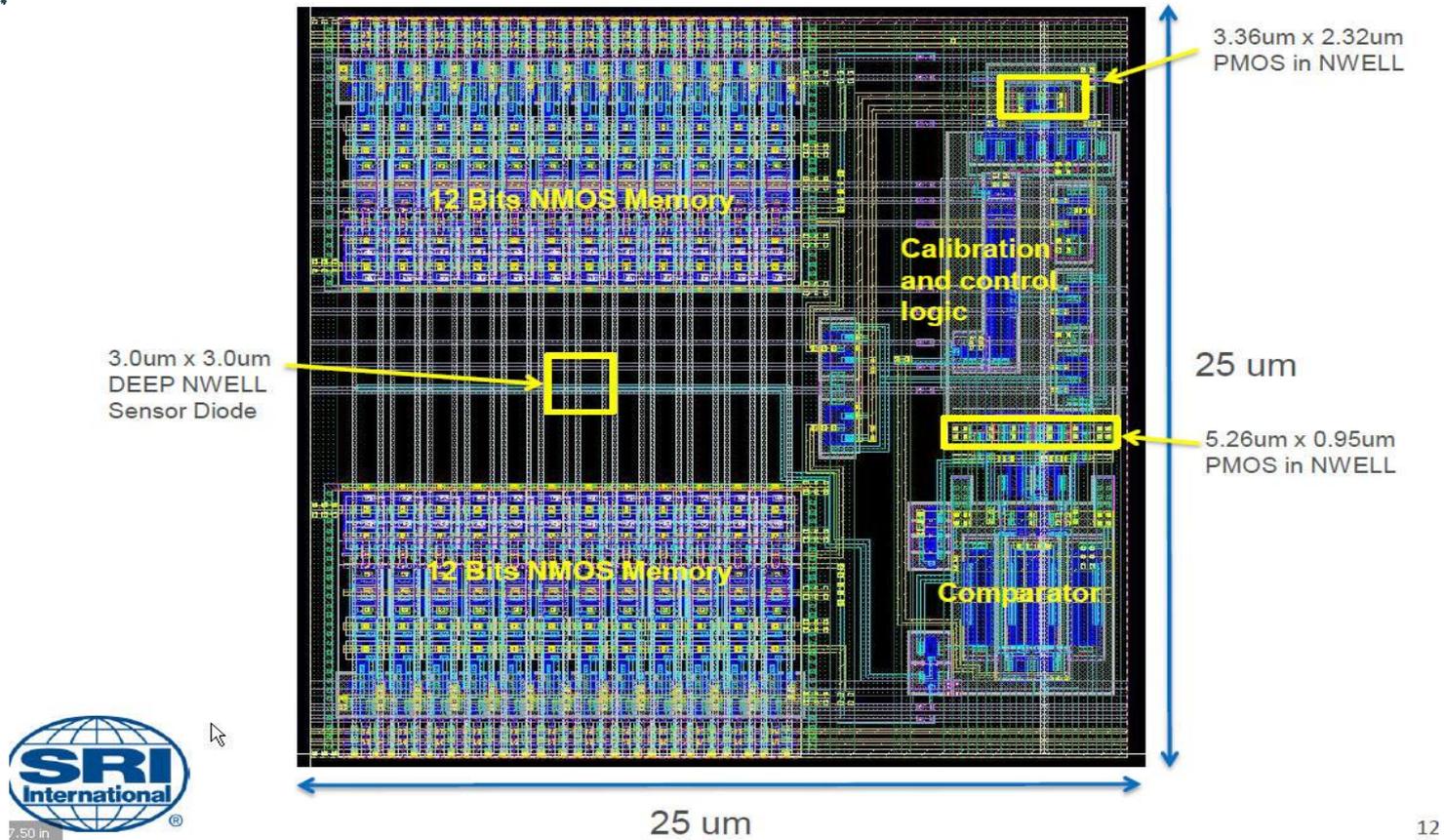
Prototype 2 features



- Design of the next **prototype** was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all **electronics inside pixels** only from **NMOS** transistors. It can allow us to have **100% charge collection without** use of **deep P-well** technology, which is expensive and rare. To reduce all NMOS logics power consumption, **dynamic memory cells design** was proposed by SARNOFF.
- **New** comparator offset compensation (“**calibration**”) scheme was suggested, which **does not have limitation in the range** of the offset voltages it can compensate.
- We agreed **not to implement sparse readout** in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.
- In September of 2011 Sarnoff suggested to build next prototype on **90 nm** technology, which will allow to reduce pixel size to **25 μ x 25 μ**
- We agreed to have **small fraction** of the electronics **inside pixel** to have **PMOS** transistors. Though it will reduce charge collection efficiency, but will **simplify comparator** design. It is very **difficult** to build good comparator with **low power** consumption on **NMOS only** transistors.

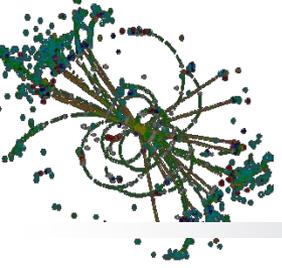


Prototype 2 pixel layout



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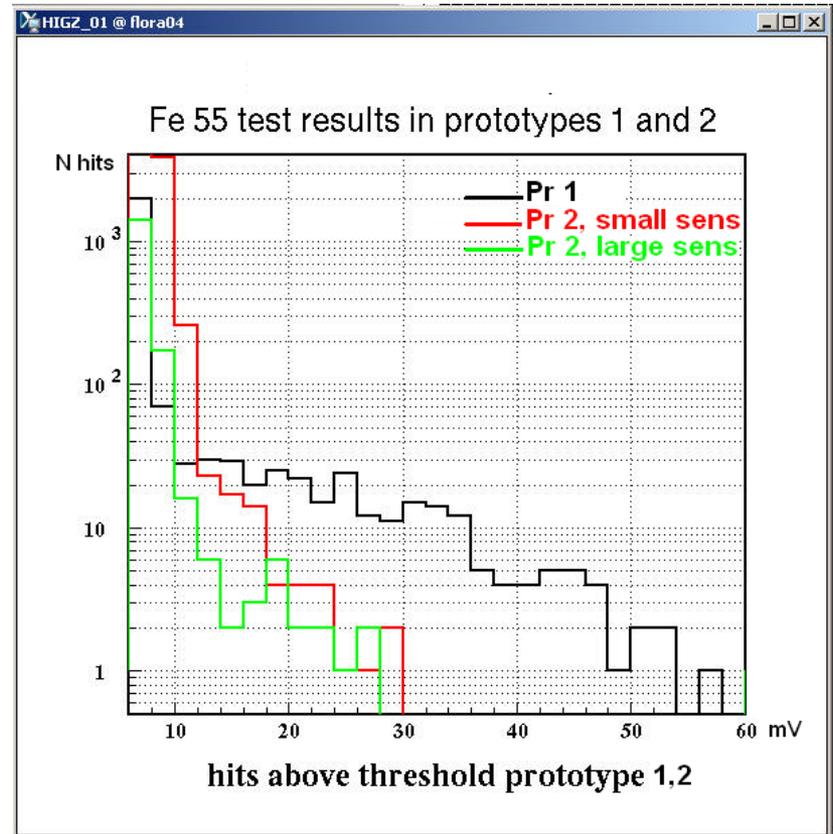
All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP NWELL), half of the pixels have it's size increased to $4 \times 5.5 \mu^2$.

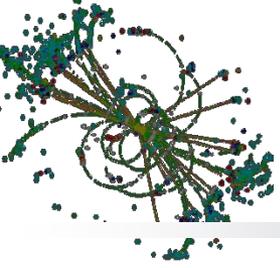


Test results – sensor capacitance

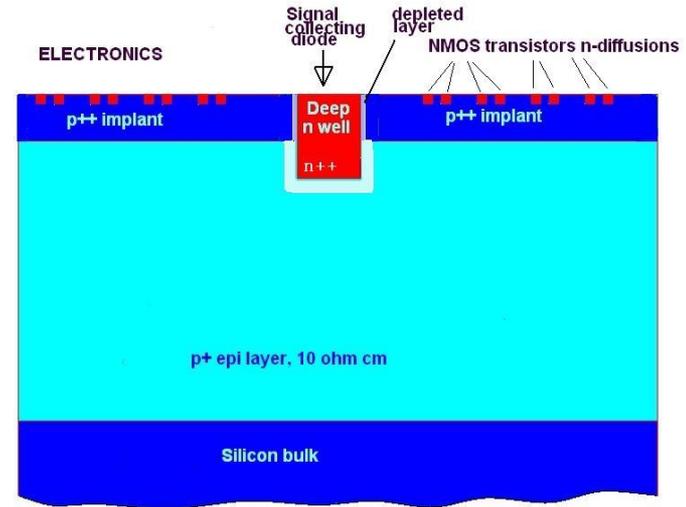
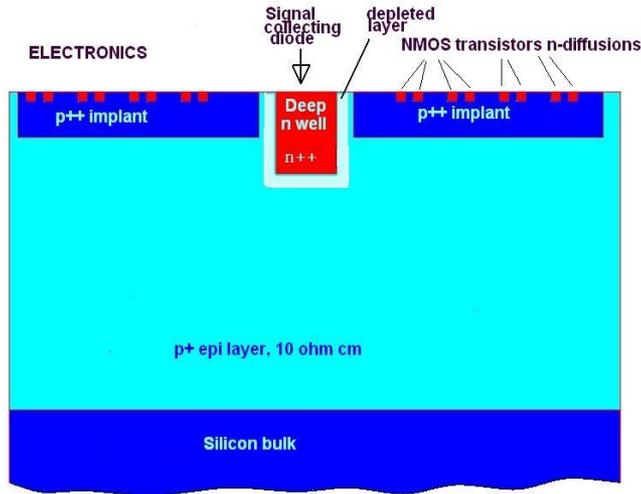


- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Prototype 2 has 2 sensor size options – $9 \mu^2$ and $22 \mu^2$ (“small” and “large” on the plot) . The maximum signal value is **roughly in agreement with expected capacitance difference** , though we would expect larger difference in maximum signal values here. But capacitance of the sensor from this measurements (~ 7.5 fF) appeared much larger than our expectation ($\sim 1-2$ fF).

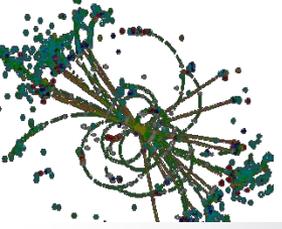




What got wrong?



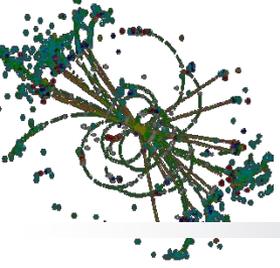
- We **hoped**, that pixel cross-section will look like what is **shown on left** picture. But it appeared, that in 90 nm design rules it is **not allowed** to have window in the top p++ implant **around deep n-well**, which forms our sensor diode. Resulting pixel cross-section is shown on **right** picture. **Very high** doping concentration of p++ implant leads to **very thin depletion layer** around side walls of deep n-well, which creates additional **large capacitance**.



Summary of prototypes tests



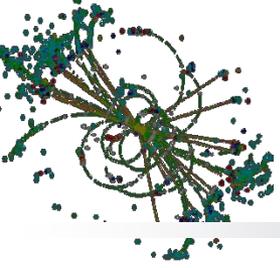
- From both, first and second prototype tests we have learned:
 - ↪ 1. We **can** build pixels which can record **time stamps with 300 ns period** (1 BC interval) - prototype 1
 - ↪ 2. We **can** build readout system, allowing **to read all hit pixels** during interval between bunch trains (by implementing **sparse readout**) - prototype 1
 - ↪ 3. We **can** implement **pulsed power** with 2 ms ON and 200 ms OFF, and this **will not ruin** comparator performance - both prototype 1 and 2
 - ↪ 4. We **can** implement **all NMOS** electronics **without** unacceptable **power consumption** - prototype 2. We **don't know yet** if **all NMOS** electronics is **a good alternative solution** to deep P-well option.
 - ↪ 5. We **can** achieve comparators **offset calibration** with virtually **any required precision** using **analog calibration** circuit.
 - ↪ 6. Going down to **smaller feature size is not as strait forward** process as we thought.



Prototype 3 wish list



- **Wish list, accepted by Sarnoff for the next prototype:**
 - ↵ **1. Find a way to decrease sensor capacitance** (they think they know how, and their calculations show decrease by factor 10).
 - ↵ **2. Take care about crosstalk** : separate analog and digital power and ground, shield trace, connecting sensor to source follower input from busses, caring strobes and clocks (by changing metal layers designations)
 - ↵ **3. Implement 2-way calibration** process
 - ↵ **4. Remove buffering of sensor reset** pulse inside the chip. It will allow us to **control the amplitude** of this pulse, which is especially important with decreased sensor capacitance.
 - ↵ **5. Remove unnecessary multiplexing of time stamp** (pure technical shortfall of prototype 2 design, which may limit speed and increase feed through noise).
 - ↵ **6. Improve timestamp memory robustness** (right now about 1% of memory cells fail to record time stamps correctly).



Prototype 3 : wish list addressed



- On the next few slides **I will show slides sent to me by Sarnoff team with suggested solutions to our concerns. The major topic – reduction of sensor capacitance will be discussed at the end**, as they suggested 6 different sensor options, and I want to discuss them in details.
- **To reduce cross talks, one of the obvious solution was the separation of analog and digital power supplies. It was not done in prototype 2 because of not enough pins in the package, and 40 pin package was used because small chip size, so chip periphery did not have enough space. Now MOSIS allows bonding pads pitch 90 μm as seen from the slide at right, which shows suggested 68 pin packaging diagram.**

Text from MOSIS Site

Text from MOSIS site

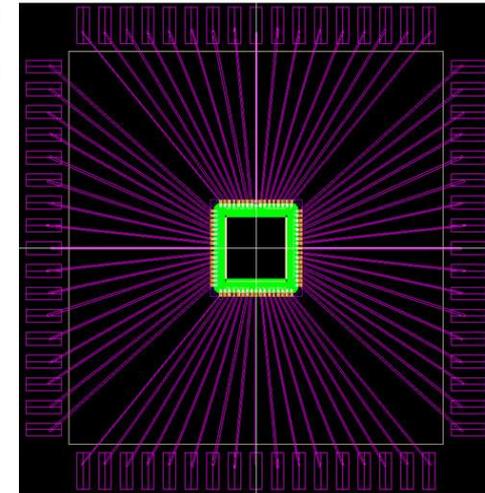
MOSIS general rule for minimum pad layout for wire bonding is:
90 μm x 90 μm (3.5 mils x 3.5 mils) glass cut box over a 100 μm x 100 μm (3.9 mils x 3.9 mils) top metal box (bonding metal) with a 150 μm x 150 μm (5.9 mils x 5.9 mils) pitch.

Additionally **most assembly vendors should be able to bond pads with 60 μm x 60 μm pad openings and 90 μm pitch. MOSIS assembly vendors can easily bond pads with these dimensions, subject to bonding diagram approval.**

Pads should be centered at the designated pad location.
If vendor design rules require a single via is used under the bonding metal, then it should be a box corresponding to the glass cut, also centered.

Bonding wires should not be at an angle greater than 45 degrees to the chip's axis.

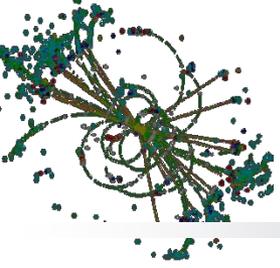
Our proposed bond scheme should fit these guidelines



9 May 2014

Notes for Prototype 3

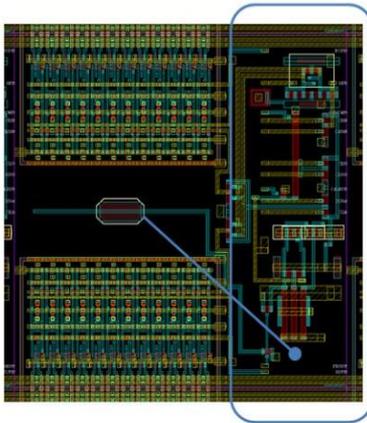
1



Cross talks – capacitive coupling and decoupling

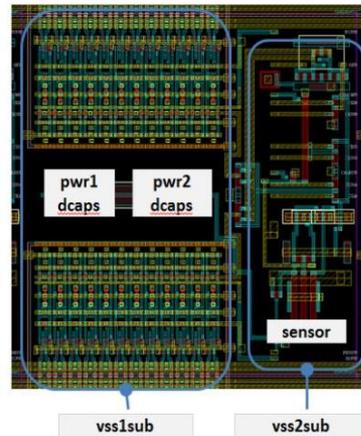


Proto 2 Comparator and Sensor

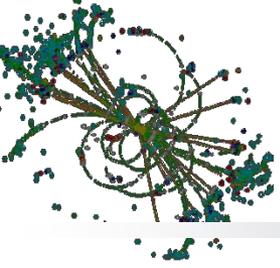


- Re-layout comparator region
 - Try to put Nwells closer to each other
- Investigate alternate no-Nwell comparator possibilities
 - Time and area permitting
- Construct sensor with NTN (no Pwell)
- Move sensor to different location nearer to comparator
 - Currently located under MIM
 - Better chance for a light slot by moving it
 - Currently also located under time stamp data lines
 - Must move to prevent capacitive coupling of time stamp data lines to sensor metal line

Power Supply Improvements



- Separate the power lines of the memory and other logic from the comparator
 - To prevent or mitigate crosstalk
- Additionally, separate sub ties from ground lines
 - Otherwise, there can be DC substrate current in addition to glitch currents in the circuits
 - vss1 to memories surrounded by vss1sub connected to neighboring pixels by M1 grid
 - vss1c to comparator surrounded by vss1csub.
- Additionally, add power filter caps
 - Best place is between memories under the data lines
 - Signals other than power would suffer crosstalk under these lines anyway
- Chip-wide
 - Add power pins to mitigate inductance and resistance of bond leads and package lead frame
 - Put drivers external to the pixel array into deep Nwell to decouple them from the main substrate
- Expectation is to yield major performance improvement using improved pixel and chip-wide power plan

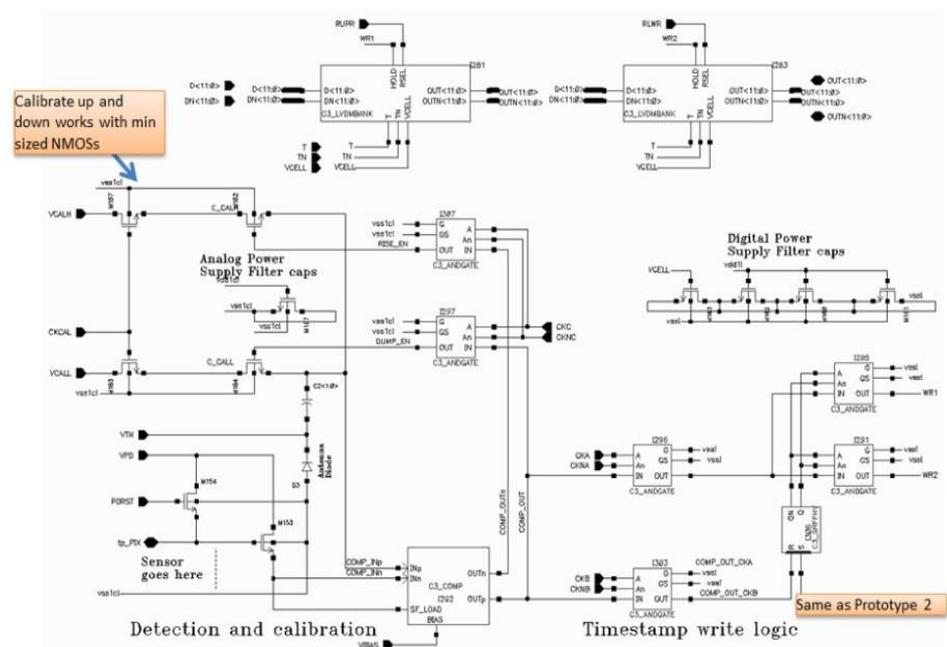


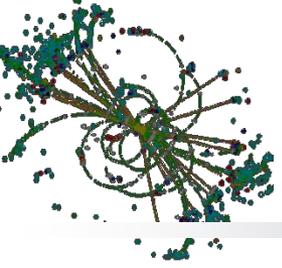
Two-way calibration implemented



- In prototype 2 calibration of comparator offsets begun with **voltage on calibration capacitor large enough** to cover all possible offsets range, and during calibration **went only one way** (lower and lower) until comparator reached balanced state. It had **few disadvantages** – as the voltage steps should be not more than 1 mV, calibration required **large number of steps**. And any noise pulses during calibration would move level only in one direction, so we would **end up with voltage few sigma noise lower**, than we want. So, we requested two-way calibration scheme. It was implemented as shown on right and simulated with SPICE model to make sure it will work.

Prototype 3 Pixel Mods (Power Supply Splits: up/down calibration)

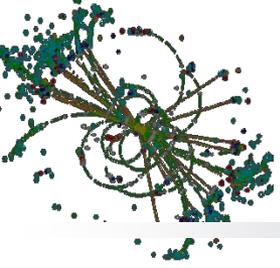




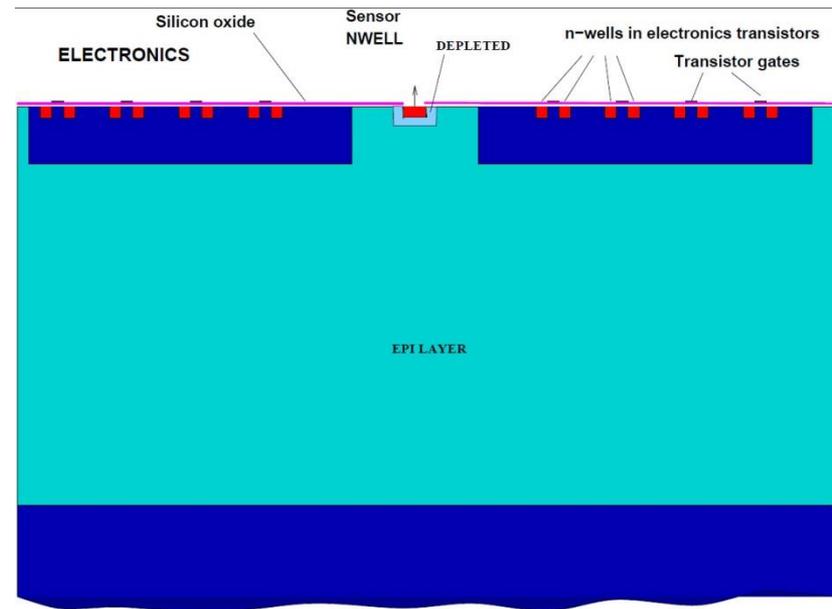
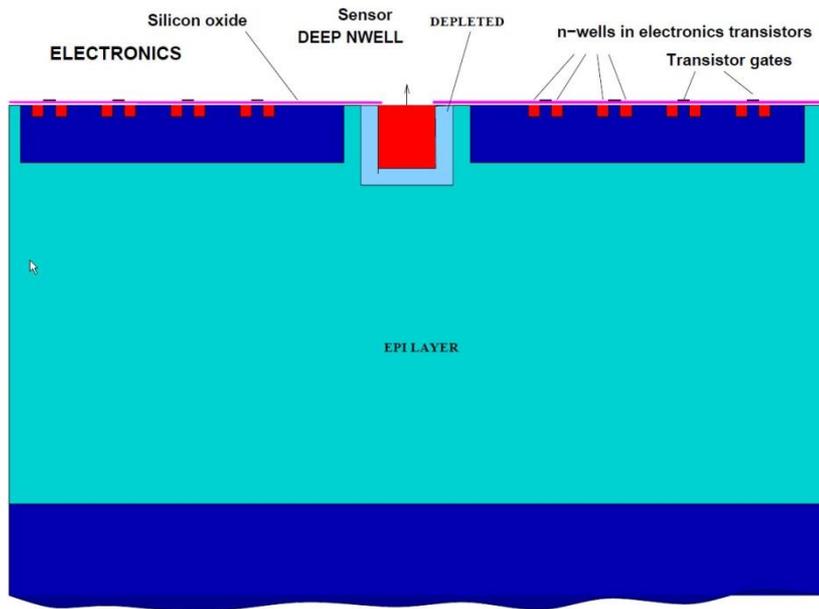
Sensor options in prototype 3



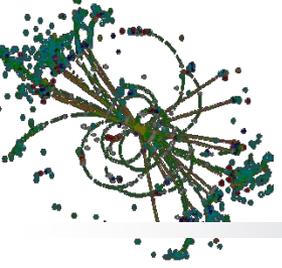
- **6 different** sensor options were implemented on the same chip – **8 column** allocated for each option:
 - ↪ **1** – same as in prototype 2 – for comparison
 - ↪ **2** – deep NWELL diode in the window in P++ layer – this **violate design rules**, but the **waver** for design rules was **accepted** by TSMC
 - ↪ **3** – shallow NWELL diode also in the window – also **violates** design rules, but **waver** was accepted
 - ↪ **4** – “Natural transistor” (NTN) **allowed by design rules** to be in the P++ layer **window** – transistor is formed **directly on P+ epi** layer. **Large** source and drain diffusion areas, **gate connected to both** source and drain and form sensor output
 - ↪ **5** – **also NTN** but with **2 fingers**, source and drain are **narrow**, **gate also connected** to both, as in option 4
 - ↪ **6** – **same as 5**, however **gate is not** connected to source and drain, but connected to external bias voltage.



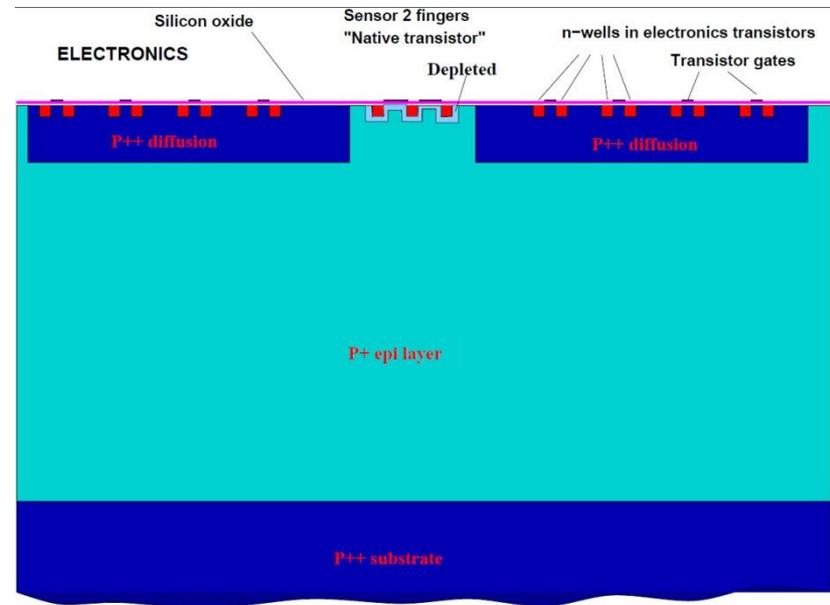
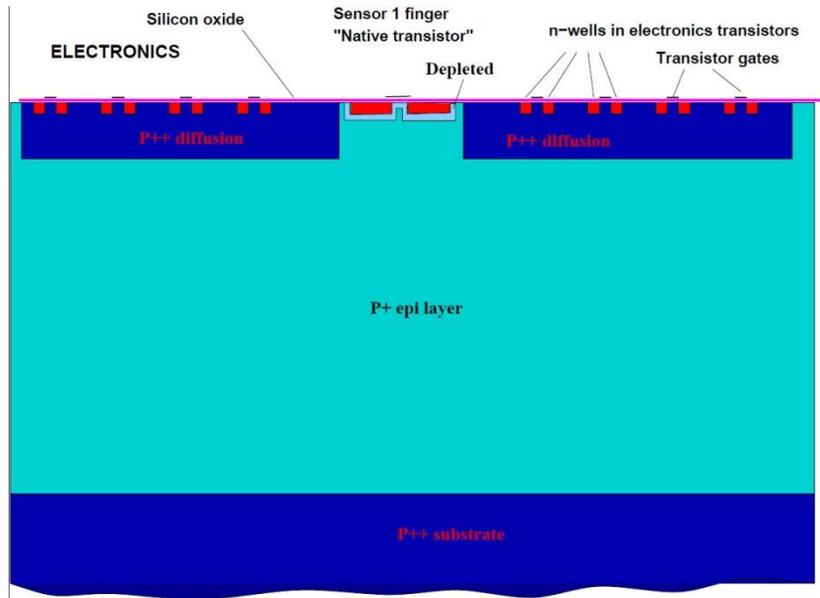
Options with N WELL diode – violating design rules



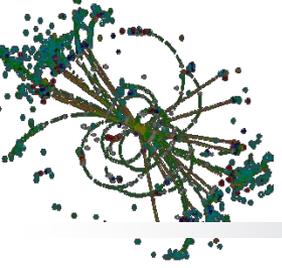
It will be interesting to compare **deep and shallow n-wells**. **Deep** has **larger area**, so larger **charge collection efficiency**, however, **larger capacitance**. **Shallow** option has **smaller area**, but because **P++** acts as **charge reflector**, the charge collection **efficiency** may be defined **not by diode size**, but by **window size**. It depends on **how deep is P++** implant, of course.



Options with “Natural transistor”



In **1 finger** option the **size of nwells** forming source and drain is **larger**, so we can hope for **better charge collection** efficiency. However, sensor **capacitance** may be **larger also**. There is **2 2-finger** options – one with **gates connected to source and drain**, another – to **external bias**. It will be interesting to see how these two options behave



Summary and plans



- Chronopixel R&D are moving forward, **we have solved many** problems and proved that concept is valid.
- If suggested **solution** of the major problem of 90 nm technology for our application **will work**, we may have sensor design **implementable on a standard** foundry process.
- We **have signed** contract with Sarnoff for prototype 3 design in July of 2013. The **design is now completed** and submitted for fabrication. We expect packaged devices at SLAC by the end of **July 2014**.
- From our side – we **need to modify** test stand to fit new design, and perform all test as soon as we receive sensors. There should be **no problems** with it. The adapter for 68 pin package is already designed, the software modification for test stand started.