

The pixel TPC

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Bundesministerium für Bildung und Forschung <u>Outline:</u>

- Pixelated gaseous detectors: Motivation & History
- Timepix and InGrid
- LCTPC-pixel group activities
- Demonstrator module



Linear Collider Forum 2014, April 29, Bonn





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Possible applications:

- Rare event searches: CAST, DARWIN
- Tracking: GOSSIP, ILC







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- 2009: Performance and prospects of GridPix and Gossip detectors H. van der Graaf, F. Hartjes, A. Romaniouk, ATLAS note ATL-P-MN-0016







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LCTPC-pixel collaboration

- LCTPC collaboration:
 - Develop a TPC for physics up to 1 TeV (at the ILC)
 - Groups from America, Europe and Asia
 - Several readout concepts using GEM/Micromegas
- LCTPC-pixel
 - R&D towards a pixel-TPC: MPGD + pixel readout
 - Groups:
 - NIKHEF: Module construction
 - University of Kiew: Simulation
 - LAL Orsay: Simulation
 - CEA Saclay / DESY: Data analysis
 - Uni Bonn: Module construction, readout system, data analysis
 - Uni Siegen: Data analysis
 - Goal: build a demonstrator module for a pixel-TPC





LCTPC Prototype

Setup at DESY





Timepix chip

- Readout chip used for many applications
- Characteristics:
 - Active surface: 1.4 x 1.4 cm², 256 x 256 pixel array
 - Pixel size 55 x 55 μm²
 - 14 bit counter in each pixel (measure arrival time or charge)
 - Analog part: single threshold typical at $\sim 500e^{-1}$ (ENC $\approx 90e^{-1}$)







- Aluminium mesh on chip
 - Hole to pixel alignment
 - Pillar height uniformity



- Use photolithographic process
 - Pioneered and optimised by NIKHEF and University of Twente
 - Production on single chip basis ____

Production on wafer scale

- High demand for InGrid chips:
 - R&D at Bonn, NIKHEF, Saclay
 - Equipment of larger surfaces
 - \Rightarrow Production on wafer scale
- 8 inch wafer = 107 chips



has machinery for post-processing





2013 test beam @ DESY





Prototype + pixel module



Setup at DESY





March/April 2013: 2 LCTPC octoboard modules

- Different amplification structures: GEM / InGrid
- Test of readout system
- Readout rate: 2.5 Hz; 40MHz clock
- Electron beam of up to 6 GeV
- Gas: Ar:CF4:iC4H10 (95:3:2) = T2K gas
- ~ 2 Mio. frames recorded, including B = 1 T
- Extensive testbeam program
- Preliminary data analysis in MarlinTPC Robert Menzen

Reconstructed tracks















Preliminary z-scan results





Detector construction

Jan Timmermans (NIKHEF) : 2 Octopuce testbeam

- Construction of InGrid octoboards
- Testbeam with 2 Octoboards @ LP in March 2014
 - B = 0T and B = 1T
 - Stable operation
 - Analysis not started
- Plan for module layout + readout







Data analysis



Andrii Chaus (DESY/CEA Saclay): Processing Octoboard test beam data

- MAFalda analysis framework ok for fast analysis at testbeam
 - Track reco based on raw data, no GEAR info
 - Field distortions, drift velocity, residuals, diffusion
- MarlinTPC for real analysis (using GEAR information)
 - Processors for octoboard analysis
 - Analysis chain setup ongoing
 - GEAR geometry for 2 InGrid octoboards + 5 Micromegas

Amir Shirazi (Uni Siegen):

Just started to set up and learn MarlinTPC

Simulation

Oleksiy Fedorchuk (Uni Kiew) : Octoboard simulation

- Single octoboard simulation
 - Successfully modelled
 - Field distortions
 - Simulated occupancy similar to data

1T

E^{1.6}

Dead distance, 1.5 1.4 1.5

1.2

1.1

- Impact of shifted chips
- Next step:

0T

0.38

0.36

0.34

0.32

0.3

0.36

0.34

0.3

0.26

- 100 chip module

0.3





Bonn group activities

Data analysis

Martin Rogowski: A new tracking algorithm

Algorithm from Forward Tracking Detector for ILD





- Comparison of different algorithms
 - Standard Hough Transformation from MarlinTPC
 - Fast Hough Transformation (DESY)
 - Randomized Hough Transformation (Lappeenranta)





Scalable Readout System (RD51, CERN)





Chain: Chip – Adapter card+FEC – Computer

SRS with Timepix chip





SRS FEC - Adapter board - HDMI cables - intermediate board - octoboard

New intermediate board



I2C: standard for small network. Signals: scl (clock), sda (data) Originally between PCBs next to each other. Several meters distance using extenders.



Status Timepix+SRS Readout

Since 2013 testbeam:

- Upgrade of hardware
 - HDMI cables
 - LVDS drivers
 - No analog/CMOS signals through cables
 - I2C for slow control
- Upgrade of FPGA firmware
 - DDR2 Ram
 - Support ADC and DAC
- Upgrade of DAQ software
 - ADC readout for DAC scan
 - automatic calibration with test pulses from multiplexer
- Redesign of intermediate board and A Card for scale-up
 - Error in layout found and fixed

LP module: next steps

~100 chip module



- Project: test a 32 InGrid board in September/October
 - Similar design as 8 InGrid module
 - Expandable to 96 InGrids
- Mechanical design (Johann Tomtschak)
 - CAD drawings in SolidWorks
 - Use water cooling
- Construction in workshop:
 - light LP frame
 - chip support structure



LP module: next steps



~100 chip module

- Field distortions & powering (Kathrin Kohl)
 - Was already critical for a single octoboard
 - Low voltage supply for 4/12 octoboards?





- PCB layout (Jochen Kaminski)
 - Depends on powering
 - Space is limited
 - Need many HDMI cables
- InGrid bonding, testing, quality control, calibration

Summary and Outlook

LCTPC-pixel collaboration is very active:

- Analysis of 2013 testbeam data
- Simulation of field distortions
- Development of readout system
- Design of a 32 / 96 chip module

=> Demonstrator for a pixel TPC (for ILD @ ILC)





Schedule for 2014

• Additionally:



- Need/would like to have a master student for full analysis
- Data analysis of new testbeam data
- 96 chip module test in 2015?

Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Octoboard capability HDMI board testing, Virtex 6 board			Firmware for 4 octoboards/ FEC		Test of full syste Software, Testbeam Prepera			m, ation	Da	ta analysis	
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PCB finalisation single/octoboards			32 chip module construction				Test	96 (eam _{cc}	chip module onstruction		
Jochen Kaminski, Michael Lupberger 2014/											
			Johann Tomtschak Kathrin Kohl					2015			
Track reconstruction algorithm											
2013 data analysis with new algorithm											
Martin Rogowski											
							Full 2	2013 da	ita anal	ysis?	B

We can provide soon:

- SRS (A card) with full functionality (for MUROS compatible intermediate board)
 - Users with SRS can plug and play Timepix
 - Users can use MUROS or SRS for same detector
 - Comparability study, documentation
- V6 evaluation board (VHDCI cables MUROS compatible):
 - Updated adapter board, I2c network tested
 - ADC, DAC control and readout with i2c (firmware, software)
 - Users with V6 board can plug and play Timepix
 - Users can use MUROS or SRS for same detector
 - Comparability study, documentation:
 - Use in CAST

Xilinx Evaluation board





Virtex 6 FPGA

Production on wafer scale



Probing and cleaning of the wafer

Adding $Si_x N_y$ protection layer

Application of the SU-8













Patterning of the grid

Dicing of the wafer





Preliminary Analysis: Cuts



Dataset for first analysis:

z-scan, B=0 T,
$$E_{Drift}$$
 = 230 V/cm (D_T = 311 µm/ \sqrt{cm})

 \Rightarrow tracks parallel to x-axis

Cuts:

- Only hits within shutter window
- More than 200 hits per track

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- Entries 400 Preliminary 350 300 250 200 Chip 150 100 50 0-50 -30 -40 -20 -10 0 10 20 30 40 d_0 in mm
- Tracks centred on lower chip row (z dependent)



Preliminary z-scan results





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