

DEPFET detectors for future e^+e^- colliders: Status and latest results

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DEPFET Collaboration



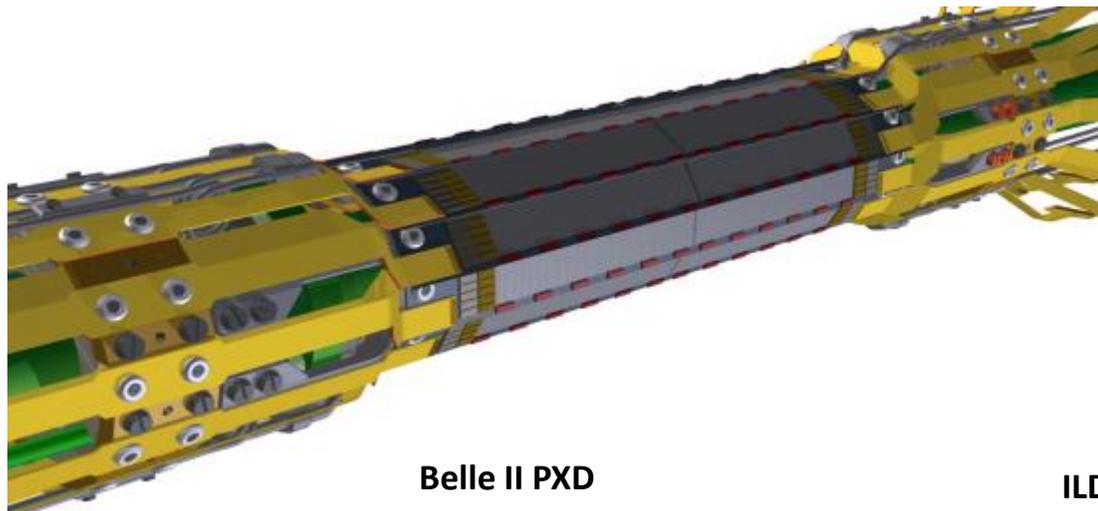
The DEPFET Collaboration

- Charles University, Prague
- DESY, Hamburg
- IFCA, Santander
- IFIC, Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- LMU Munich
- MPI, Munich
- HLL, Munich
- TU, Munich
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen
- University of Tabuk

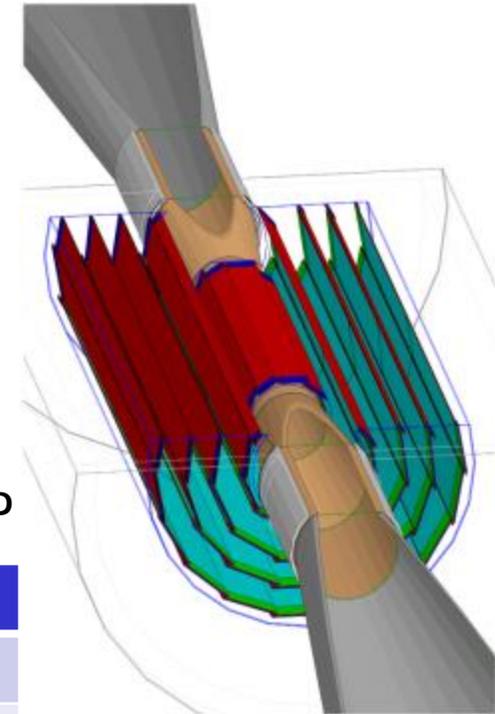


- SuperKEKB and ILC
Main common requirements
- DEPFET-based pixel detectors
Fundamentals
System elements
- Recent progress
PXD6 production
Test beam

The Belle II Collaboration decided on DEPFET as baseline for the pixel detector



Belle II PXD

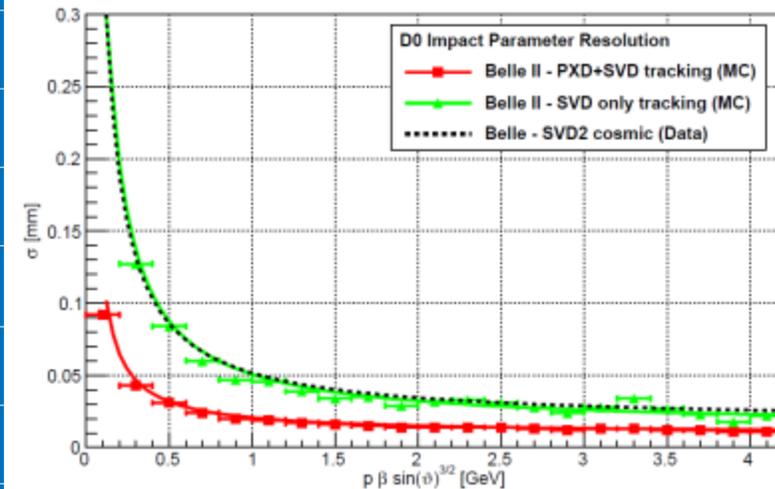


ILD 5-layer VXD

	Belle II	ILD LOI 5-layer layout	
Radii	14, 22	15, 26, 38, 49, 60	mm
Ladder length	90 (L1), 122 (L2)	123 (L1), 250 (L2-L5)	mm
Sensitive width	12.5 (L1-L2)	13 (L1), 22 (L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel size	50x50 (L1), 50x75 (L2)	25x25 (L1-L5)	μm^2
Frame rate	50	20 (L1), 4 (L2-L5)	kHz

The Belle II PXD DEPFET ladders: *almost* prototypes for L1 and L2 of ILD

	Belle II
Occupancy	0.4 hits/ $\mu\text{m}^2/\text{s}$
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Duty cycle	1
Frame time	20 μs
Momentum range	Low momentum (< 1 GeV)
Acceptance	17° - 155°
Material budget	0.21% X_0 per layer
Resolution	15 μm ($50 \times 75 \mu\text{m}^2$)

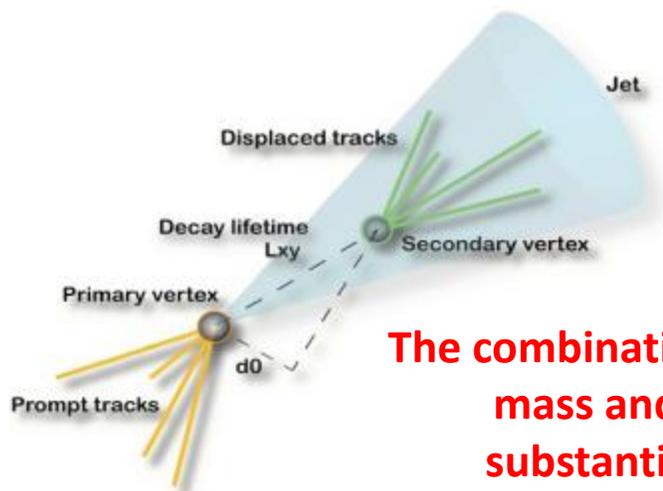


- Modest resolution (15 μm), dominated by multiple scattering \rightarrow Pixel size ($50 \times 75 \mu\text{m}^2$)
- Lowest possible material budget (0.2% X_0 /layer)
 - Ultra-transparent detectors
 - Lightweight mechanics and minimal services

	Belle II	ILC
Occupancy	0.4 hits/ $\mu\text{m}^2/\text{s}$	0.13 hits/ $\mu\text{m}^2/\text{s}$
Radiation	2 Mrad/year	< 100 krad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year	10^{11} 1 MeV n_{eq} per year
Duty cycle	1	1/200
Frame time	20 μs	25-100 μs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	17° - 155°	6° - 174°
Material budget	0.21% X_0 per layer	0.12% X_0 per layer
Resolution	15 μm (50x75 μm^2)	5 μm (20x20 μm^2)

- Excellent resolution (5 μm) \rightarrow Pixel size (20 x 20 μm^2)
- Lowest possible material budget (0.1% X_0 /layer)
 - Ultra-transparent detectors
 - Lightweight mechanics and minimal services

\rightarrow Both detectors have very similar requirements



The combination of resolution, mass and power is a substantial challenge

$$\sigma_{d0} \approx \sqrt{\frac{r_2^2 \sigma_1^2 + r_1^2 \sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{p \sin^{\frac{3}{2}} \theta} 13.6 \text{ MeV} \sqrt{\frac{x}{X_0}}$$

$$\sigma_{d0} \approx a \oplus \frac{b}{p \sin^{\frac{3}{2}} \theta}$$

▪ Common vertex detector requirements

- First layer close to the IP
- Low material budget
 - Reduced services
 - Low power dissipation
- High granularity
 - Good spatial resolution
- Fast readout
- Radiation hardness

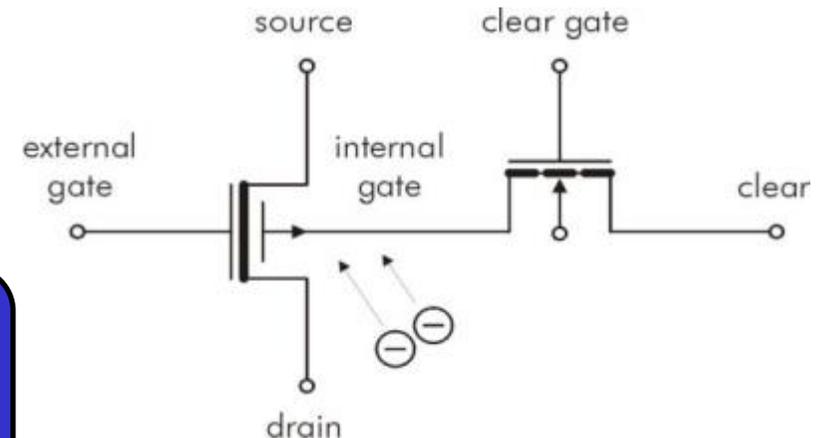
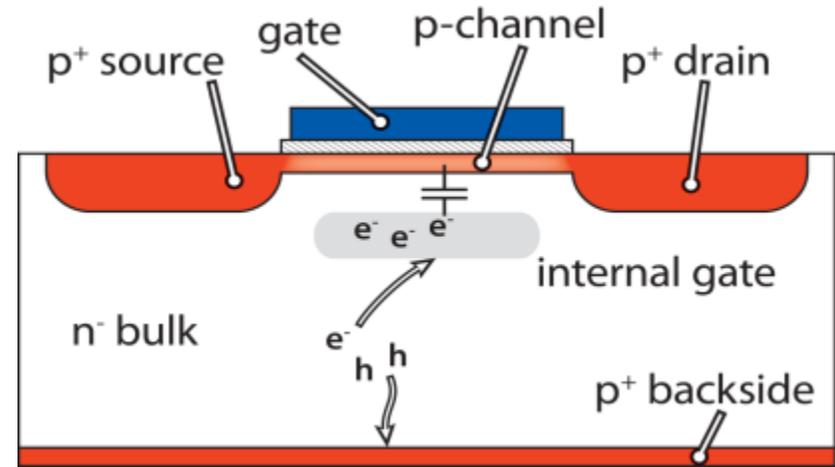
	a (μm)	b (μm GeV)
LHC	12	70
STAR	12	19
Belle II	8.5	10
ILC	5	10

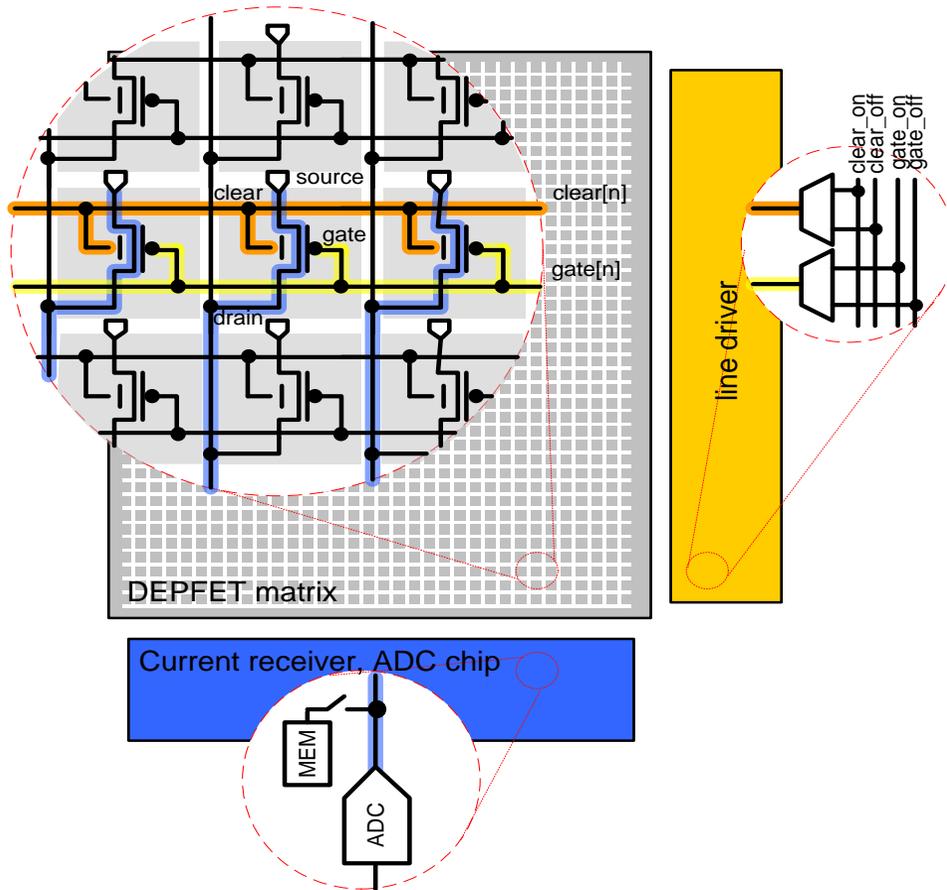
a: Governs high momentum
b: Dominates at low momentum

- Each pixel is a p-channel FET on a completely depleted bulk.
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)
- Signal electrons in the internal gate modulate the transistor current

$$g_q = \frac{\partial I_d}{\partial q} \propto \left(\frac{I_d}{L^3 W C_{ox}} \right)^{1/2} \sim 500 \text{ pA}/e^-$$

- Detection and internal amplification
- Small intrinsic noise
- Low power consumption

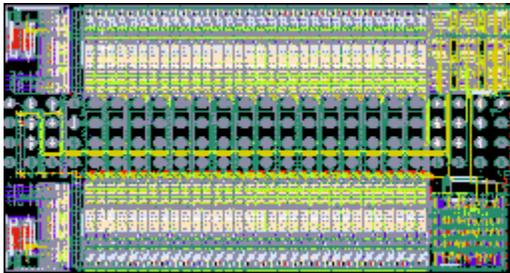




- Pixels are arranged in a matrix
- Row wise readout (4 rows at a time)
- Gate, clear lines need Switcher steering chip
- Long drain readout lines to keep material out of the acceptance region
- Only 'activated' rows consume power
 - The others are still sensitive to charge
 - Low power consumption

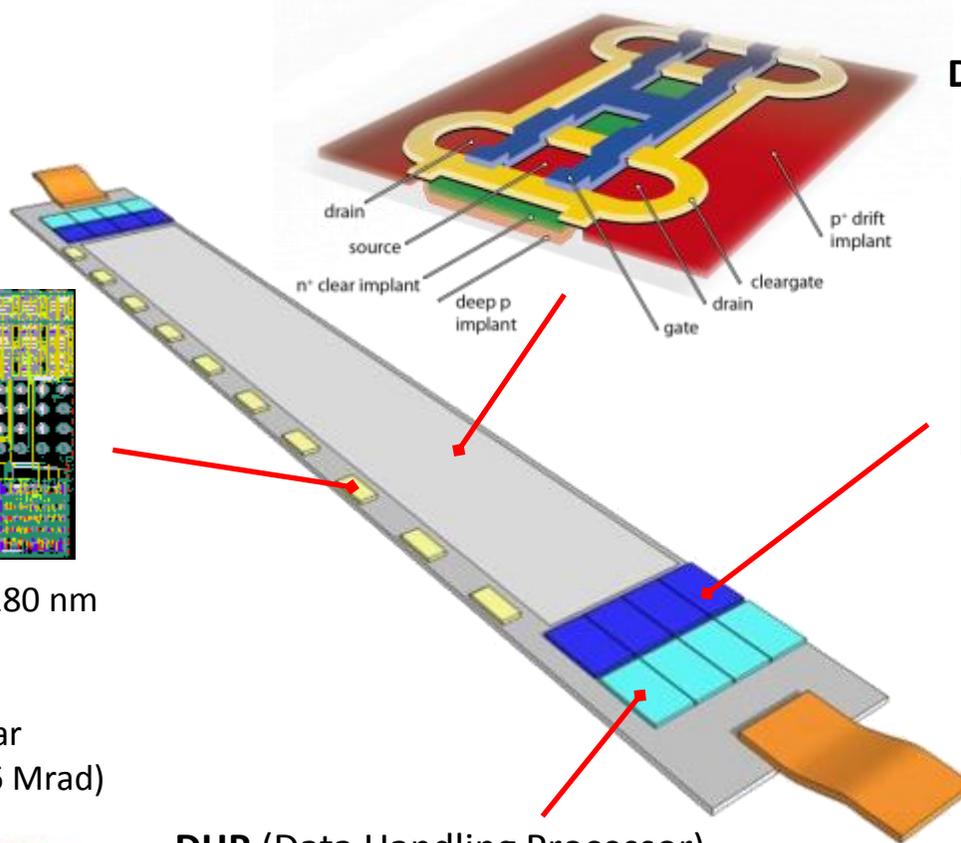
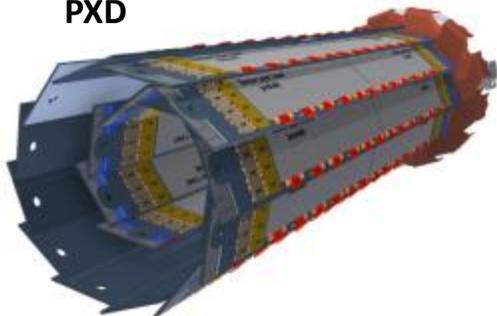
SwitcherB

Row control

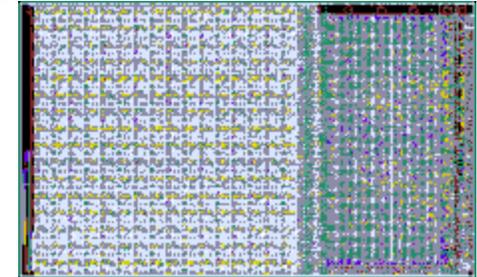


AMS/IBM HVCMOS 180 nm
 Size $3.6 \times 1.5 \text{ mm}^2$
 Gate and Clear signal
 Fast HV ramp for Clear
 Rad. Hard proved (36 Mrad)

PXD



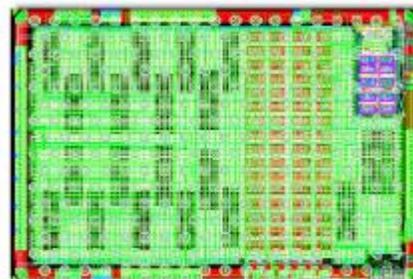
DCDB (Drain Current Digitizer) Analog frontend



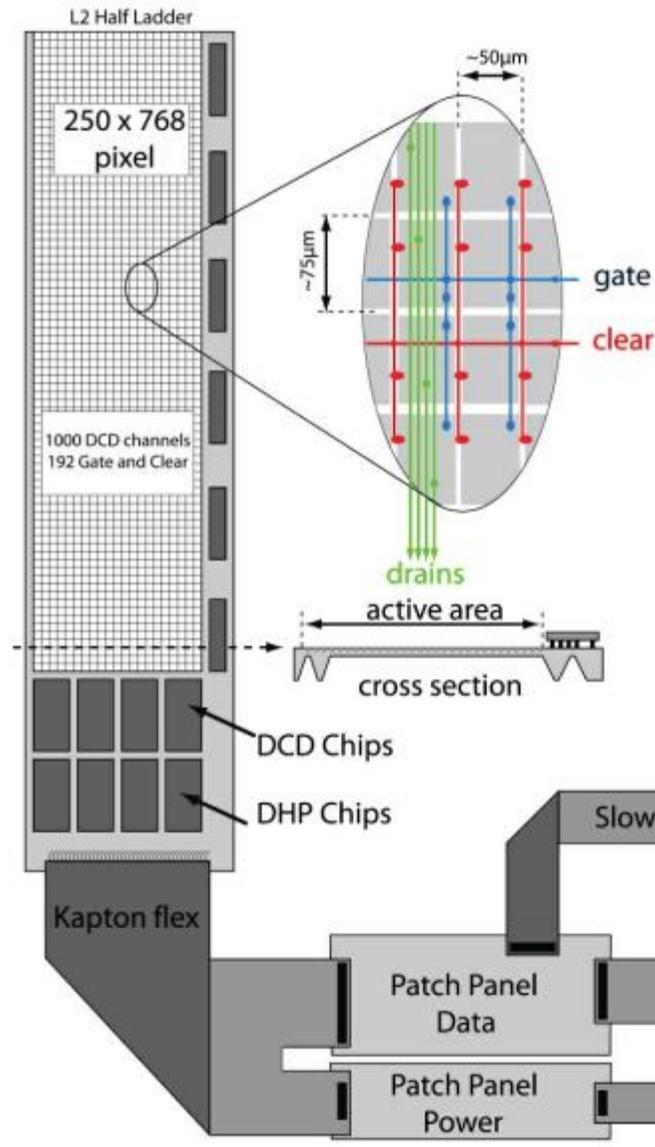
UMC 180 nm
 Size $5.0 \times 3.2 \text{ mm}^2$
 TIA and ADC
 Pedestal compensation
 Rad. Hard proved (20 Mrad)

DHP (Data Handling Processor)

First data compression



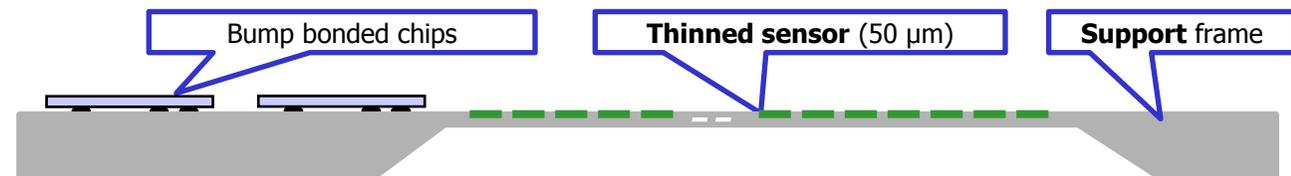
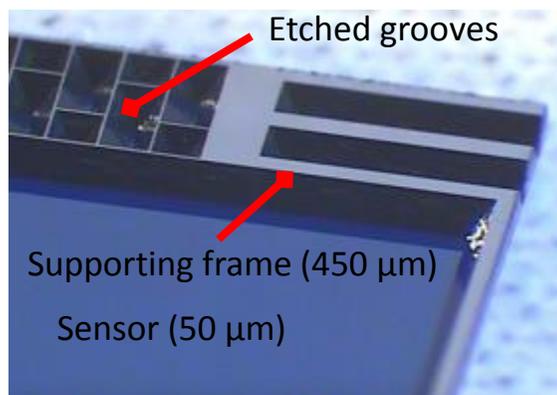
TSMC 65 nm
 Size $4.0 \times 3.2 \text{ mm}^2$
 Stores raw data and pedestals
 Common mode and pedestal correction
 Data reduction (zero suppression)
 Timing signal generation
 Rad. Hard proved (100 Mrad)

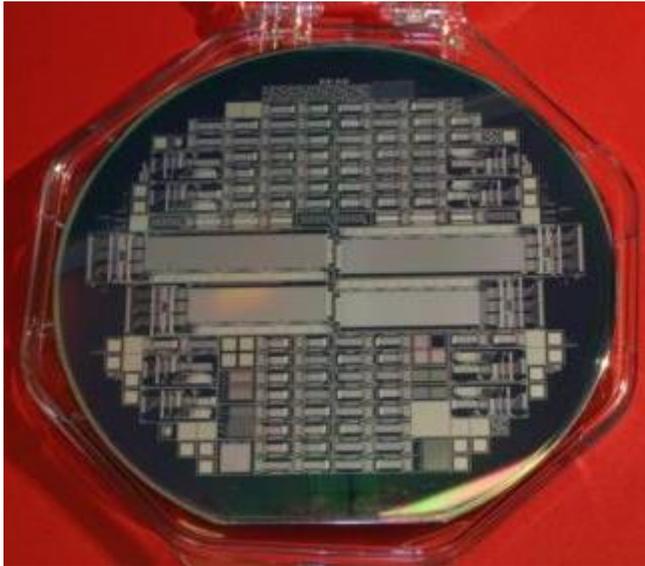


- **DHH** (Data Handling Hybrid)
Electrical - optical interface
Slow control master (JTAG)
Clustering
- **ONSEN**
Data buffer
Reduction via ROI selection (DATCON, HLT)

Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

- One material: uniform and small thermal expansion
- The DEPFET thickness is a free adjustable parameter





- 8 SOI wafers with 50 μm thin sensors (450 μm handle)
- Small test matrices with design variations
 - Full size sensors for prototyping

90 steps fabrication process:

9 Implantations

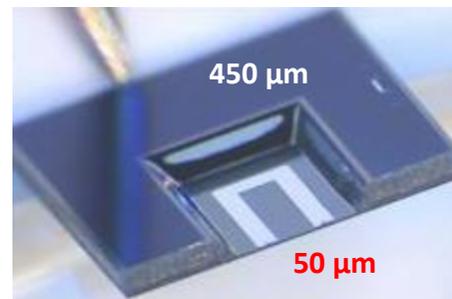
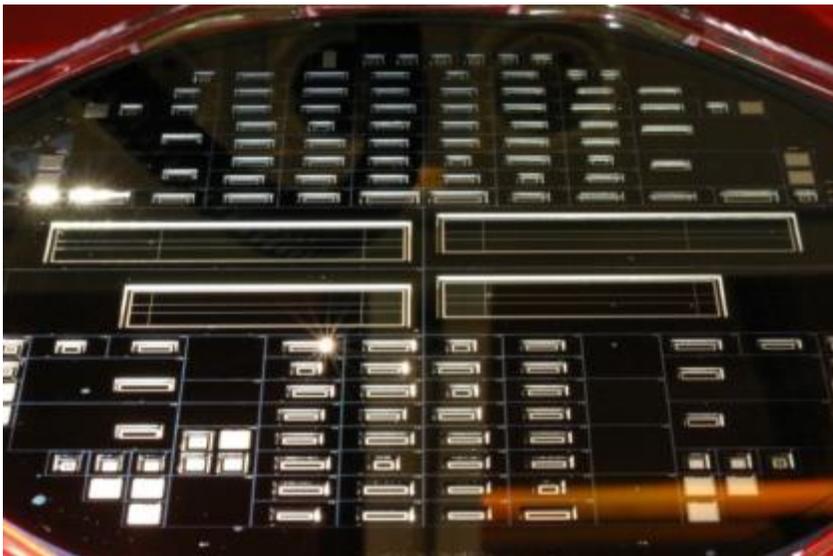
19 Lithographies

2 Poly-layers

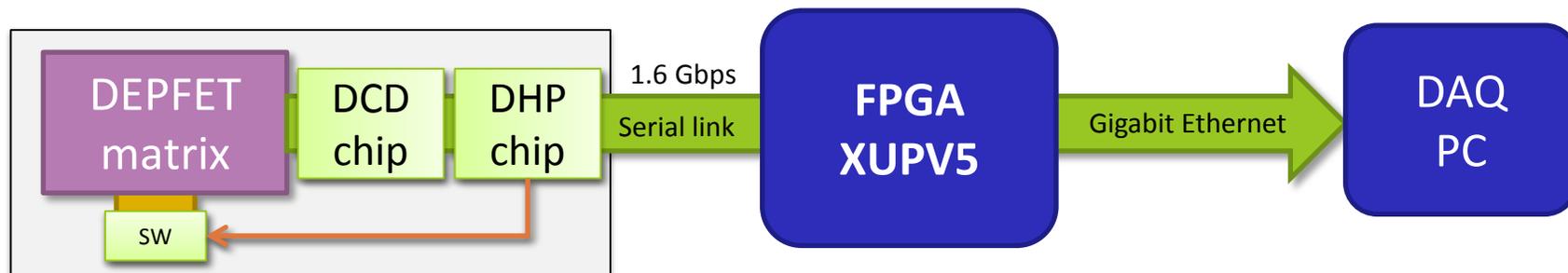
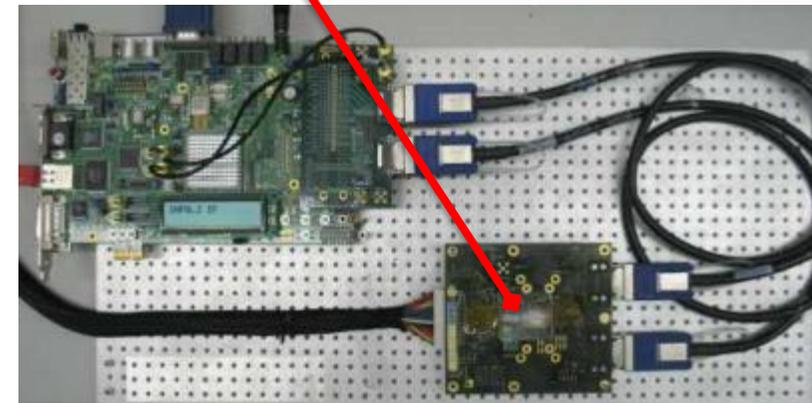
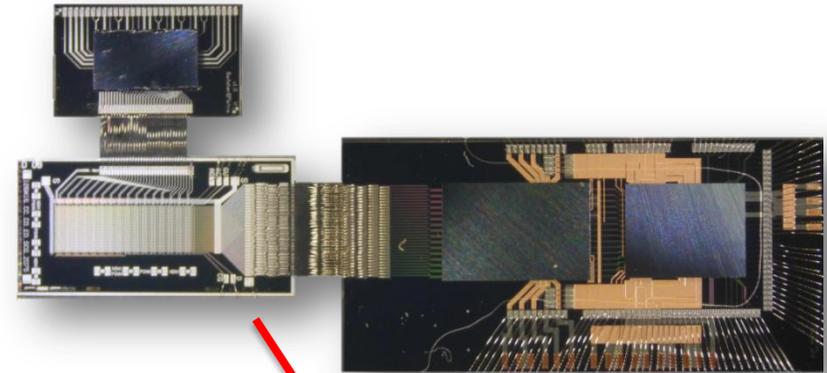
2 Alu-layers

1 Copper layer

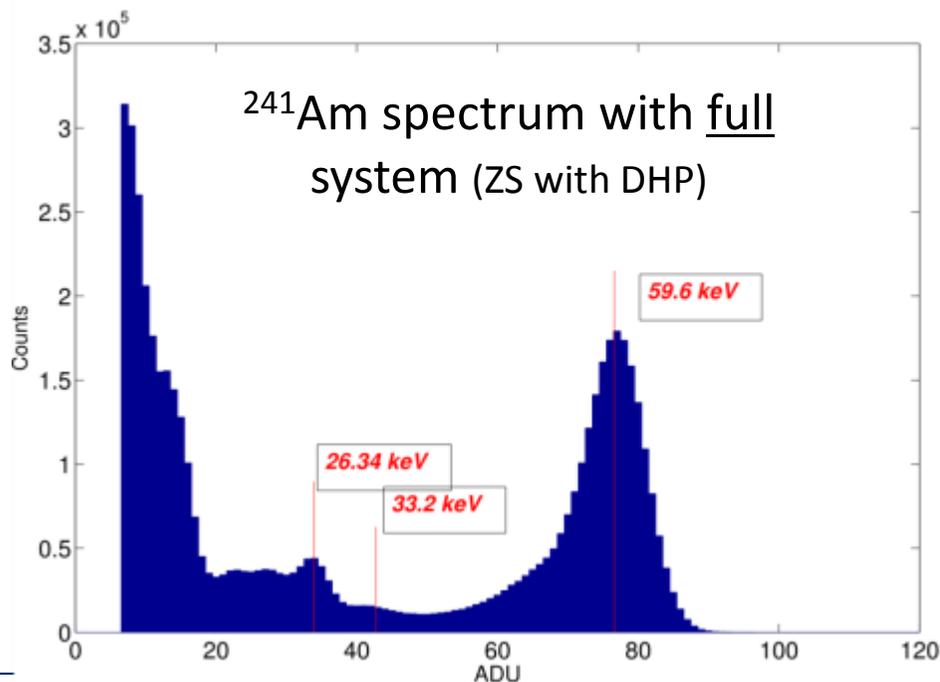
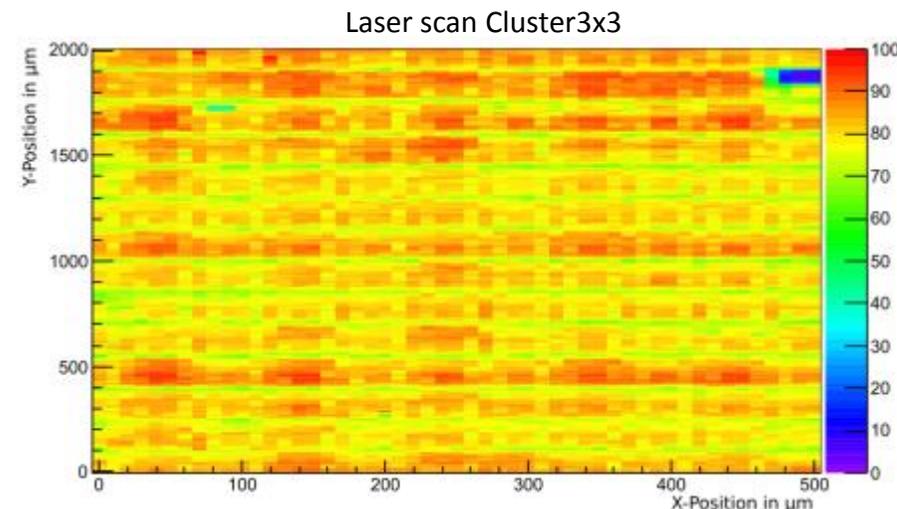
Back side processing



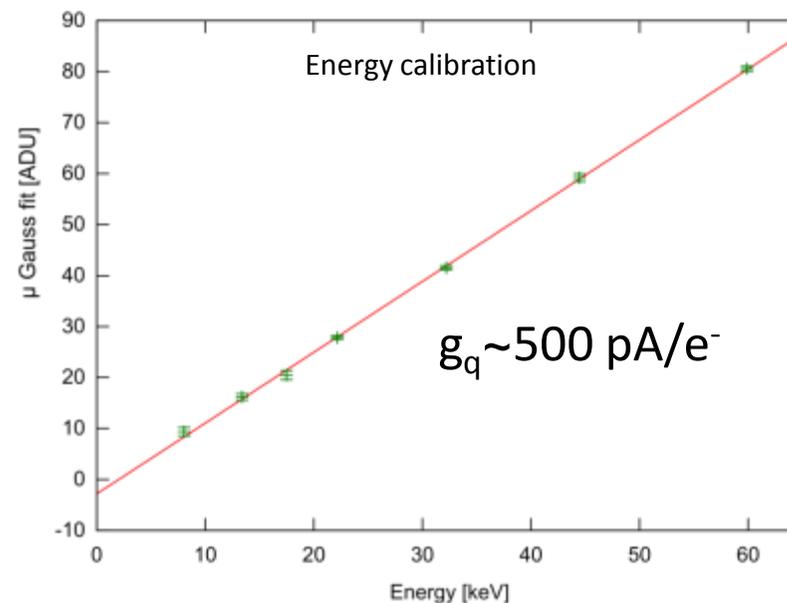
- Zero suppressed readout with the minimum necessary amount of components:
 - One Switcher-B
 - One DCDBv2
 - One DHP 0.2
 - Small thin matrix: Belle II SD PXD6 type, 16x128 pixels, 50x75 μm^2 pitch



- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
Charge collection homogeneity
In pixel studies
- Radioactive source
System calibration

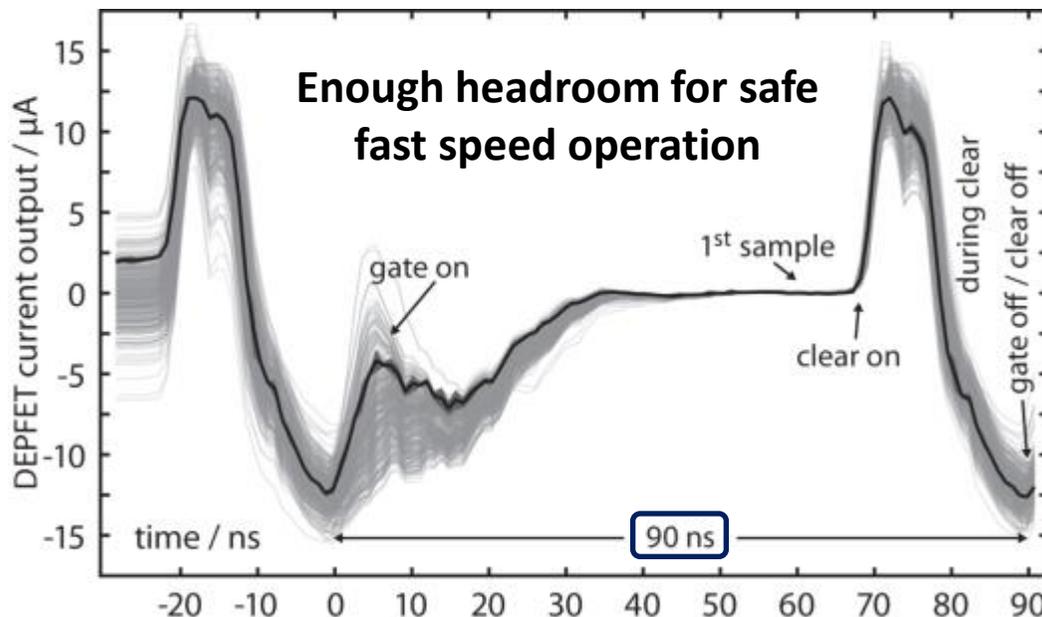
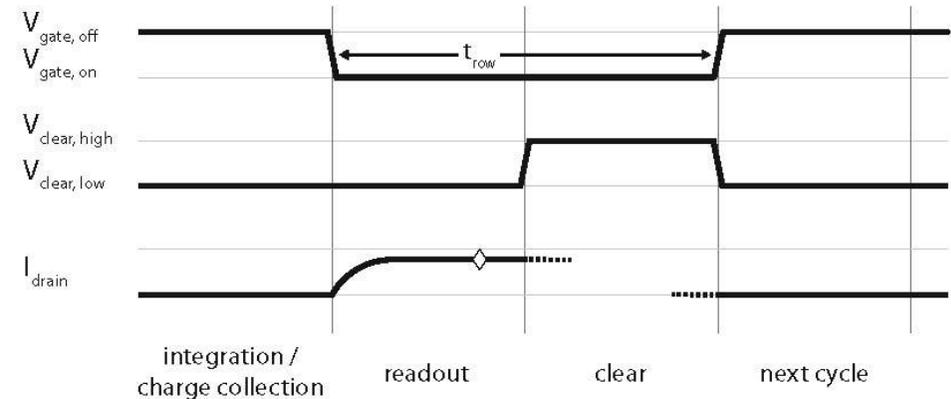


Homogeneous charge collection



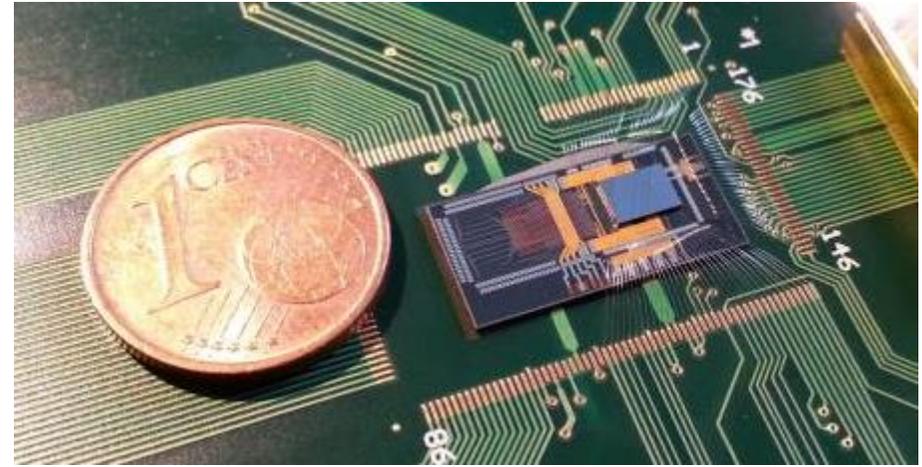
DEPFET Readout Speed

- DCD dynamic measurements
Readout speed with single sampling
- Belle II PXD frame readout: 20 μs
(50 KHz frame rate)
- Read-clear cycle: **100 ns**
(768 rows, 4 fold readout)

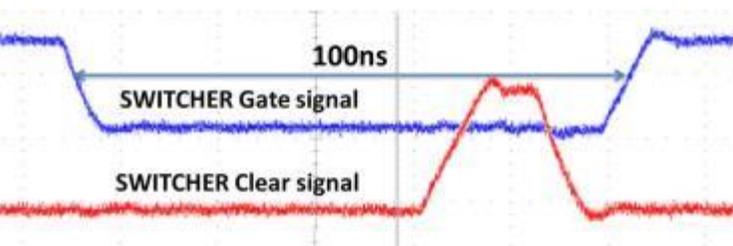


Long drain lines ~ 60 pF parasitic capacitance

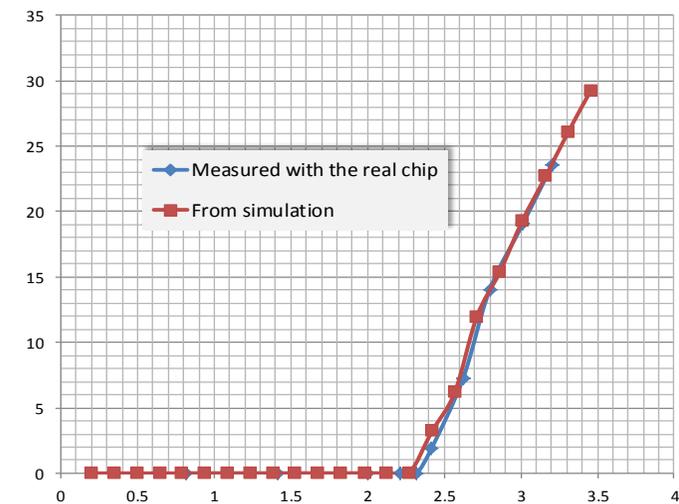
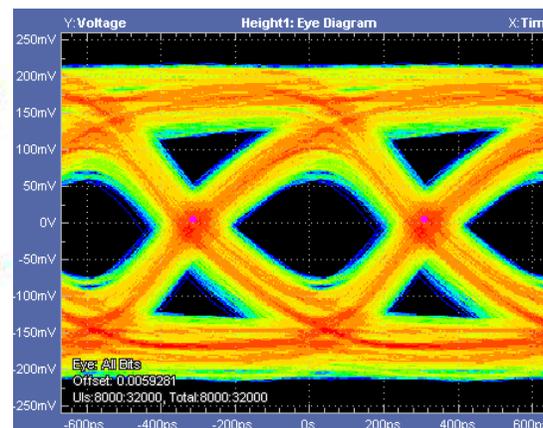
- Functionality tests
 - High speed link
 - Configuration and communication with DCD
 - Data processing
- Switcher output sequences



Steering Signal Output

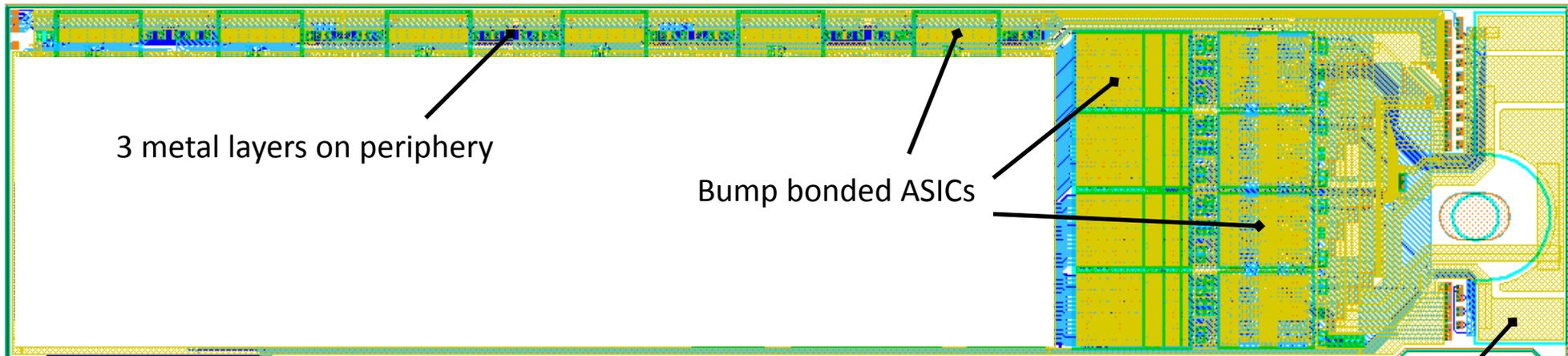
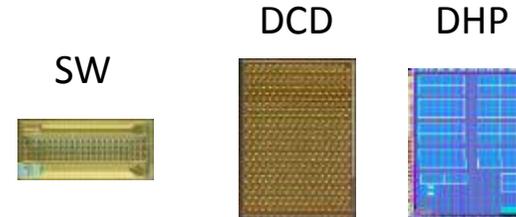


Eye Diagram after 15m Cable



Electric Multichip Module (EMCM)

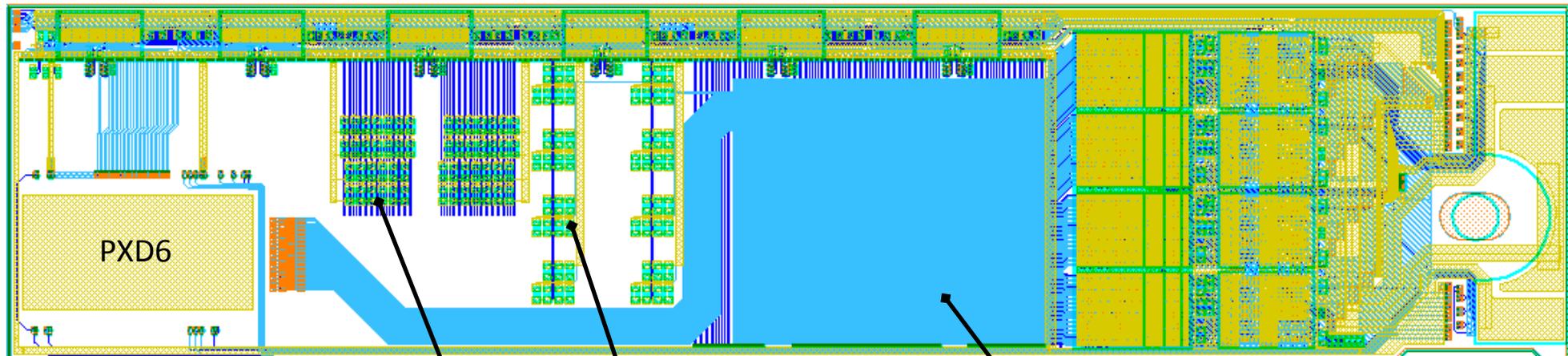
E-MCM: Everything but the DEPFET
Electrically active prototype of a half ladder



4 layer kapton cable attached and wire bonded to Si-Module for I/O and power

Electric Multichip Module (EMCM)

E-MCM: Everything but the DEPFET
Electrically active prototype of a half ladder

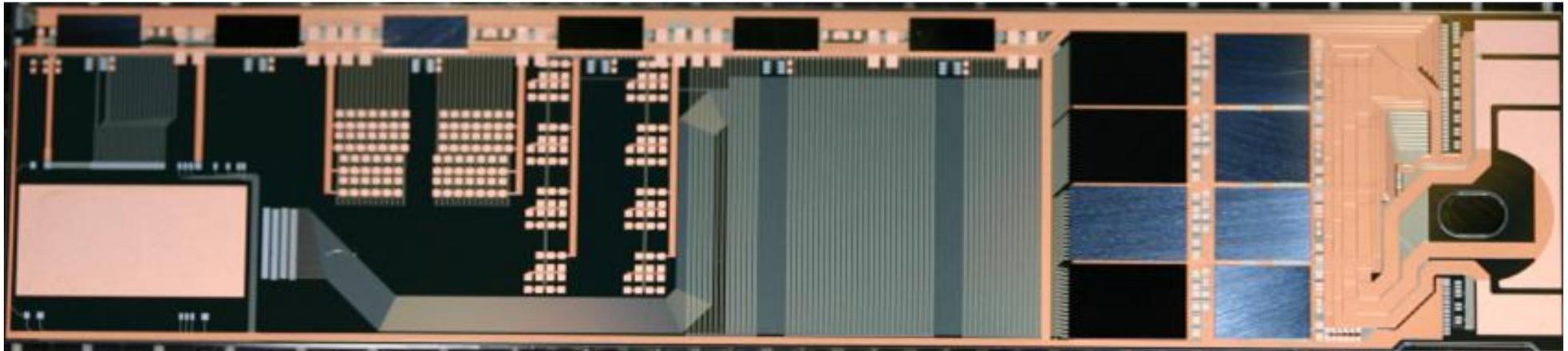


Capacitors for SW tests
Circuitry for DEPFET emulation
Long drain lines to DCD

- Study and characterization of routing and electronic components
- Understanding of the technological feasibility of the 3-metal layers
- Practice flip-chipping and off-module interconnections

E-MCM in reality

→ Modules produced, tested, ASICs flip chipped and Kapton attached



Electrical Properties under investigation

Beam tests

- **DEPFET PXD6 extensively tested over the last campaigns**
120 GeV pions at CERN-SPS
1-5 GeV electrons at DESY
Magnetic field
- **Sensor properties**
Charge collection homogeneity, operating points, efficiency, angular scans
Various pixel sizes, gate lengths, clear structures, drift regions and pixel designs
- **System related aspects**
Power supply prototypes
DHH and ONSEN readout

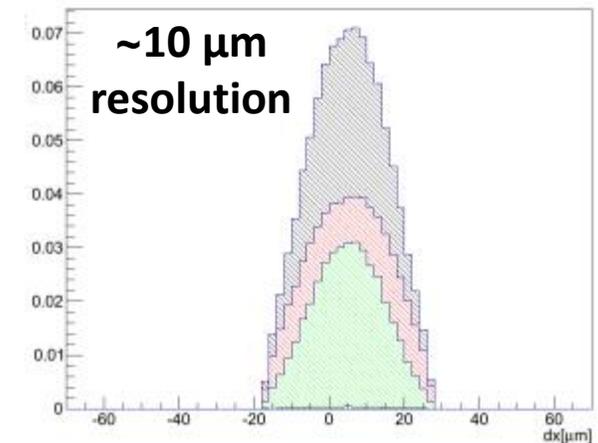
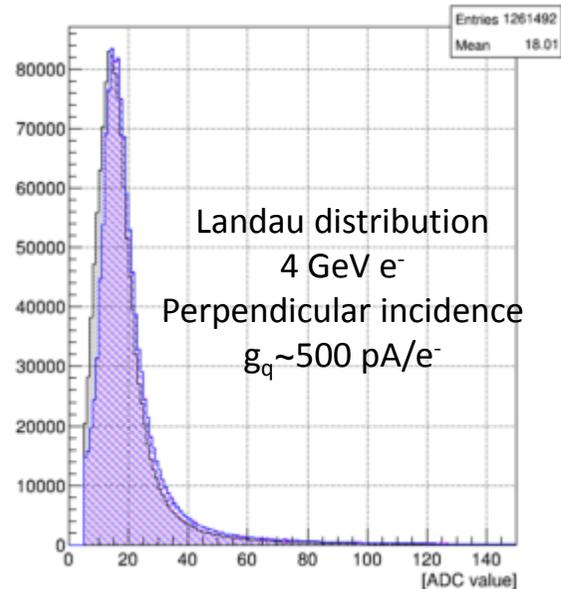
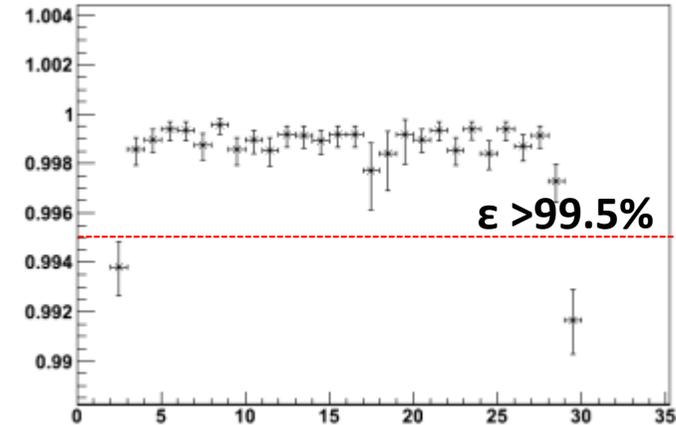
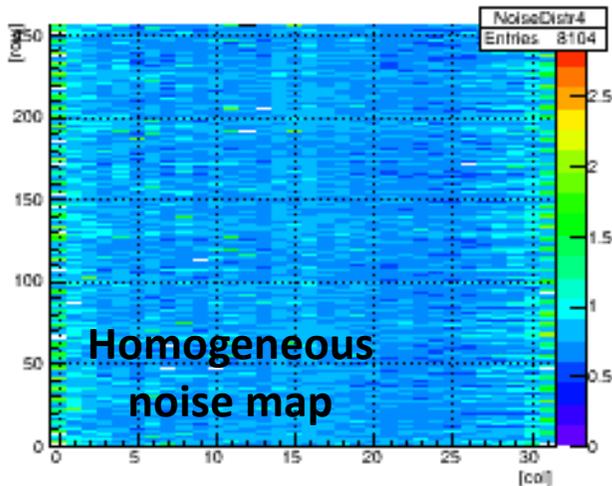
Here, just an appetizer

PXD6 Belle II design

Thin 50 μm sensor

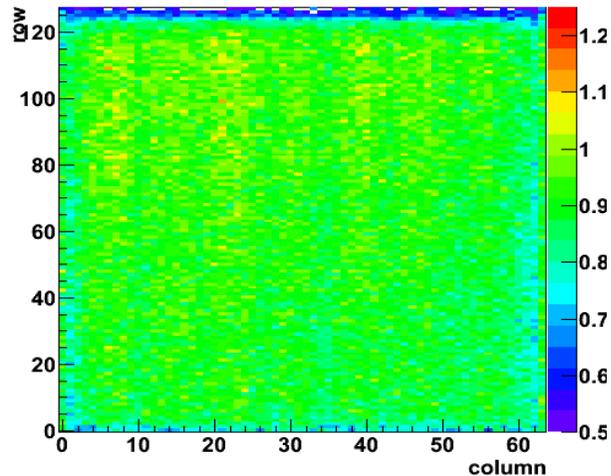
Pitch 50x75 μm^2

Targeted speed readout

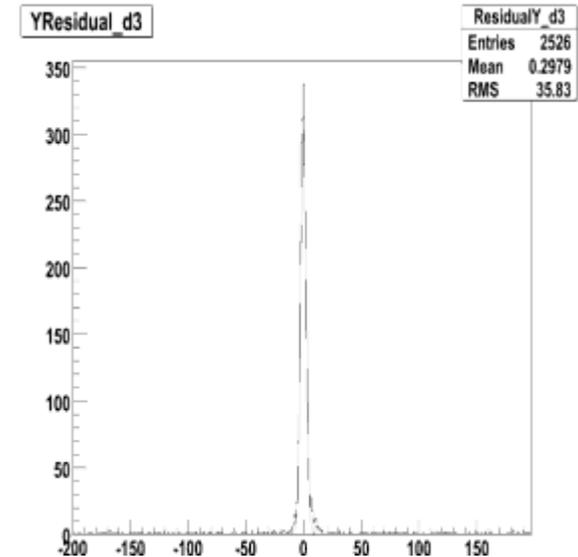
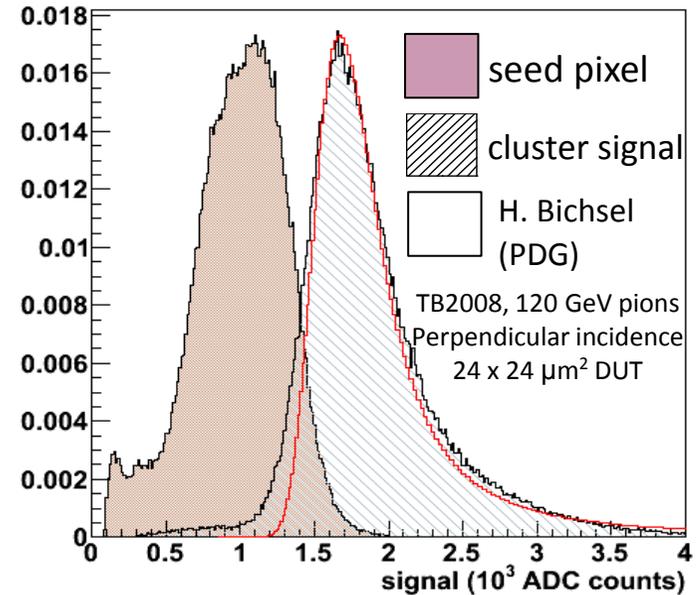


Prove of principle demonstrated in many test beam campaigns over the past years

Gain map: Deviation from average seed signal

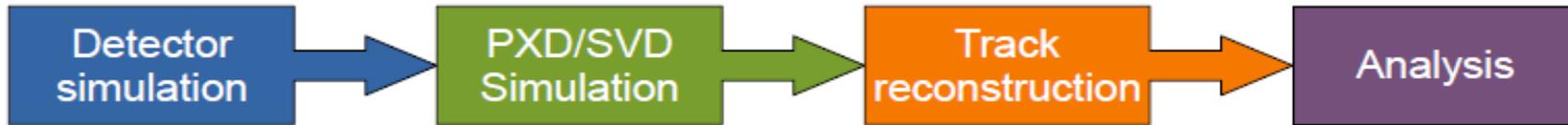


- 64x128, 24x24x450 μm^3 CCG, 6 μm (TB2008)
 $g_q = 363 \text{ pA/e}^-$
- 64x256, 20x20x450 μm^3 CCG, 5 μm (TB2009)
 $g_q \sim 650 \text{ pA/e}^-$
- Resolution $\sigma \sim 1 \mu\text{m}$, 20x20x450 μm^3 , analog readout with charge interpolation



ILC Design

→ Extensively tested

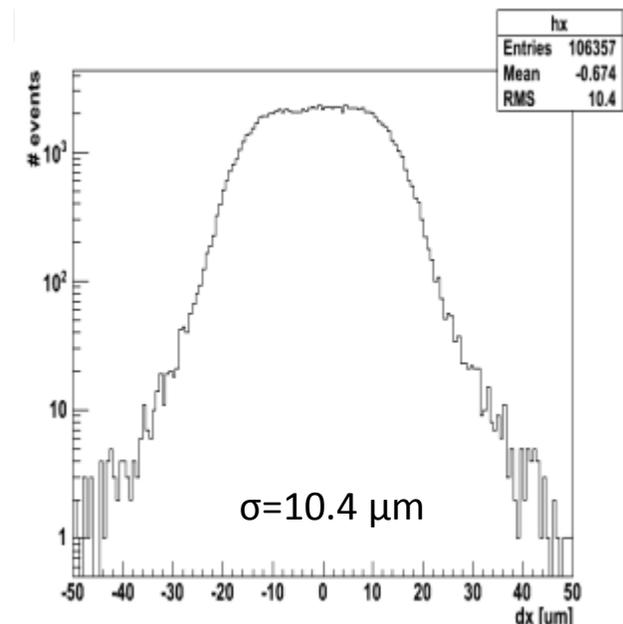
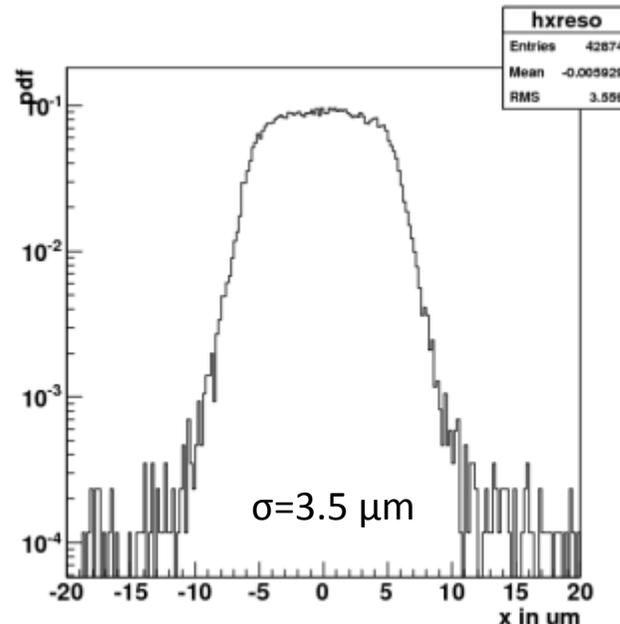
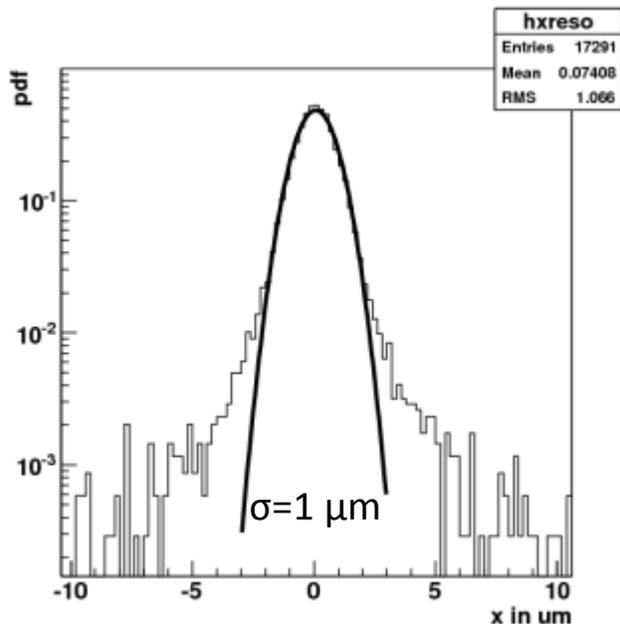
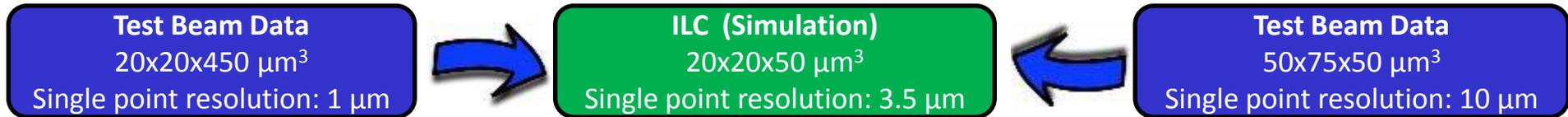


Particle gun (single event)
EvtGen (physics event)
Mokka geometry

Ionization points
Signal points
Electronic noise
Digitization and clustering

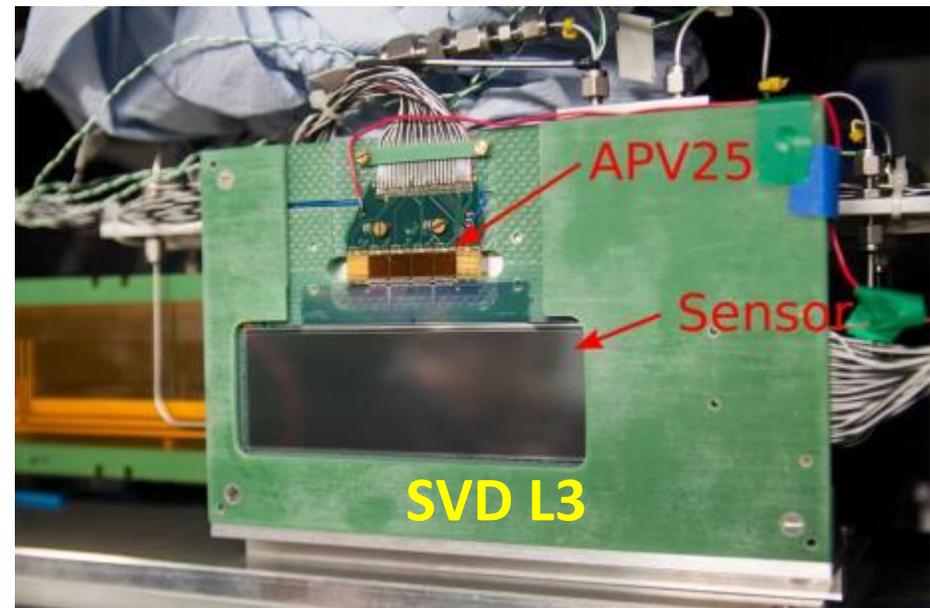
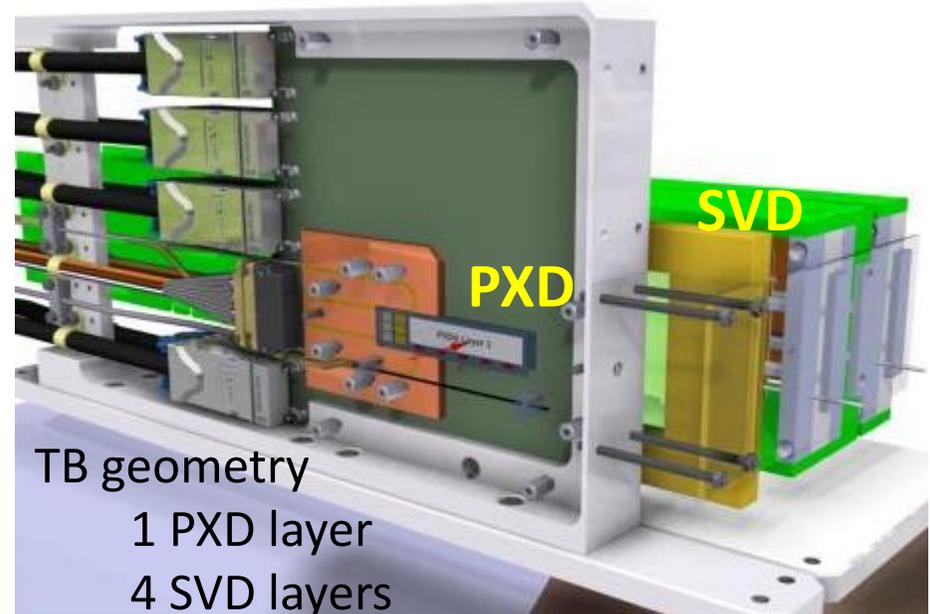
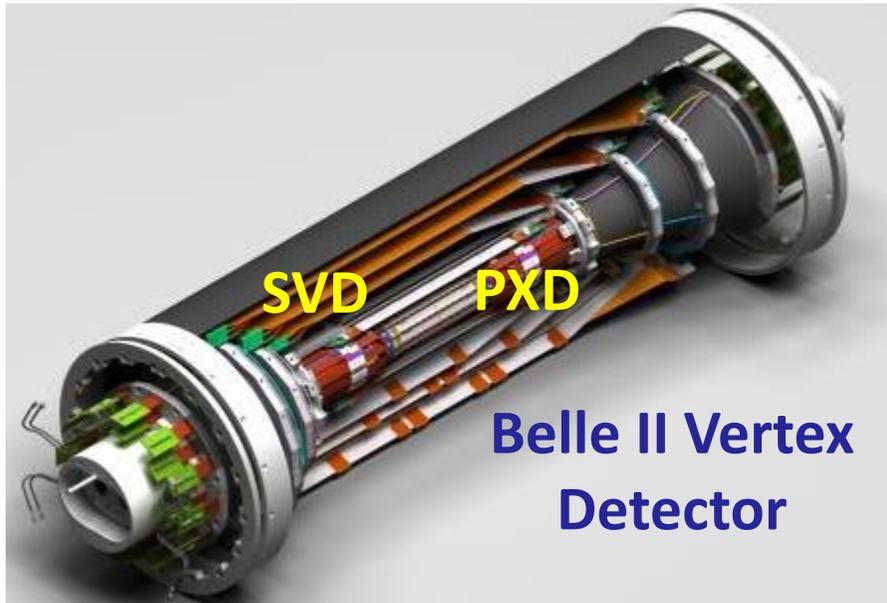
Marlin tracking
PXD+SVD+CDC

Physics channels

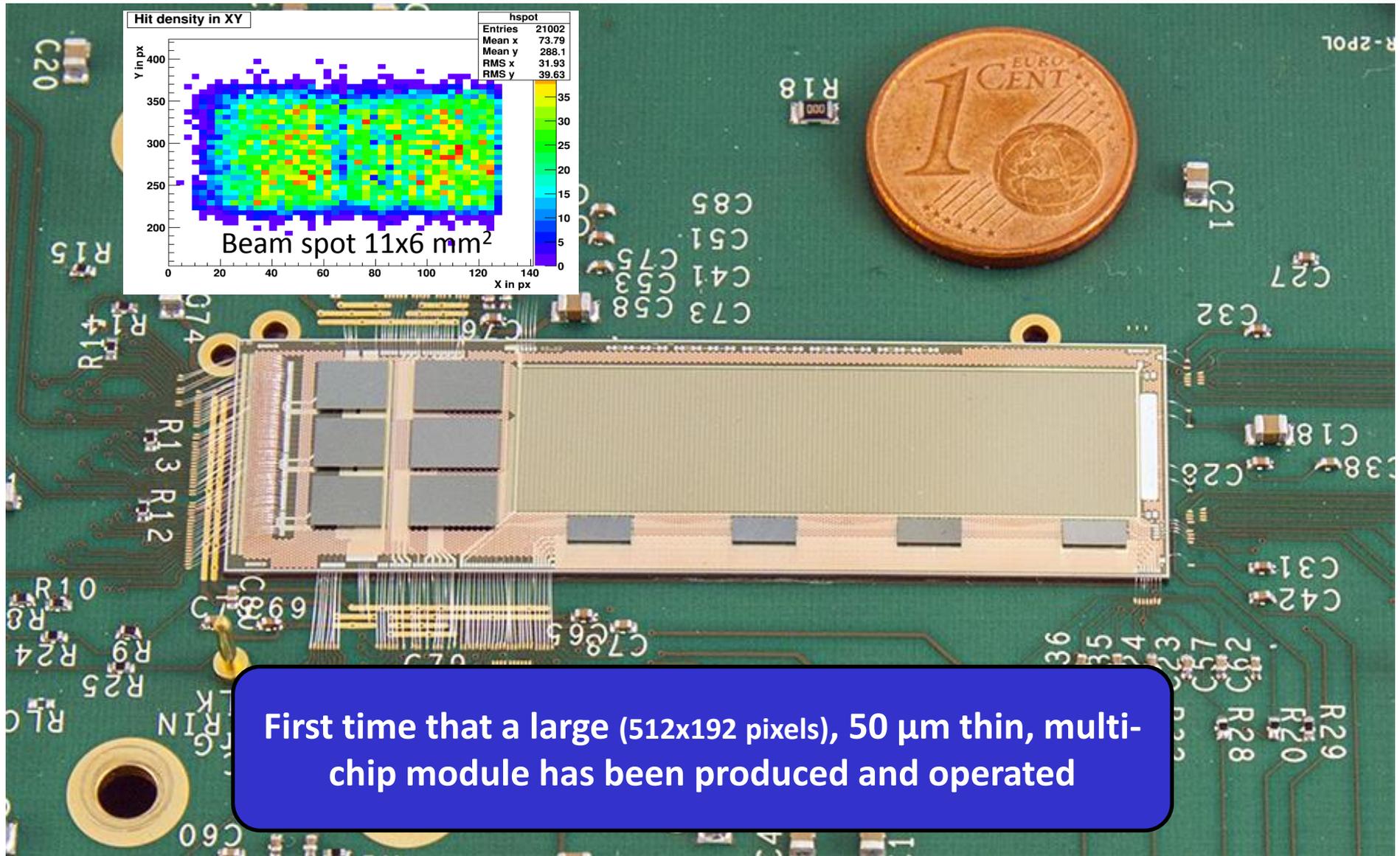


- PXD+SVD common test beam in January 2014
 - Small sector of the close to final prototype detectors and ASICs
PXD half ladder + 4 SVD single module layers
 - Readout using the complete DAQ chain
 - CO₂ cooling, slow control, environmental sensors
 - Alignment, tracking algorithms, ROI with B=1 Tesla
-
- **Goal: System integration test**

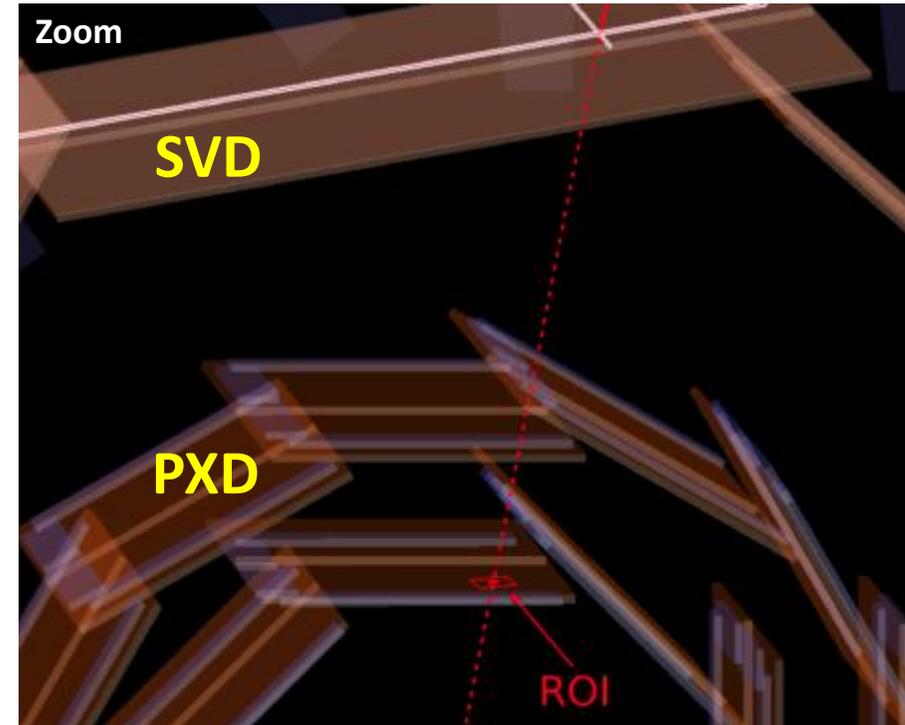
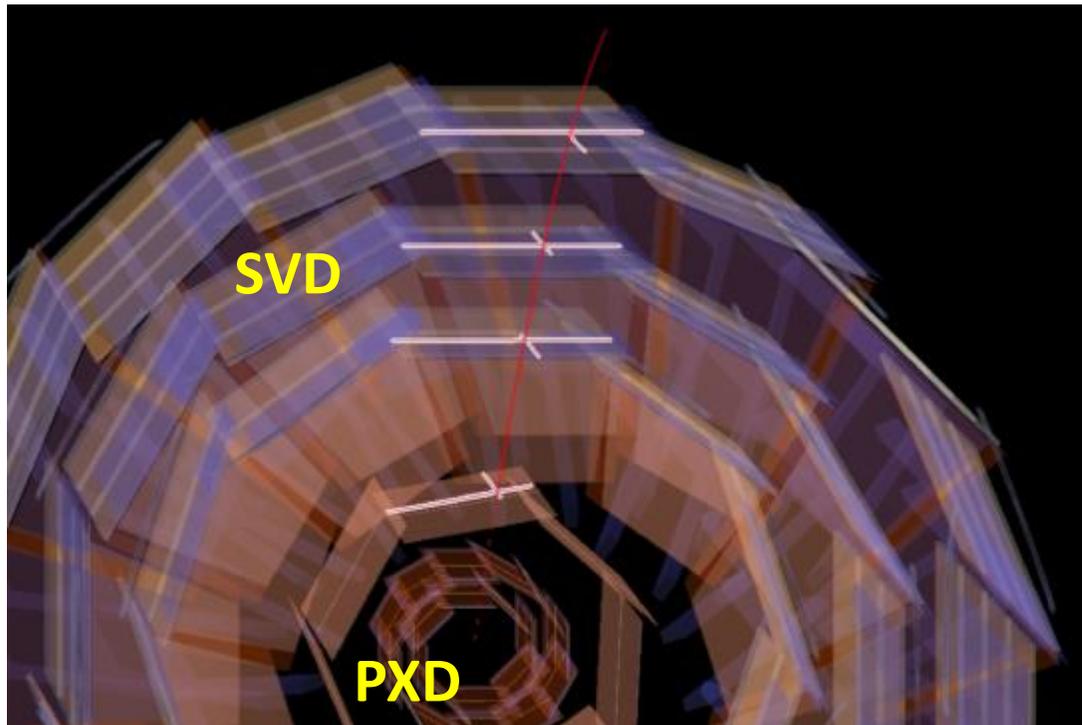
Test Beam Setup



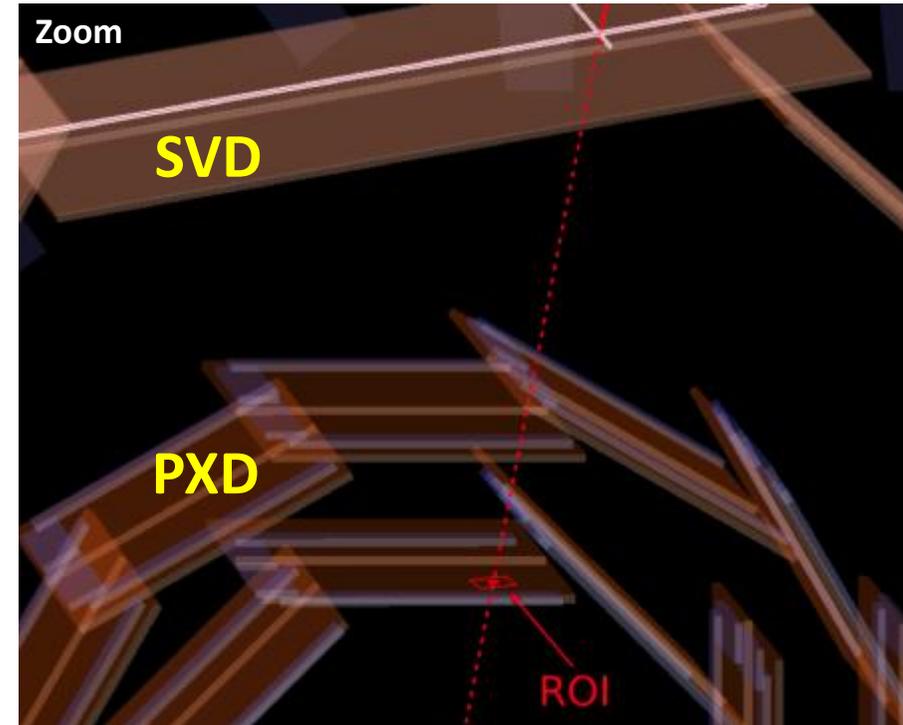
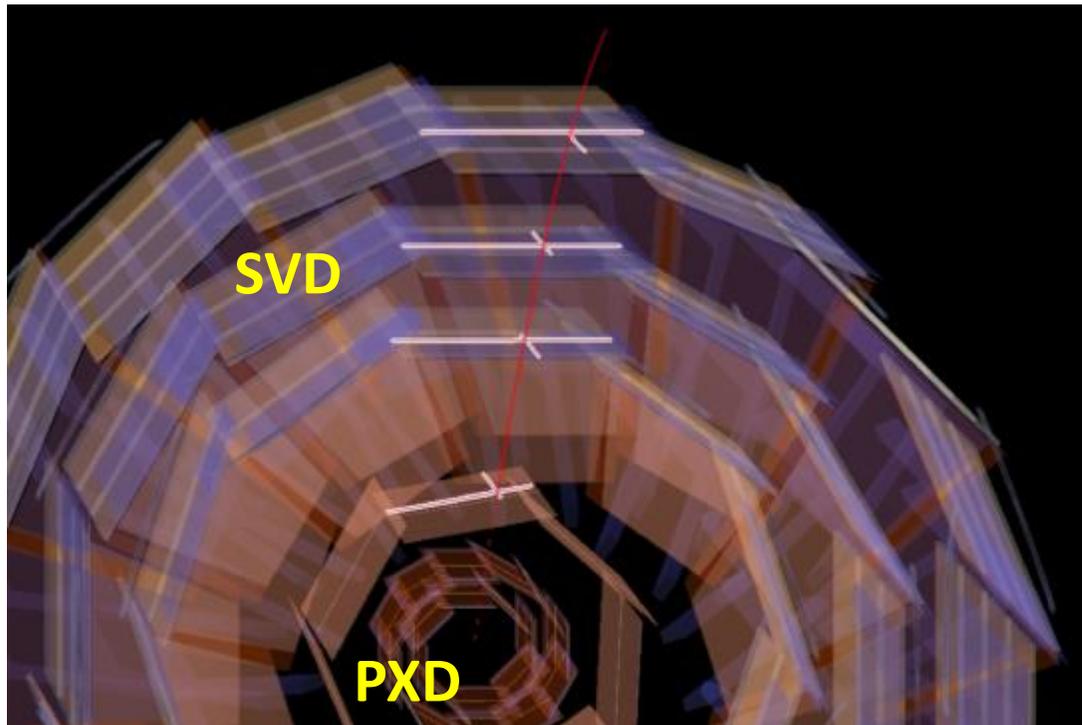
Thin Multichip Module



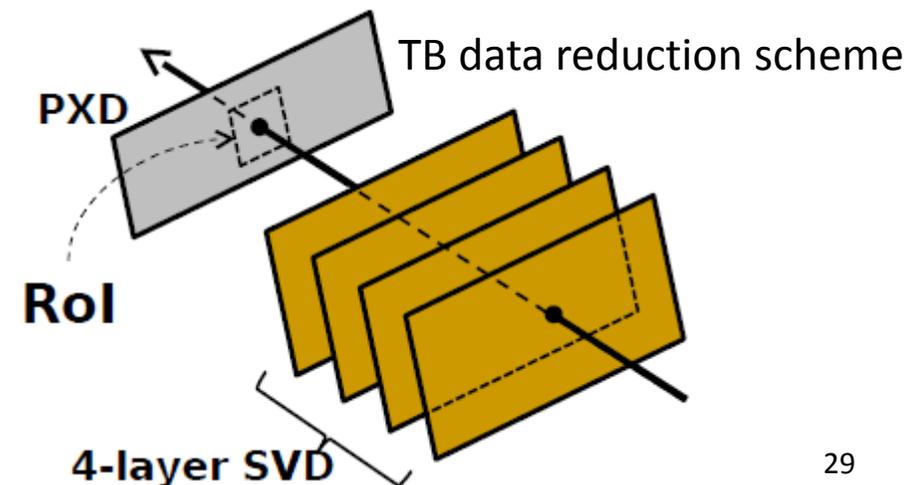
First time that a large (512x192 pixels), 50 μm thin, multi-chip module has been produced and operated

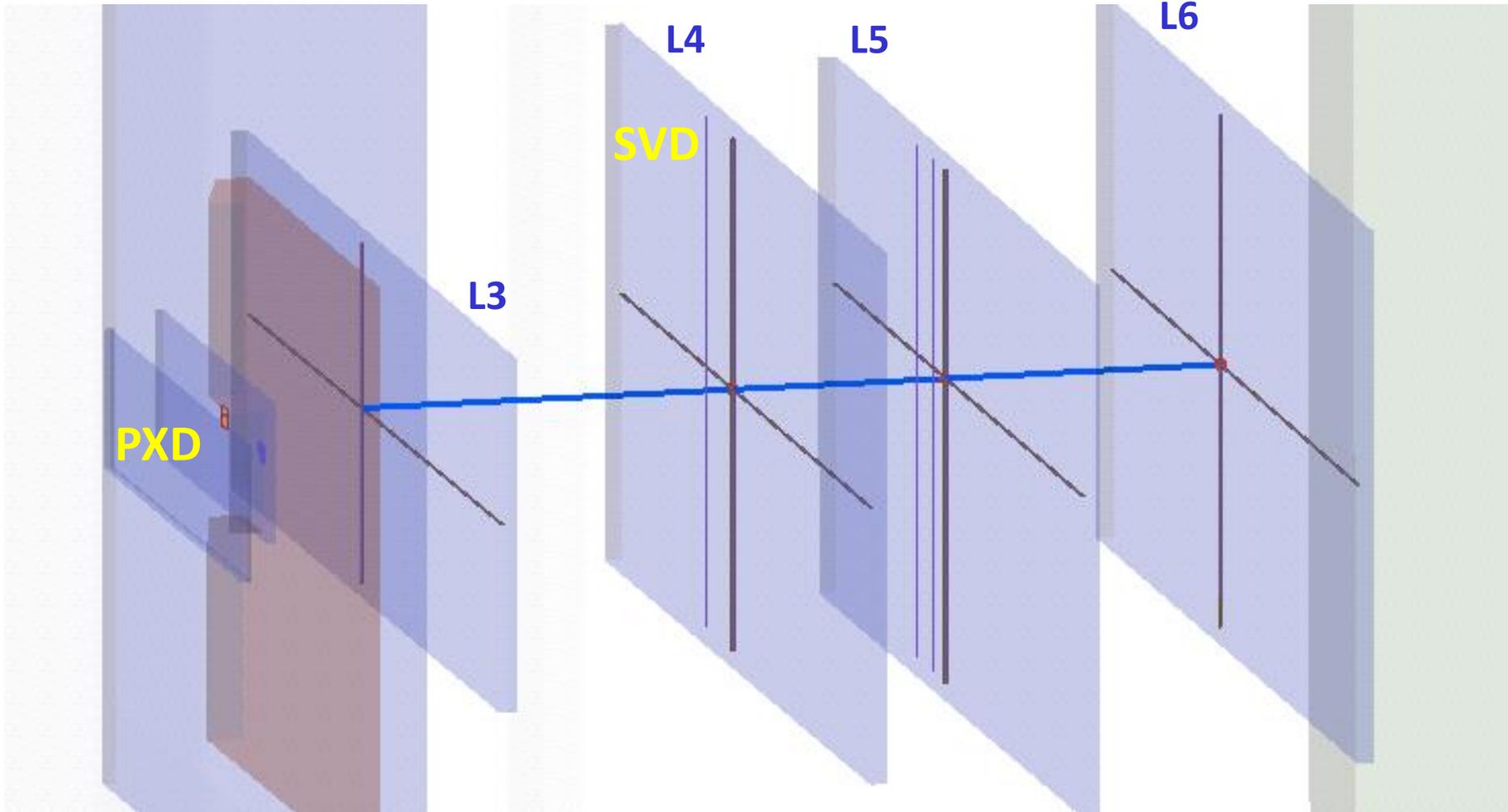


- Expected maximum occupancy 3%
- Total data rate >20 GB/s after zero suppression
- Data reduction (factor ≥ 10) needed for data storage
- Solution: region of interest (ROI) by track extrapolation from the outer detectors

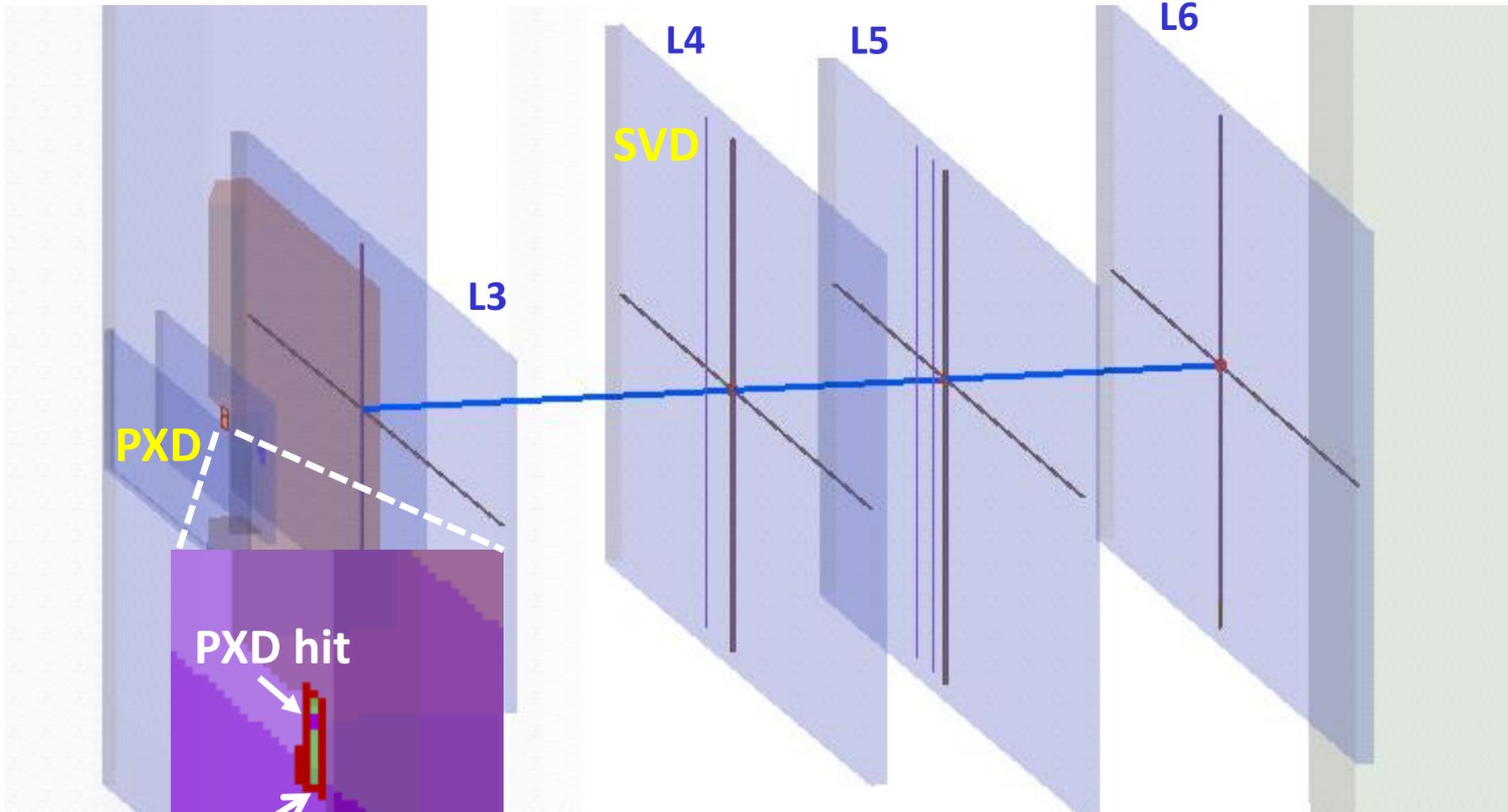


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- Tracking using SVD and PXD ROI extrapolation



- Tracking using SVD and PXD ROI extrapolation
↳ Hit found inside the PXD ROI
- Factor 6 data reduction → Further investigations ongoing

Telescope

SVD

PXD

Telescope

- 5 GeV electron under 1 Tesla field
- SVD real data
- Track reconstruction
- PXD and telescope extrapolation

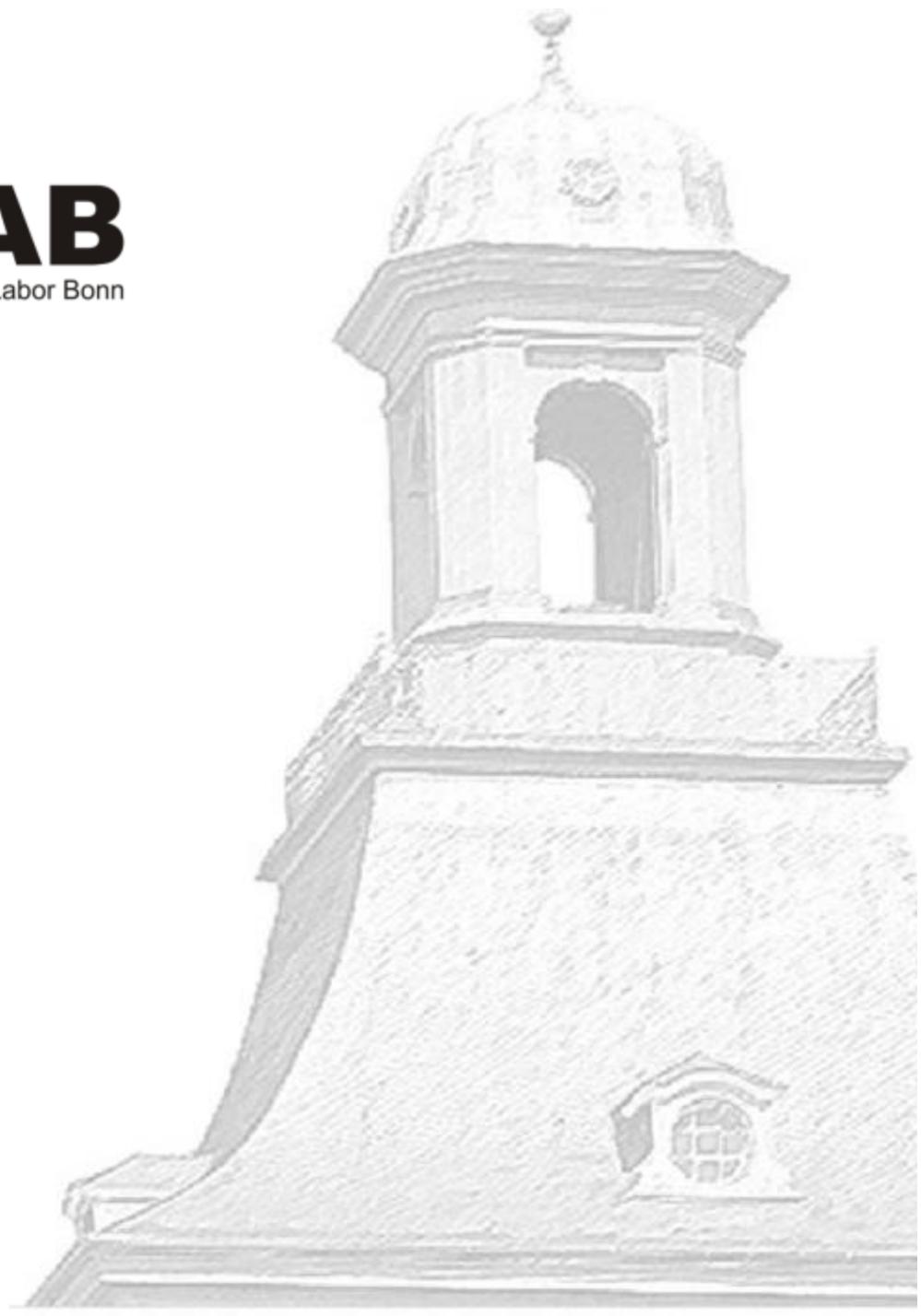
- The DEPFET Collaboration is developing ultra-transparent pixel sensors with integrated amplification
- The good performance of the DEPFET detector system in terms of SNR, spatial resolution, readout speed is demonstrated
- The Belle II PXD boosted the development of DEPFET detectors
 - Direct benefit towards the ILC-VXD project (ILD-VXD layer concept '*engineered*')
- Building a real system: Every detail (although not covered here) is being considered
 - Interconnection technologies, rad. hardness, cooling, mechanics, ... (see backup)

'DEPFET active pixel detectors for a future linear e^+e^- collider'.

M. Vos *et al.* arXiv:1212.2160



Thank you



- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link

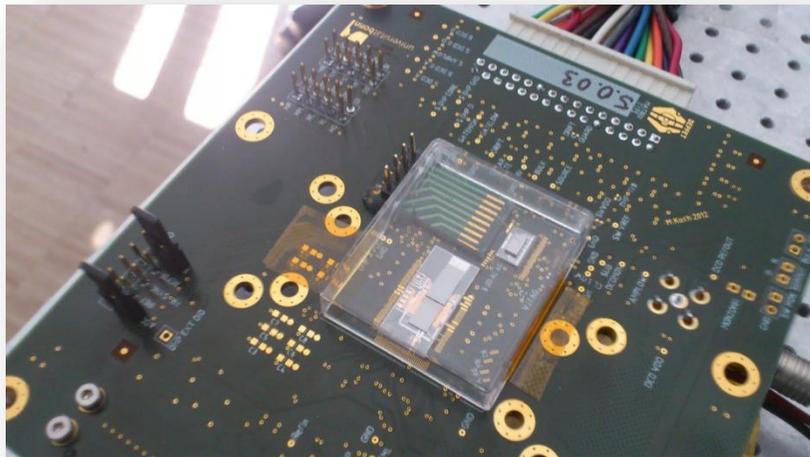
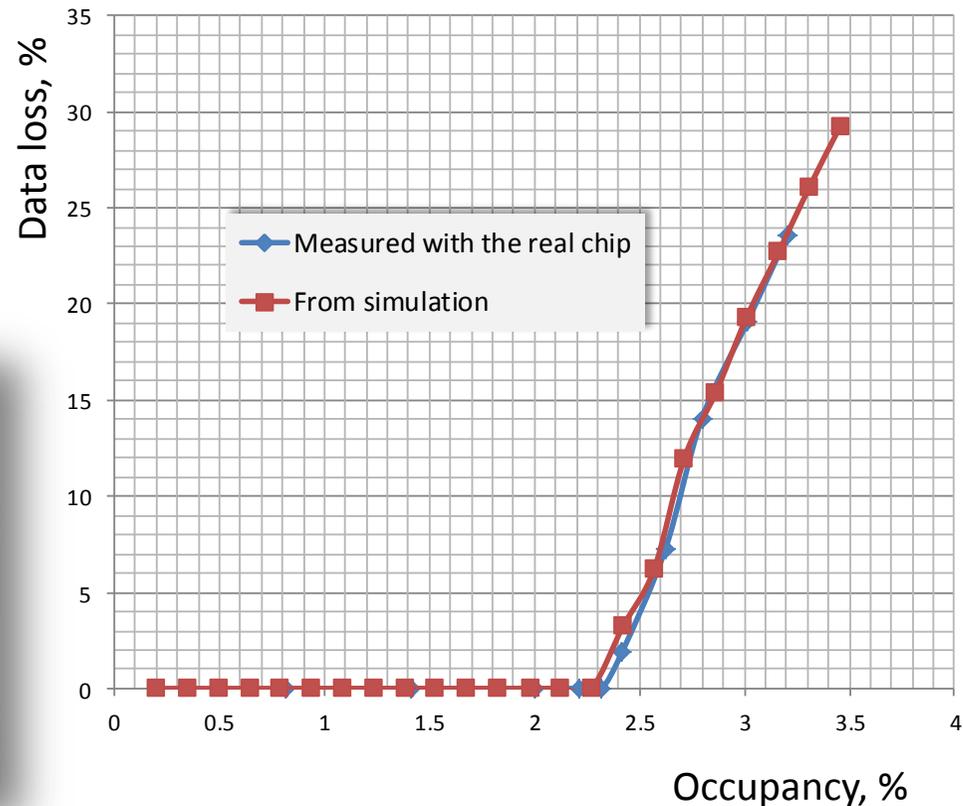


Photo of the hybrid 5 (without DEPFET matrix)

Un-triggered acquisition, DHP0.2 data loss characteristic as a function of the input data occupancy (C++ and real chip)



No data loss for the expected occupancy

- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link

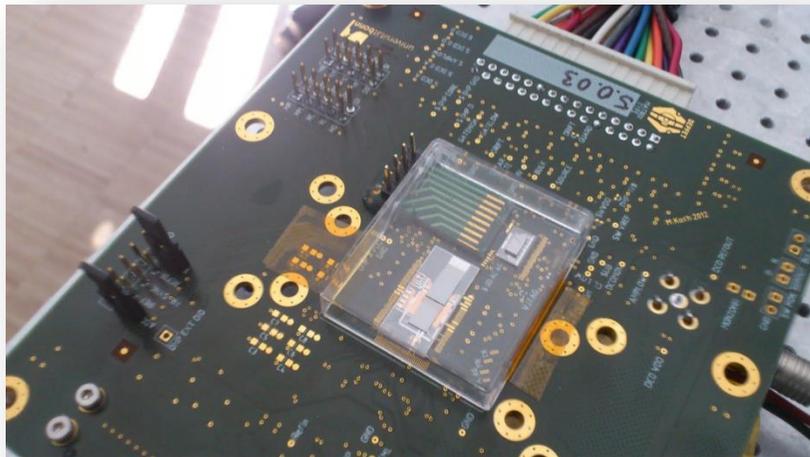
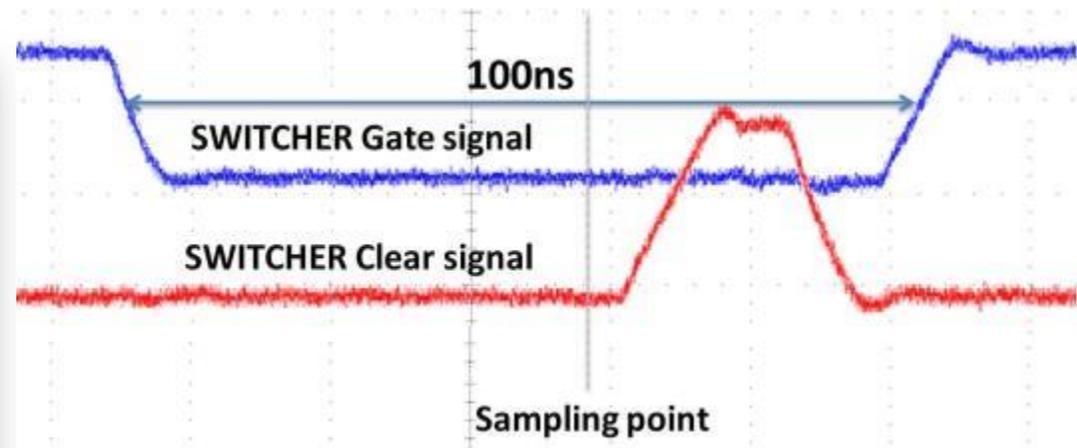
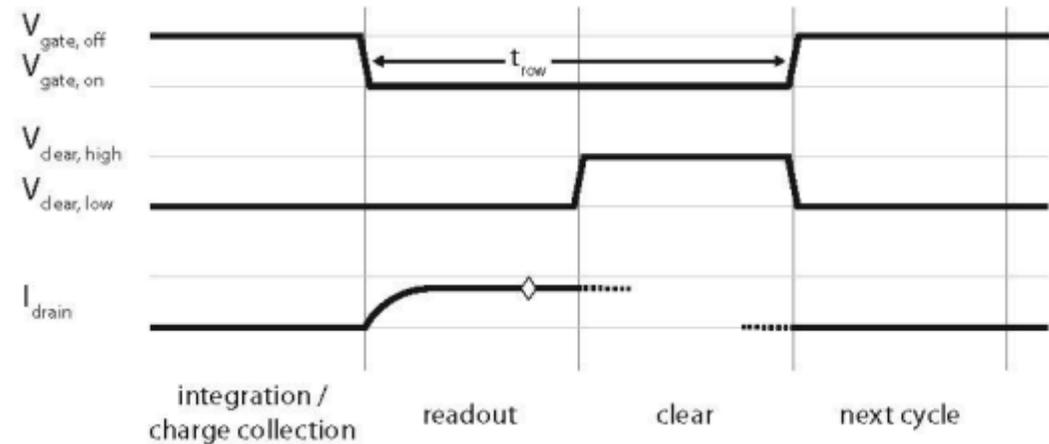


Photo of the hybrid 5 (without DEPFET matrix)



DHP can control the SwitcherB sequence

- Data processing
- SWITCHER sequencing
- **Inter-chip communication**
- Serial link

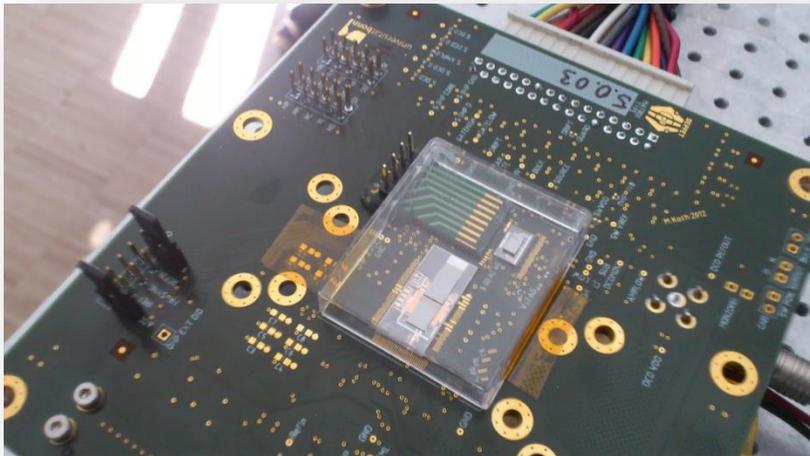
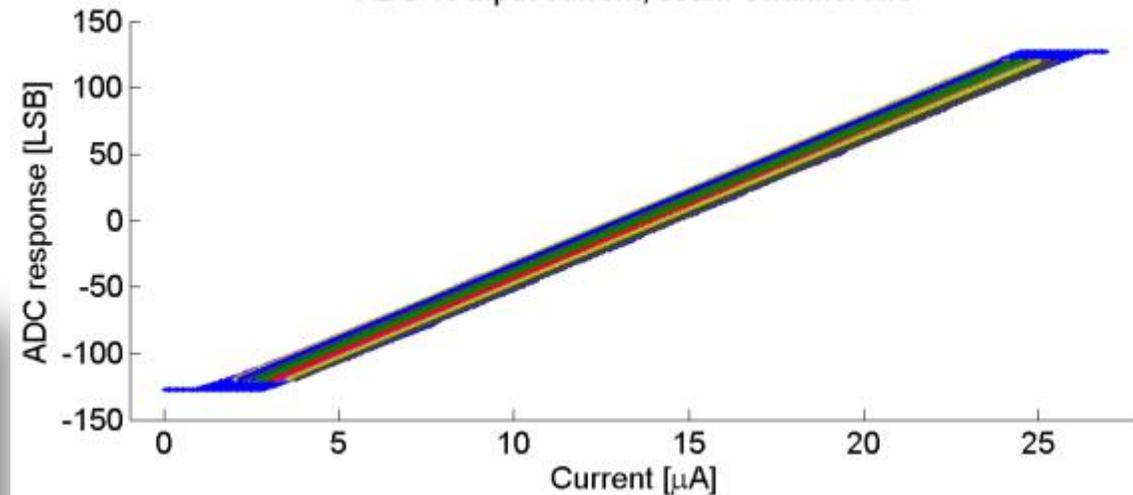


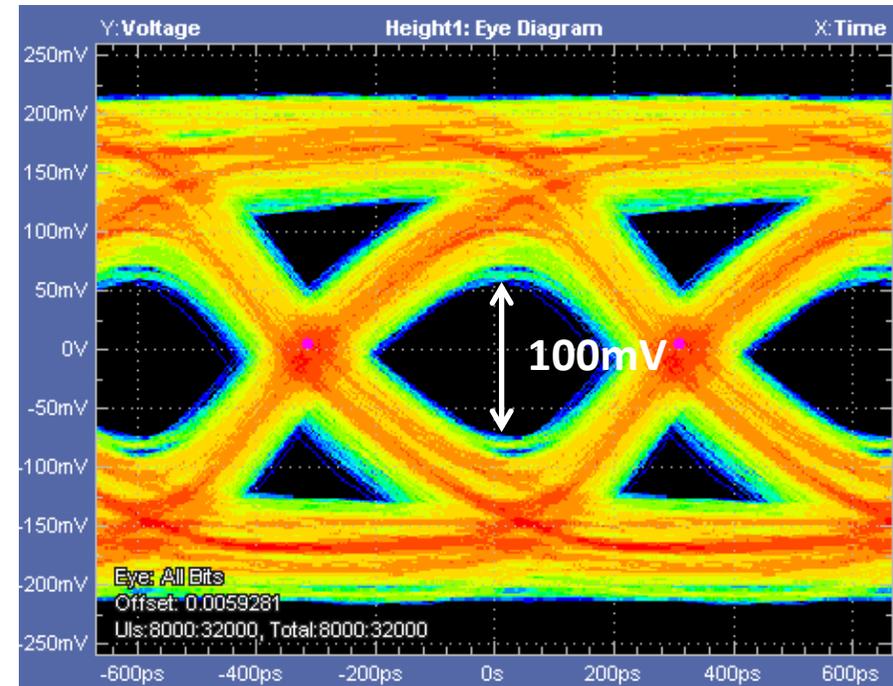
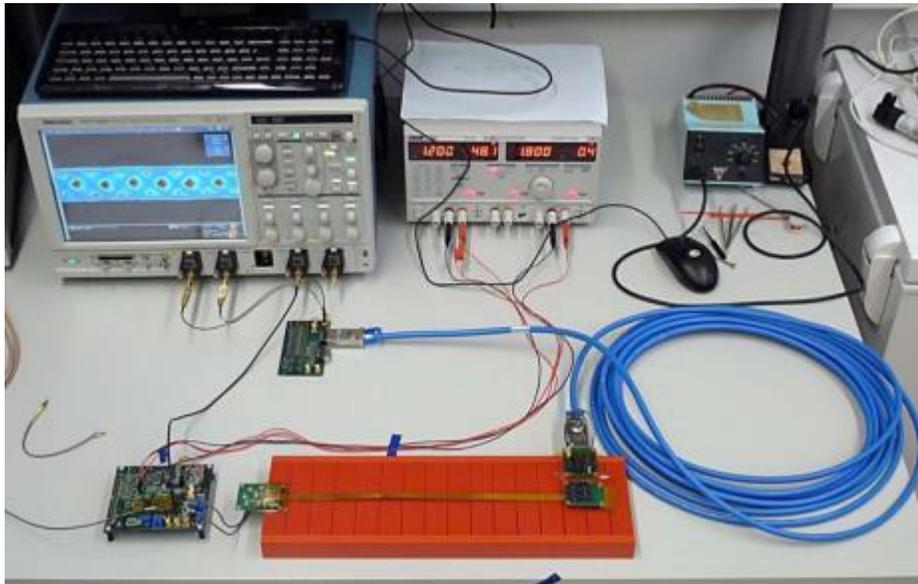
Photo of the hybrid 5 (without DEPFET matrix)

ADC vs Input current, all channels



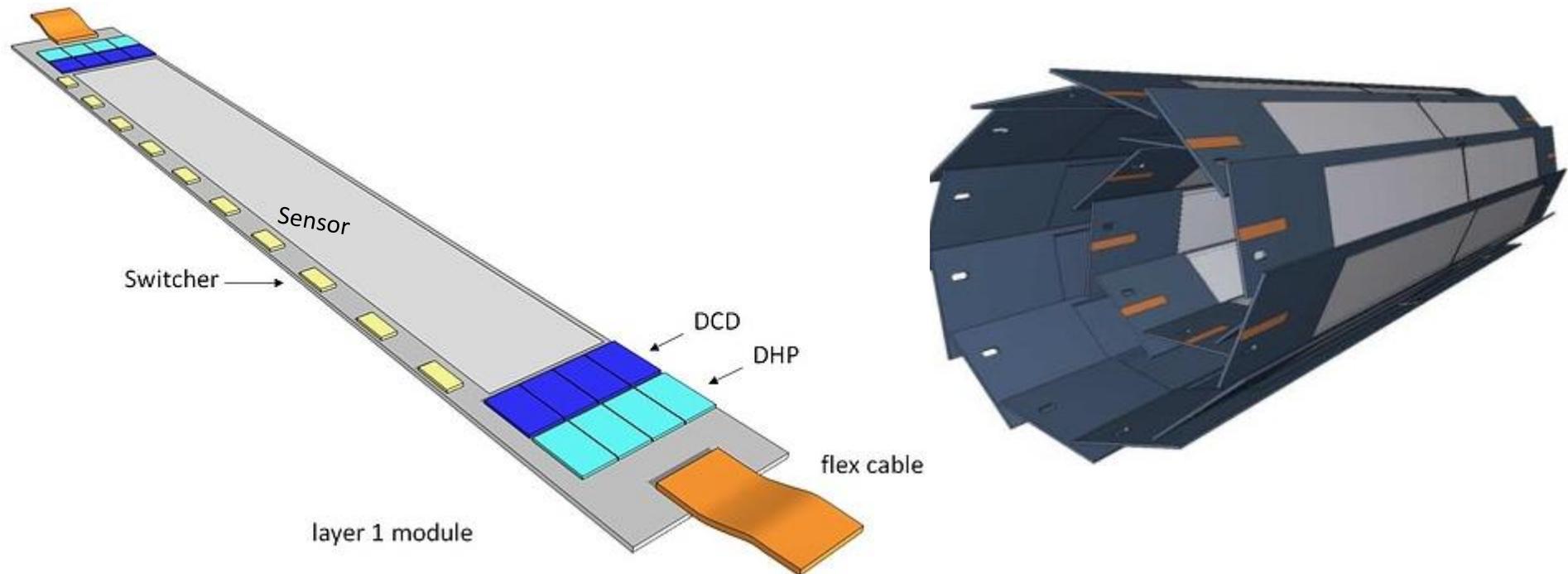
DCDB and DHP can communicate at full speed

- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link

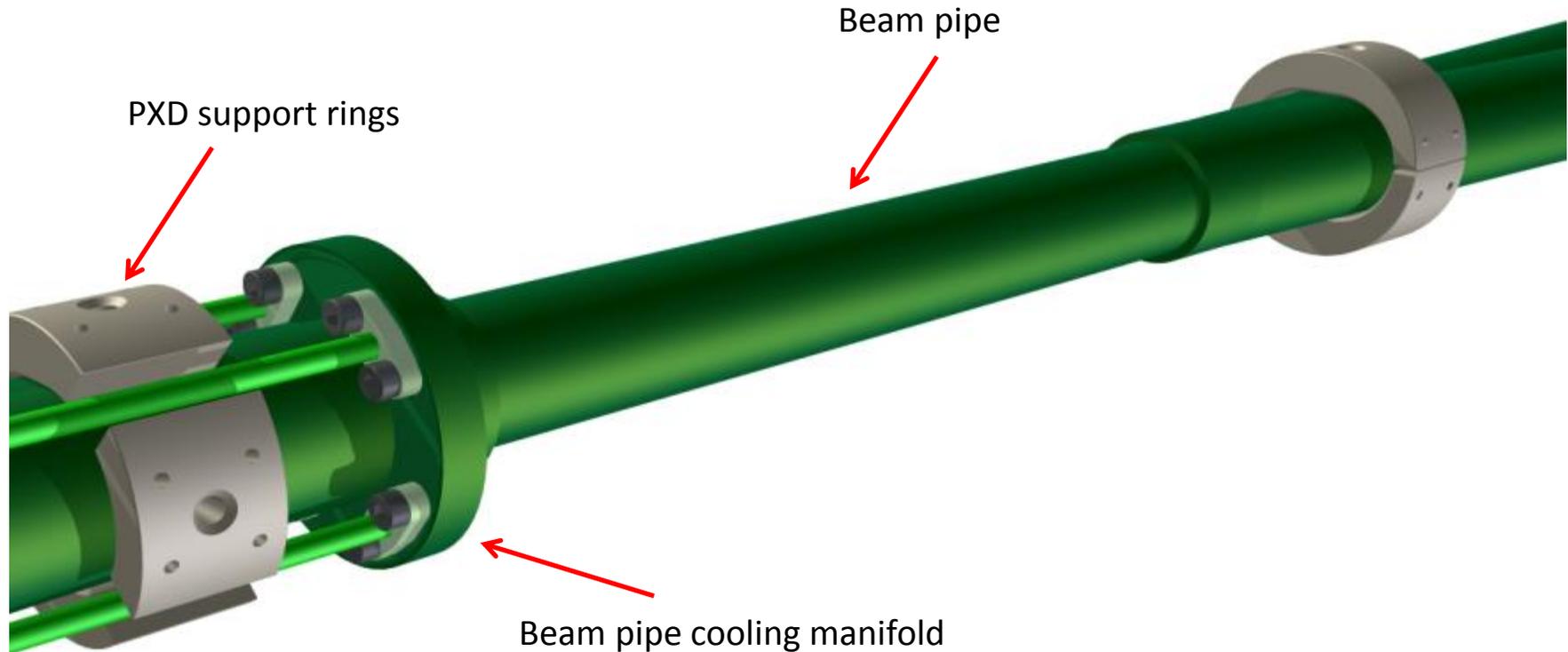


**Irradiated (100 Mrad) DHPT 0.1, can drive
15 m of Infiniband cable**

Remember the DEPFET detector unit, the ladder and how the ladders are assembled to form a vertex detector:

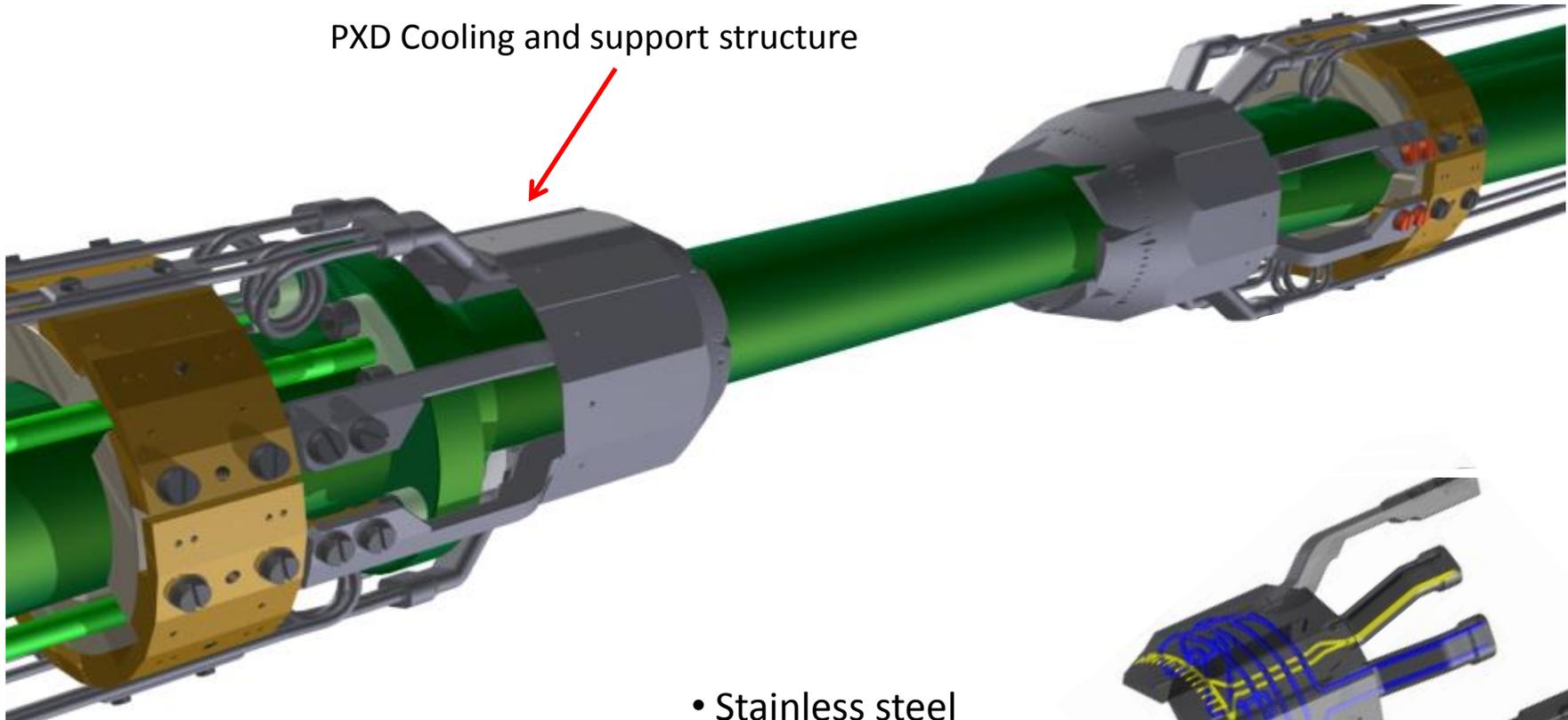


- The material budget must be minimal, no active cooling is allowed inside the acceptance
- The major amount of heat is dissipated in the readout chips, at both ends of the ladder
- The most straightforward solution:
 - Massive structures outside the acceptance to cool down the readout chips
 - The center of the ladder must be cooled using cold air

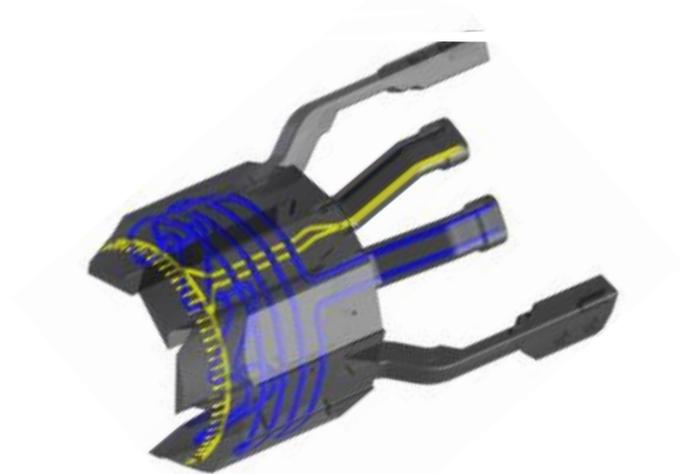


- Thinner pipe
- Smaller radius
- Lighter materials

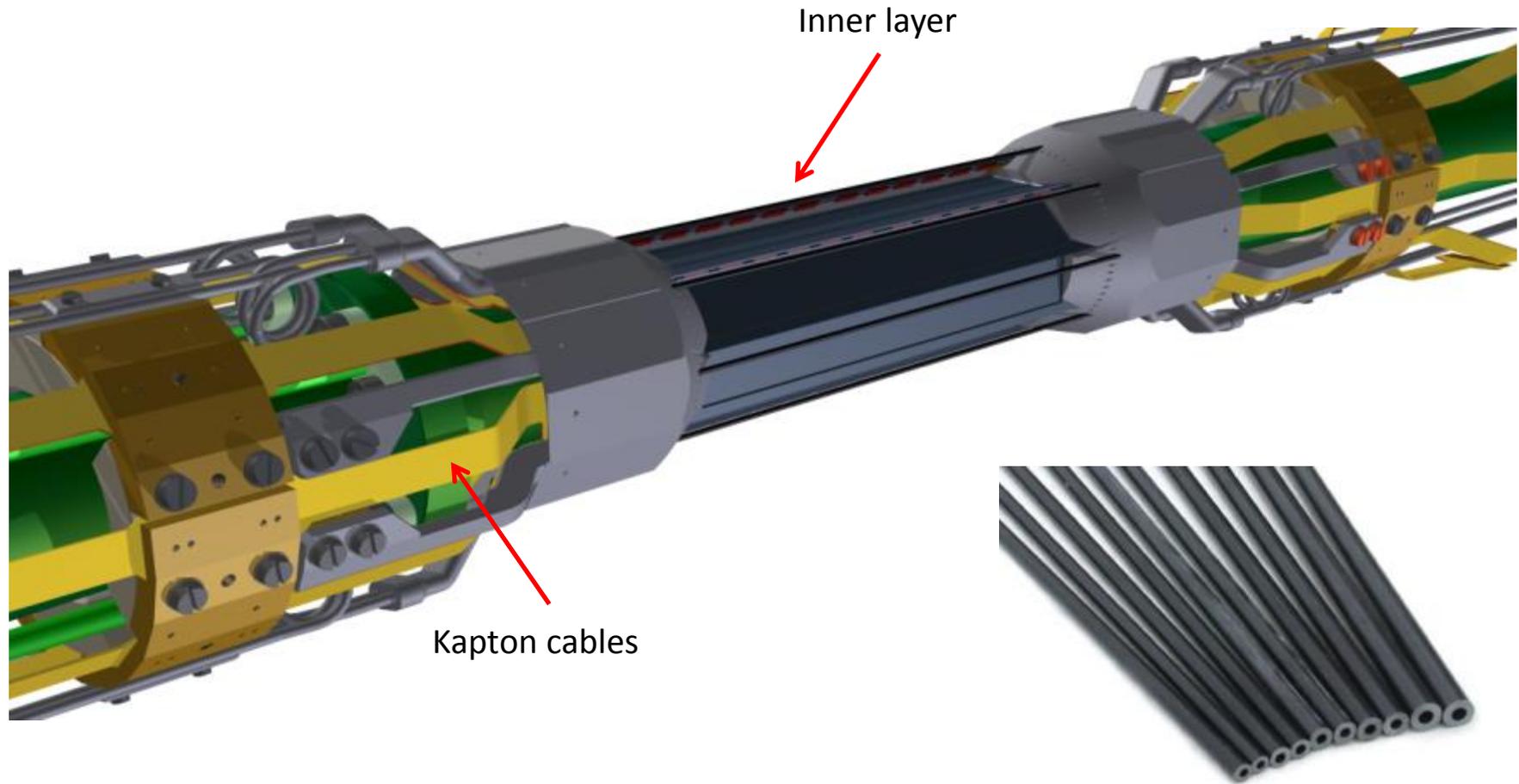
PXD Cooling and support structure



- Stainless steel
- Fast sintering
- Coolant: CO₂

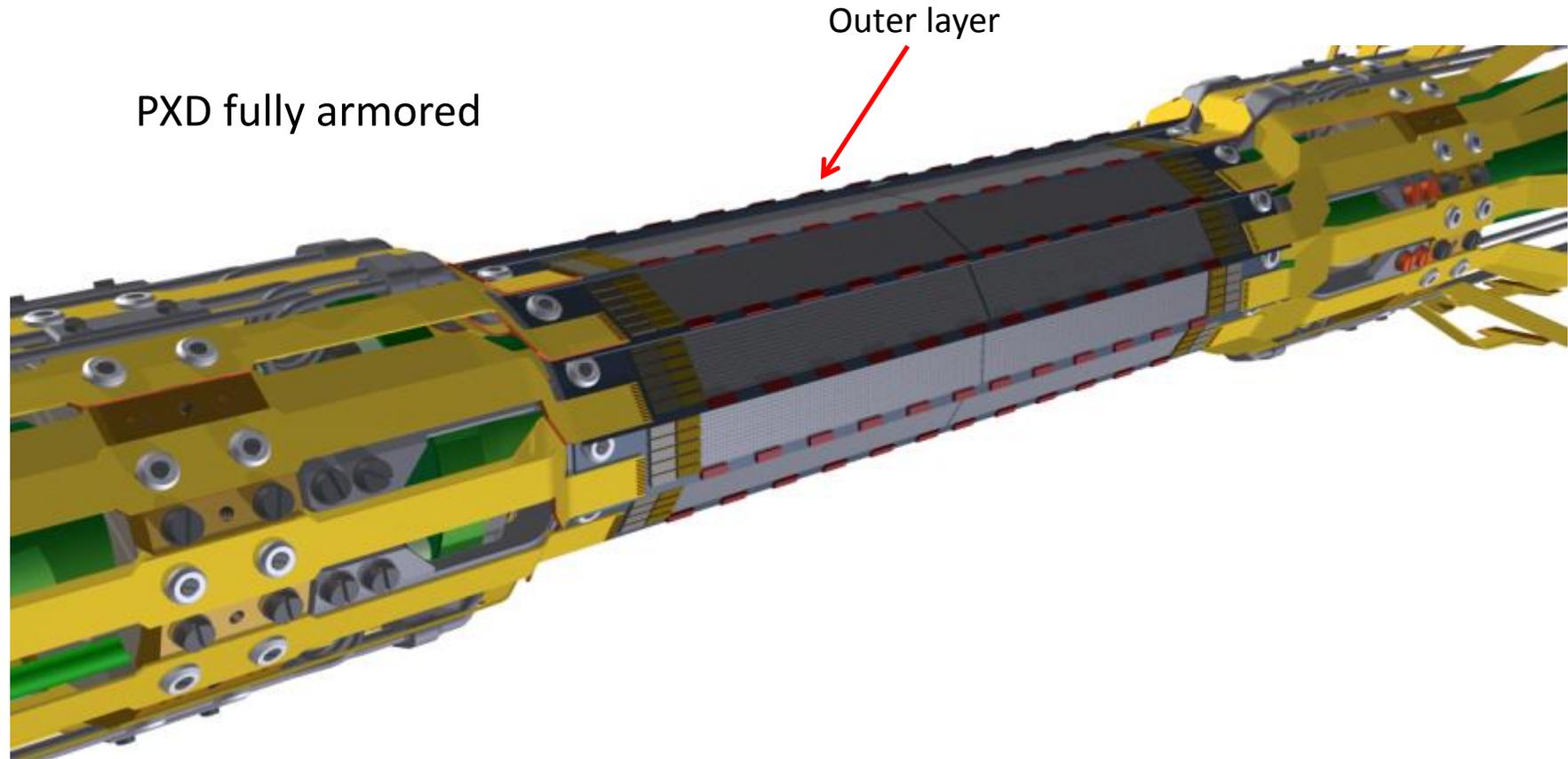


Blue: CO₂ capillaries
Yellow: Air channels

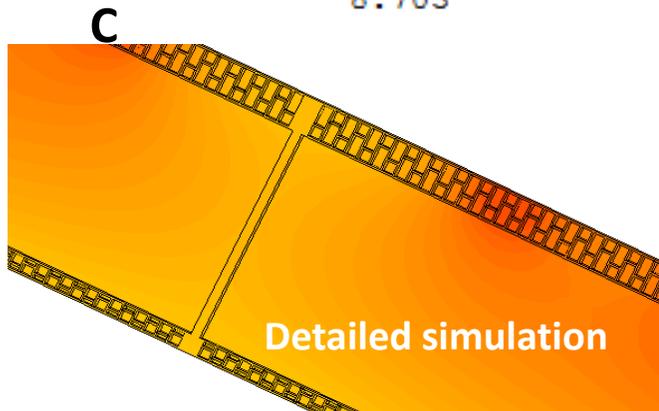
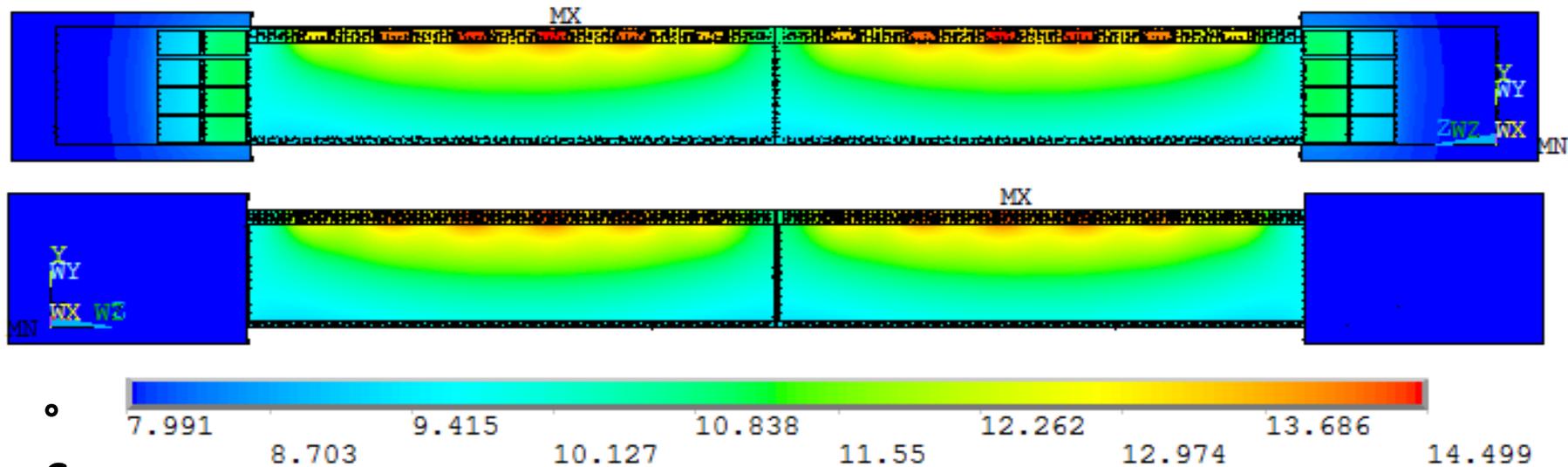


Inner layer close to the IP (14mm)

Additional carbon fibers capillaries to cool the Switchers, if needed (not tested yet)



- Low material budget cooling
 - Massive structures outside the acceptance to cool down the readout chips
 - The center of the ladder rely on cold air



Set of reasonable
environment conditions

$$T_{\text{env}} = -5^{\circ}\text{C}$$
$$T_{\text{cb}} = 8^{\circ}\text{C}$$

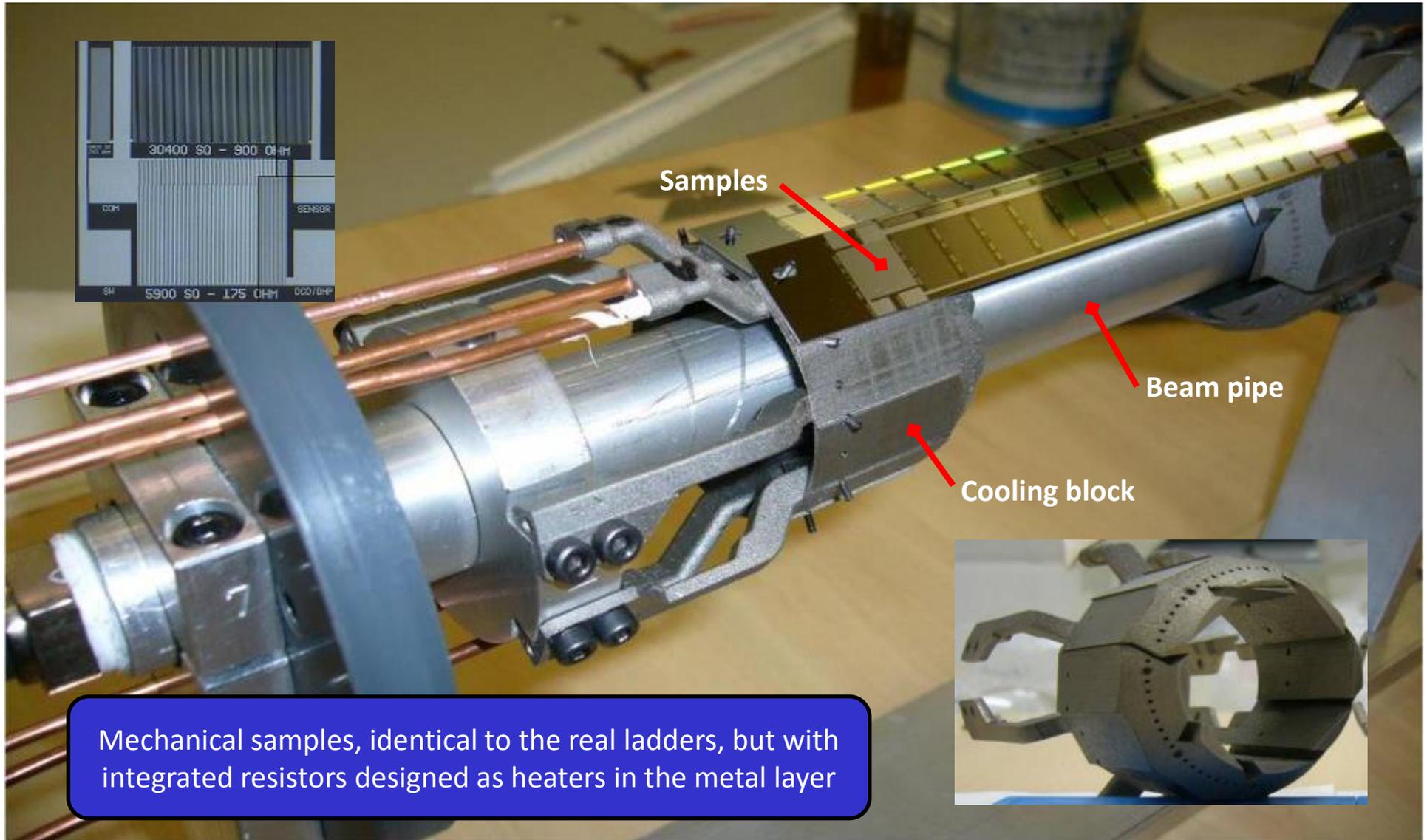


$$T_{\text{SENSORmax}} = 14^{\circ}\text{C}$$
$$\Delta T = 4.7^{\circ}\text{C}$$

$$\Delta L < 3\mu\text{m}$$

Just a gentle air flow (2 m/s) is enough to decrease and homogenize the temperature distribution

Measurements with mockup



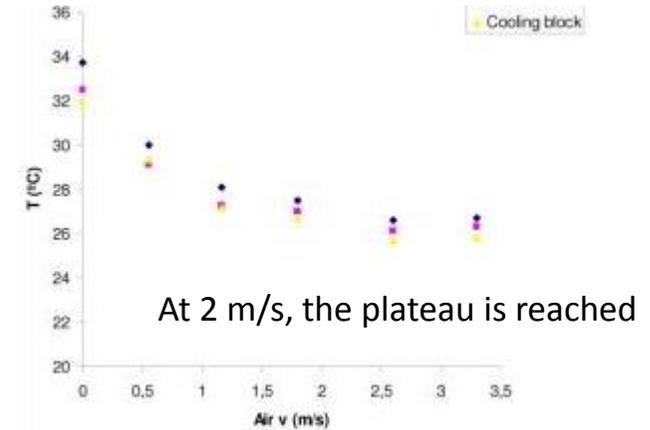
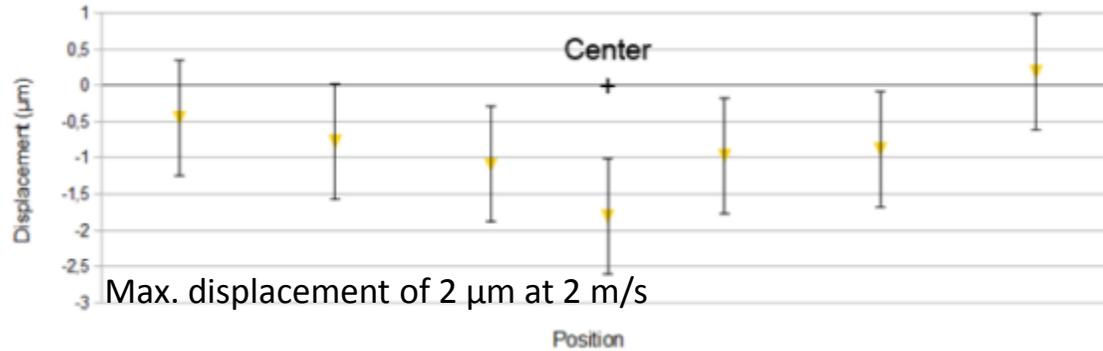
Samples

Beam pipe

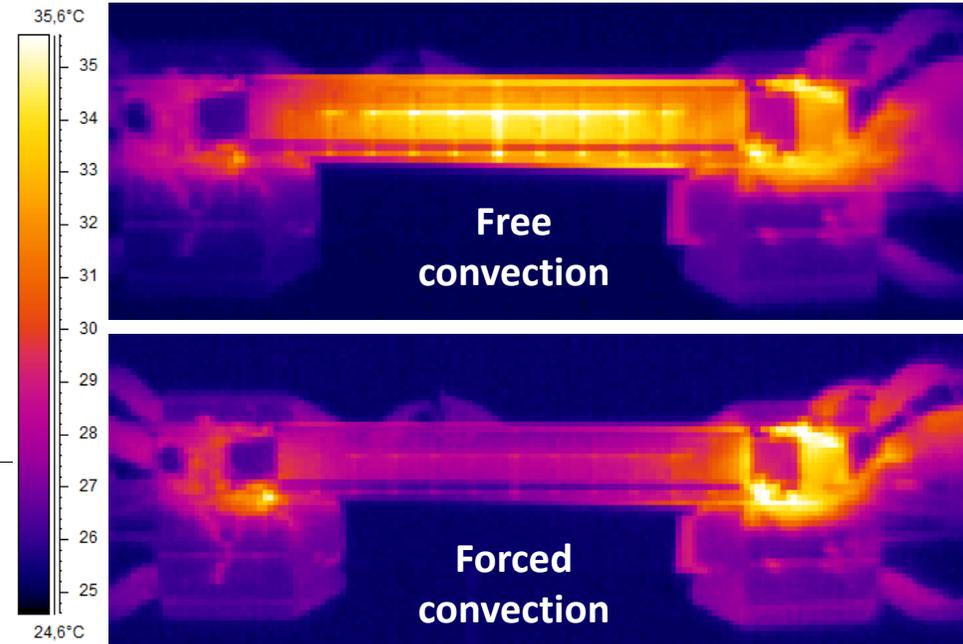
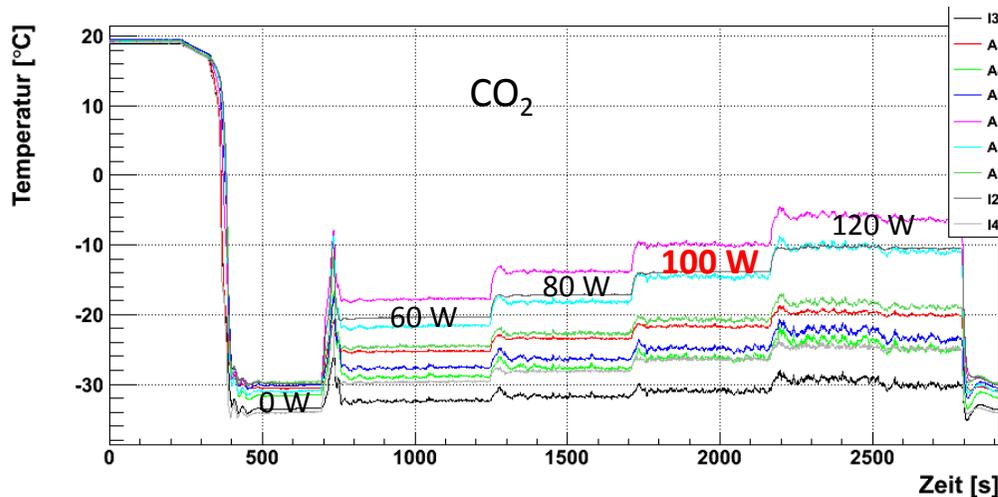
Cooling block

Mechanical samples, identical to the real ladders, but with integrated resistors designed as heaters in the metal layer

Thermo-mechanical measurements



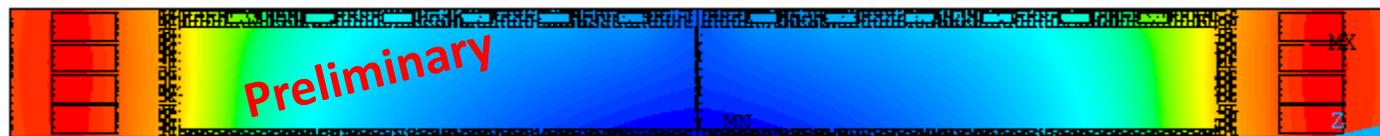
- Stainless steel
- Fast sintering
- Blue: CO₂ capillaries
- Yellow: Air channels



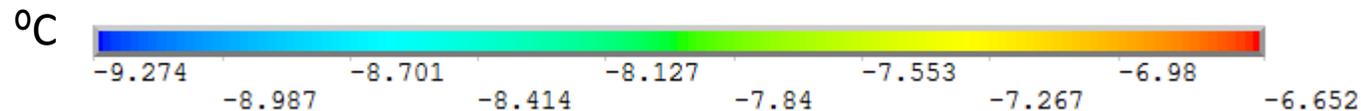
Cooling proof of principle

↘ Naïve approach using the XFEL hands-on:

- The power consumptions are weighted accordingly to the estimated duty cycle.
→ Completely shutting down the DEPFET and the analogue part of the electronics between trains → 1/25 power reduction if 1/100 duty cycle



• $T_{env} = -10\text{ °C}$
• $V_{air} = 2\text{ m/s}$

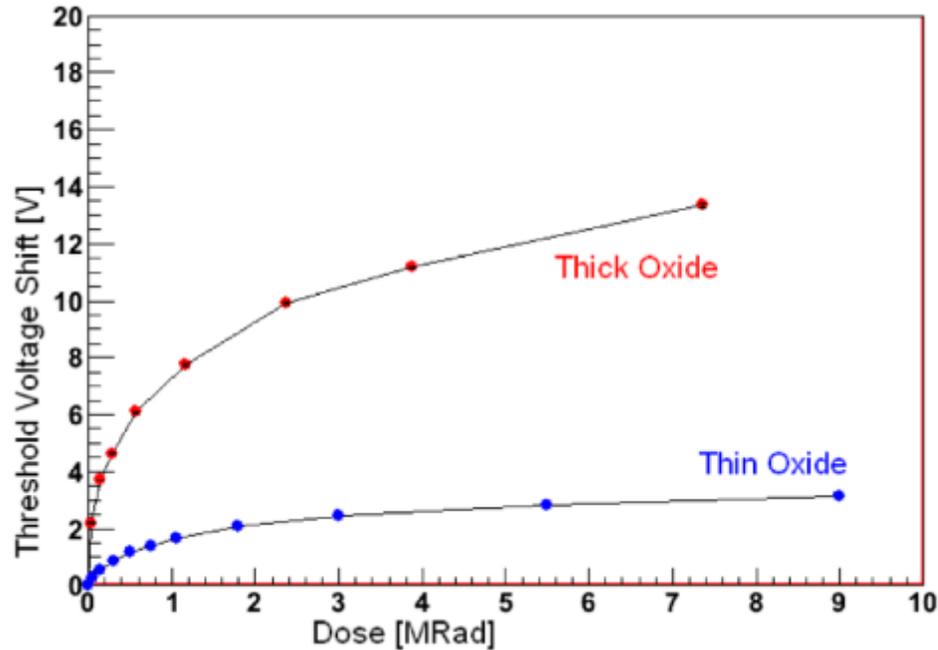


The air speed and temperature are not optimized to minimize the temperature distribution

$P_{FE} = (0.5/25.)\text{ W / per chip}$
 $P_{Sw} = (0.1/25.)\text{ W / per chip}$
 $P_{Sensor} = (1./25.)\text{ W in total}$

↘ Although very preliminary, the cooling seems feasible so far

- Surface damage



- Bulk damage

