



- Annual Conference of German Physics Society (DPG)
  - Section Particle Physics
  - 24. 28. March in Mainz
  - Every member is allowed to give a talk
  - ~1000 contributions
  - Many parallel sessions
  - Also invited talks and plenar sessions
- This talk:
  - TPC 2 session
  - Abstract: http://www.dpg-verhandlungen.de/year/2014/conference/mainz/part/t/session/33
  - Group report: ~15-17 minutes talk + 3-5 minutes for questions
  - Idea: want to intoduce LCTPC-pixel collaboration
  - Present our work (with focuss on my/Bonn activities)
  - Hope: find some new members ;)





# A pixel TPC for the Linear Collider:

# **Towards a demonstrator module**

#### **Michael Lupberger**

GEFÖRDERT VOM



Bundesministeriun ür Bildung ınd Forschung University of Bonn On behalf of the LCTPC-pixel Collaboration



Pixel-TPC Meeting 13.03.2014







- LCTPC-pixel collaboration
- Timepix Chip
- 2013 Testbeam and data analysis
- Simulation
- Readout system
- Demonstrator module



# **LCTPC-pixel collaboration**

- LCTPC collaboration:
  - Develop a TPC for physics up to 1 TeV (at the ILC)
  - Groups from America, Europe and Asia
  - Several readout concepts using GEM/Micromegas
- LCTPC-pixel
  - R&D towards a pixel-TPC: MPGD + pixel readout
  - Groups:
    - NIKHEF: Module construction
    - University of Kiew: Simulation
    - CEA Saclay / DESY: Data analysis
    - Uni Bonn: Module construction, readout system, data analysis
    - Uni Siegen: Data analysis
  - Goal: build a demonstator module for a pixel-TPC







• Setup at DESY





# Timepix chip

- Universal readout chip
- Properties:
  - active surface: 1.4 x 1.4 cm<sup>2</sup>
  - pixel size 55 x 55 μm<sup>2</sup>
  - 256 x 256 pixel array
  - 14 bit counter in each pixel (ToA or ToT)
  - Noise threshold  $\sim 500e^{-1}$  (ENC  $\approx 90e^{-1}$ )





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#### Setup at DESY







March/April 2013: 2 LCTPC octoboard modules

- Different amplification structures: GEM / InGrid
- Test of readout system
- Readout rate: 2.5 Hz; 40MHz clock
- Electron beam of up to 6 GeV
- Gas: Ar:CF4:iC4H10 (95:3:2) = T2K gas
- ~ 2 Mio. frames recorded, including B = 1 T
- Extensive testbeam program
- Preliminary data analysis in MarlinTPC Robert Menzen



### 2013 test beam





200

### **Reconstructed tracks**







# **Transverse spatial resolution**





## **Data analysis**

Andrii Chaus (DESY/CEA Saclay):

Processing Octoboard test beam data

- MAFalda analysis framework ok for fast analysis at testbeam
  - Track reco based on raw data, no GEAR info
  - Field distortions, drift velocity, residuals, diffusion
- MarlinTPC for real analysis (using GEAR information)
  - Processors for octoboard analysis
  - Analysis chain setup ongoing

Amir Shirazi (Uni Siegen):

Just started to set up and learn MarlinTPC



# Simulation

Oleksiy Fedorchuk (Uni Kiew) : Octoboard simulation

- Single octoboard simulation
  - Successfully modelled
  - Field distortions
  - Simulated occupancy similar to data
  - Impact of shifted chips
- Next step:
  - Include B field
  - 100 chip module



0.45

0.4

0.35

0.3

0.25

E

0.05 mm gap

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-100

-200

-250

-300 -350

-400

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### **Detector construction**

Jan Timmermans (NIKHEF) : 2 Octopuce testbeam

Testbeam with 2 Octoboards @ LP

• Plan for module layout + readout

			0		
	PCB		<u>Common atom</u>		
	Т?		Connector		
	Ingrid		CO2 cooling tul	be	
	FPGA				universitätbo



# Bonn group activities



### **Data analysis**

Martin Rogowski: A new tracking algorithm



Reinvestigate field distortions of Roberts analysis





• Algorithm from Forward Tracking Detector for ILD



### **Data analysis and simulation**



Martin Rogowski: A new tracking algorithm

### Listen to his talk !



#### Scalable Readout System (RD51, CERN)





#### Chain: Chip – Adapter card+FEC – Computer



### SRS with Timepix chip

Adapter card Type A



JTAG program

SRS FEC with Virtex 5 FPGA

Timepix chip on carrier

Intermediate board (can carry 8 daisy-chained chips)

Ethernet to PC

# New Intermediate board



I2C: standard for small network. Signals: scl (clock), sda (data) Originally between PCBs next to each other. Several meters distance using extenders.



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# **Status Timepix+SRS Readout**

- Test of FPGA Firmware:
  - I2C interface ready
- Test of new components finished
  - I2C network ok (DACs, ADC, expander work)
  - DDR2 Ram ok
  - LVDS driver work
    - => chip can be operated, data taking ok, even for 8 chips
- Software implementation finished (ADC readout for DAC scan, automatic calibration with test pulses from multiplexer)
- Redesign of intermediate board and A Card for scale-up



# **LP module: next steps**

- ~100 chip module
- Progress depends on many factors
  - InGrids
  - Man power
  - DESY testbeam schedule
- Project: test a 32 InGrid board in September/October
  - Similar design as 8 InGrid module
  - Expandable to 96 InGrids
- Mechanical construction (Bachelor student: Johann Tomtschak)
  - CAD drawings in SolidWorks
  - Construction of light LP frame in workshop
  - Construction of chip support structure in workshop
  - Use water cooling

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# **LP module: next steps**

- ~100 chip module
- Powering (Bachelor student: Kathrin Kohl)
  - Was already critical for a single octoboard
  - Low voltage supply for 4/12 octoboards?
  - High voltage supply
- PCB layout (Jochen Kaminski)
  - Depends on powering
  - Space is limited
  - Need many HDMI cables
- InGrid bonding, testing, quality control, calibration





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#### LCTPC-pixel collaboration is very active:

- Analysis of 2013 testbeam data
- Simulation of field distortions
- Development of readout system
- Design of a 32 / 96 chip module

#### => Demonstrator for a pixel TPC (for ILD @ ILC)



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# Schedule for 2014

• Additionally:



- Need/would like to have a master student for full analysis
- Data analysis of new testbeam data
- 96 chip module test in 2015 ?

Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	
Octobo HDMI Virt	ard cap board to ex 6 bo	oability, esting, ard	Firmy for octobo FE	Firmware for 4 ctoboards/ FEC Testbeam Prepera				m, ation	Dat	ıta analysis		
Michael Lupberger												
PCB single	finalisa e/octobo	ation bards	32 chip module construction					Testt	96 chip module Testbeam <sub>co</sub> nstruction			
Jochen Kaminski, Michael Lupberge								20	14/			
			Johann Tomtschak Kathrin Kohl					2015				
Track reconstruction algorith												
2013 data analysis with new algorithm											÷.	
Martin Rogowski												
							Full 2	2013 da	ata anal	ysis?		
									sier slude	III?		

## We can provide soon:

- SRS (A card) with full functionality (for MUROS compatible intermediate board)
  - Users with SRS can plug and play Timepix
  - Users can use MUROS or SRS for same detector
  - Comparability study, documentation
- V6 evaluation board (VHDCI cables MUROS compatible):
  - Updated adapter board, I2c network tested
  - ADC, DAC control and readout with i2c (firmware, software)
  - Users with V6 board can plug and play Timepix
    - Users can use MUROS or SRS for same detector
    - Comparability study, documentation:
  - Use in CAST



### Xilinx Evaluation board





#### Virtex 6 FPGA

# **Preliminary Analysis: Cuts**



Dataset for first analysis:

z-scan, B=0 T, 
$$E_{Drift}$$
 = 230 V/cm (D<sub>T</sub> = 311 µm/ $\sqrt{cm}$ )

 $\Rightarrow$  tracks parallel to x-axis

Cuts:

- Only hits within shutter window
- More than 200 hits per track



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- Entries 400 Preliminary 350 300 250 200 Chip 150 100 50 0\_50 -40 -30 -20 -10 0 10 20 30 40 50 d<sub>o</sub> in mm
- Tracks centred on lower chip row (z dependent)











# Preliminary z-scan results



