Toward the Final Design of ILD TPC

Responding to the requests of the ILD management

The ILD meeting 2014
Ohoshu City/ 7-9 September, 2014

T. Matsuda
LCTPC collaboration

Requests from the ILD Management

ILD at the moment is considering several options for the sub detectors. While we are clearly not yet in a position to make a technology choice, we nevertheless should prepare ourselves for the moment when we will be asked to make such a choice. We like to invite you to discuss , again with the perspective of your sub-detector, how we should approach this point:

1. Which steps are still needed to have sufficient information so that a comparison can be made
2. How do you propose to make a comparison.
   Can you provide a list of "observables"?
   Is there a list of milestones each technology has to meet?
3. Are there major things missing?
4. Do you foresee major problems (funding/ manpower/ technological)?
5. How do you want to organize this process? How do you ensure that any decision at the end is supported by the community?

The Options of ILD TPC

We have the options only for the MPGD TPC technology and modules. We do not set options for other components of ILD TPC. We have a lot of engineering issues for the other components, which we are not able to access enough with our minimum resources:

(a) **The options of the analog TPC (Pad readout):**

Micromegas module with the resistive anode readout

GEM modules with the direct pad readout:

Three layers of the CERN GEM (DESY module).

Two layers of thicker (100micron) GEM (Asian module).

The current basic performances (resolution) of the three options in the TPC Large Prototype beam tests at DESY are comparable and satisfy the basic requirements for the ILD TPC. Thus the selection among the options will be made by other considerations.

(b) **The option of the digital TPC with the pixel readout (Timepix I):**

The idea of the digital TPC is interesting and elegant. This option has not reached to the performance level of the pad readout TPCs. The R&D will be continued with a larger number of the Timepix-I chips (one full LP module) and with the new Timepix-III chips with which we can route the signal by the silicon through hall.

Remaining R&D Issues

(1) **Before the comparison of the options:**

a. **Ion gate**: the most urgent issue since it has a large impact on the modules designs.
b. **Local distortions of MPGD modules**: Module designs to minimize the distortion、and the corrections for the remaining local distortions.
c. **Some issues with the MPGD technologies and the MPGD modules:**

(2) Before the engineering design of the ILD TPC :

d. Demonstration of the power pulsing and the cooling of module (with the S-ALTRO16 electronics).
e. More demonstration of the performance of the MPGD TPC at the ILD magnetic field: 3.5-4T, and necessary measurements of basic parameters of the TPC gas (T2K gas).

<u>Ion Gate: The Most Urgent Issue</u>

We need an ion gate: To prevent the backflow of positive ions from the gas amplification region into the drift space we need a ion gate.

The candidates:

GEM gate: A GEM with a large geometrical aperture of holes. <u>The goal is the electron transmission of 80% (*1).</u> Mechanically friendly to our current MPGD modules**.**

Traditional wire gate: Known to work with high electron transmission (LEP etc.). Mechanical issue to mount on the MPGD modules.

(*1) The deterioration in the TPC spatial resolution would be O(10%) but the deterioration in the momentum measurement by the ILD tracking system will be much smaller for high momentum particles.

Schedule:

- The gate GEM fabrication: A LP size gate GEM (proto) in JFY2014.
- A confirmation in beam test (with the current LP modules mounted with the GEM gate) in 2015.
- The decision of the gate device for ILD TPC in 2015-2016.
- The design, the fabrication and the tests of the optimized (*2) LP modules with the gate in 2015-2017.

(*2) Also for the local distortions hopefully.

Local Distortion:
The Old TPC Problem in the New Regime.

All current LP modules see rather large local distortions:
First try to minimize the distortions in the hardware level, and then, try to correct the remaining distortions by software.

(1) Distortions due to **the specific structures of the current modules:**
Micromegas module: A grounded guard structure of the micromegas mesh all around the module (To be modified in next module).
Asian GEM module (ready to mount a Gem gate):
The structure to stretch GEM (without the field shaper) (To be modified in next module).

(2) Distortions at **the module boundary and the gaps between the modules:**
The E-field calculation and the E x B simulation suggest how to reduce the distortion. The studies with the laser beam, the laser pattern on the cathode, and the beam test to confirm the improvements.

The module boundaries and the distortion regions of the modules as the dead regions should be included in the ILD physics simulation. (Currently only the fiducially volume of ILD TPC.)

(3) Develop **the method to correct the remaining distortions after (1) and (2)**

Some Issues Raised

for the MPGD Technologies, the MPGD Module

and the ILD Trcaking Ssytem

1. **Possible signal pileup in the resistive anode** (the micromegas module) in the ILC environment : To be done.
2. **The rate of the micro discharge of the Asian GEM module** : in the case of the Asian thick GEM (in for the given gas condition of the LP TPC, i.e., the ILD TPC): Under study.
3. **The long term stability of the modules**:

----

4. **The size and the shape of the module**: Make it larger, but possibly limited by the gate.
5. **The pad shape and size**: Not really select one technology and one module.

----

6. **The optimization of the ILD tracking system and the momentum resolution:** <u>Need clear criteria from our physics goals at ILC.</u>

What are Missing Now

The Questions 3 & 4 by the ILD Management

A. We have a lot of design work left to be done for the TPC components other than the MPGD module. The major ones are:
   - **Readout electronics for the ILD TPC**: Trying to organize our own electronics group (chips and boards) to investigate the possibilities for the ILD TPC electronics. The real work may start by the GO sign for ILC.
   - **Engineering Design of the whole ILD TPC** :

B. We still miss a plan of our tests in the high magnetic field: 3.5-4T.

Some Excerpts from

The European R&D Committee Report: 2013 Report No. 3

(Received in March 2014)

The collaboration needs to increase resources in the area of technological and system R&D, and to prepare an overall plan for completion of R&D, technology choice, and the development of a complete design for the TPC system to be captered in a Technical Design Report .

1. Design of new front-end electronics (readout chip) is too early.
2. Look into the flip-chip interconnection techniques in the integration of the electronics in the end (pad)-plates ("the advanced endplate"). Need a group of a few engineers.
3. Make a unified GEM group using the CERN GEM.
4. The distortions are the urgent issue.
5. The collaboration should clarify the acceptance criteria that would allow the further development of this interesting digital readout concept.
6. The gating grid structure is most urgent. It should be concluded as early as possible with detailed design and prototype tests.
7. Review the current mechanical design of the endcap where the combined mechanical structure of Al and PCB that could lead to deformations.

Conclusion

2014-16	**R&D on ion gates and a decision on the ion gate.**
2015-17	**New LP modules with the gate and their beam tests.**
2017-18	**Decision on the MPGD technology and the module design (when necessary).**

----------------------------- In the earliest ---------------------------------

2017-18	ILC LAB & the call for the ILC experiment .
2017-19	Design of the readout electronics for ILD TPC and its verifications Engineering design of the ILD TPC
2019	The TDR of the ILD tracking system.
2019-24	Prototyping and production: Electronics (chips →boards) Prototyping , test and production: Modules . Production: Field cage/endplate and all others.
2025	TPC integration and the final test on the surface.
2026	TPC Installation into the ILD detector (underground).
2027	The ILC commissioning