Status report on the development of a TPC readout system based on the SALTRO-16 chip

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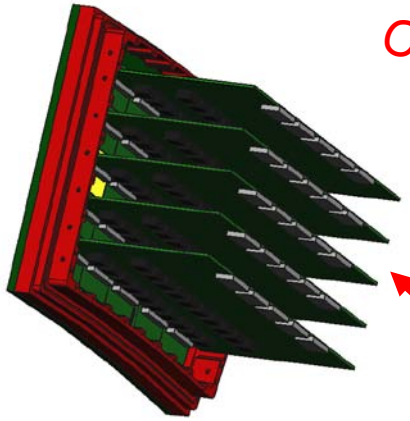
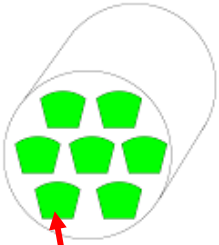
Overview of the SALTRO16 readout system

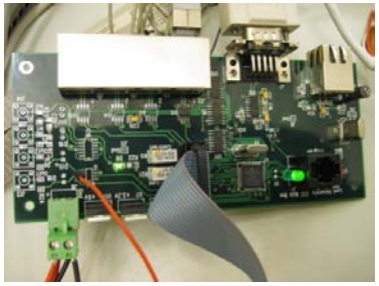


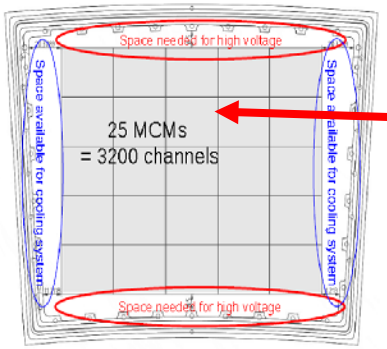
LowVoltage boards attached to one pad module



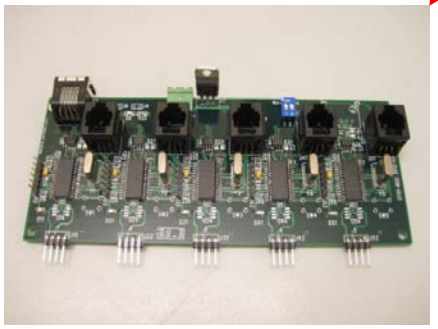
The Large Prototype TPC

Detector Control System – Master module

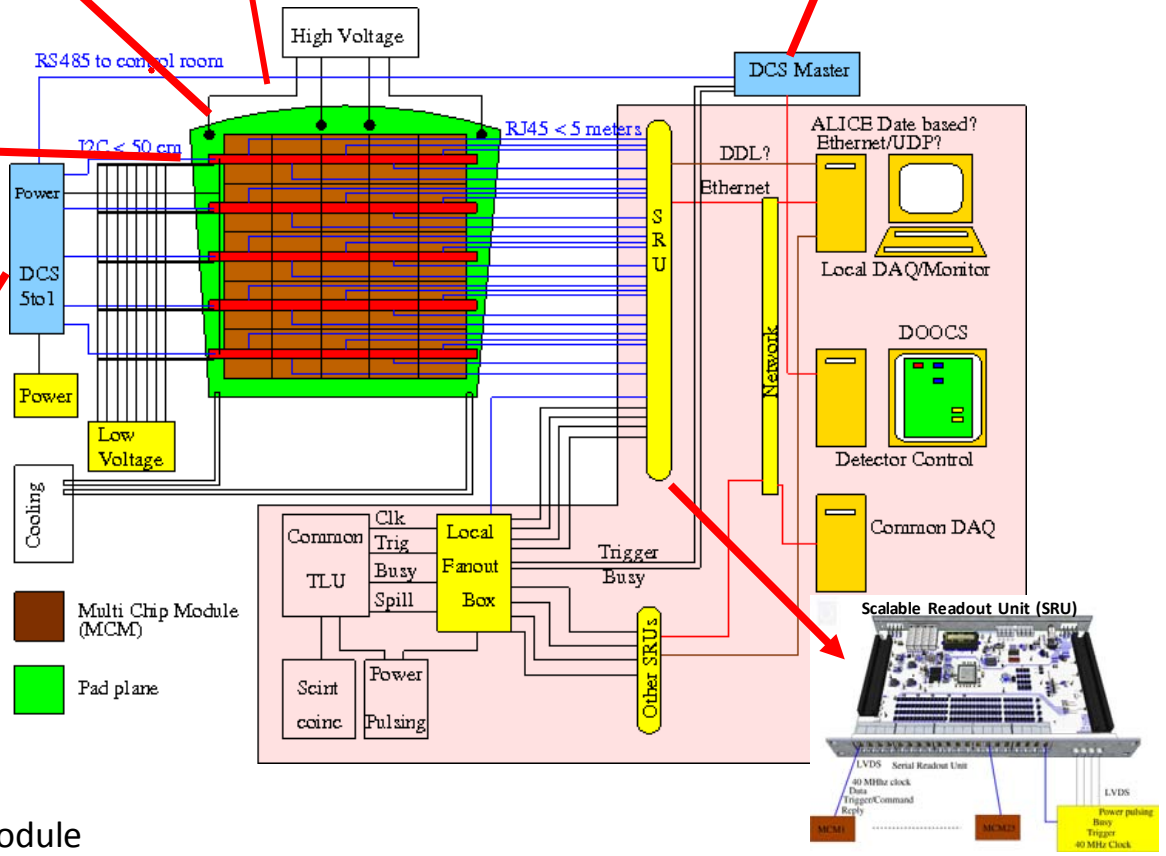




MultiChipModules on a pad module

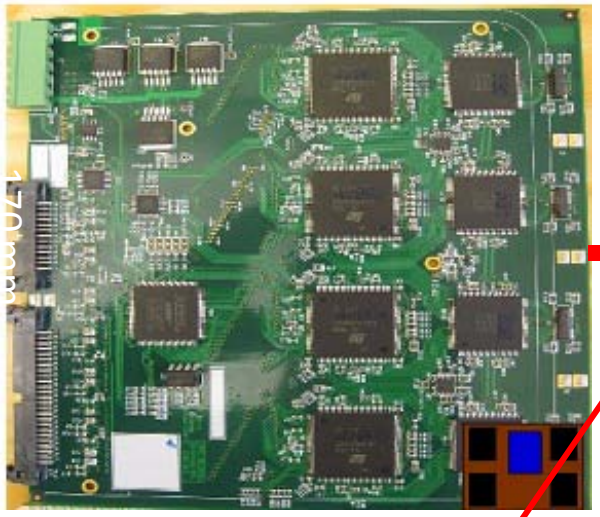


Detector Control System – 5to1 slave module

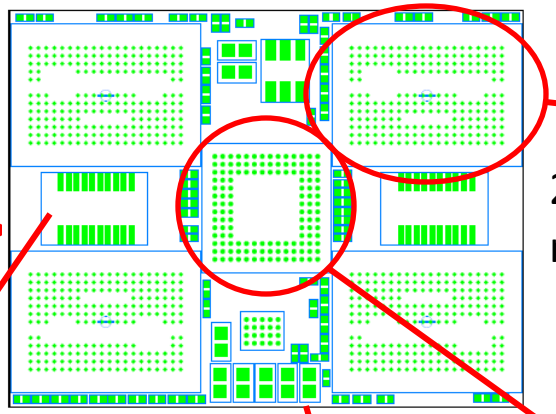


From ALTRO to SALTRO16
A decrease in size by a factor 40 of the front end electronics

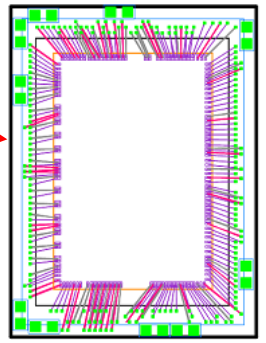
FEC with 8 ALTRO



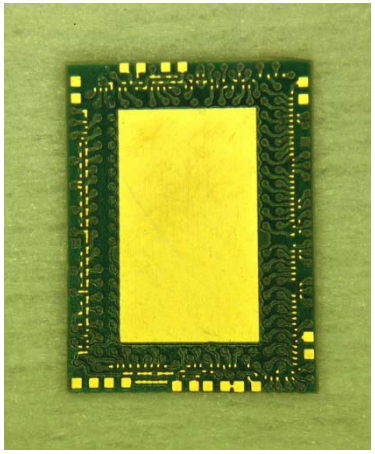
MCM with 8 SALTRO on carrier boards



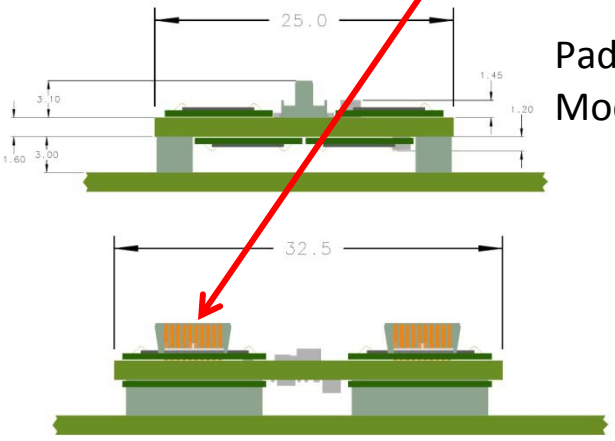
Carrier Board



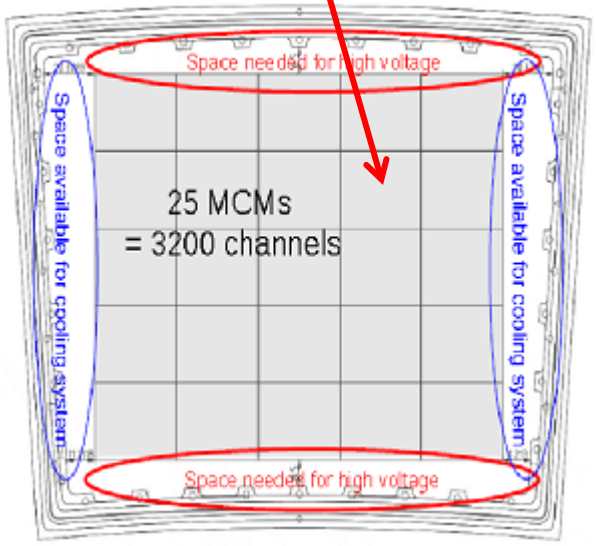
Carrier Board PCB



Side views of an MCM

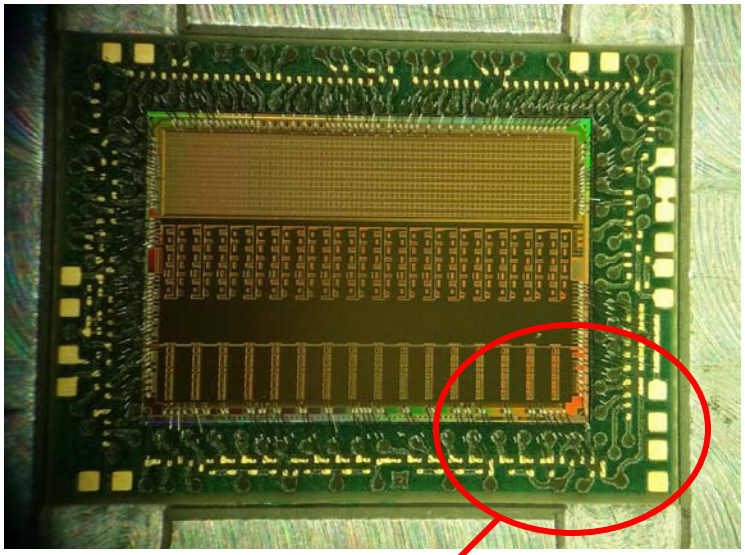


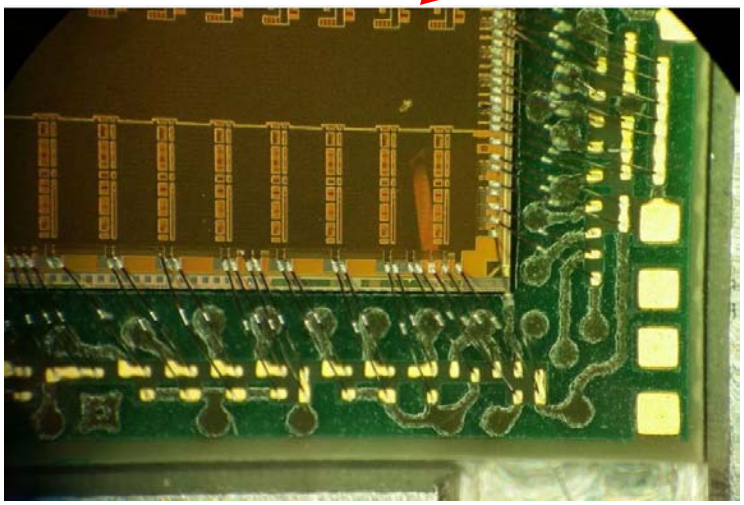
Pad Module



Status of the Carrier Board

Carrier Board with SALTRO chip mounted





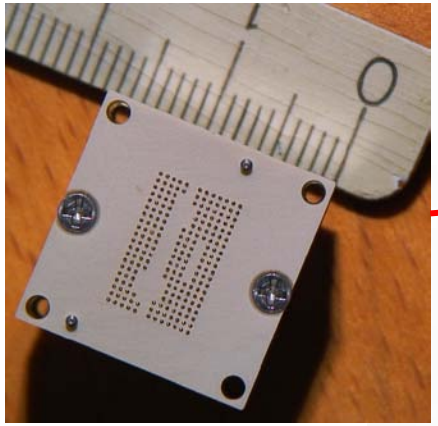
Bottom side of the Carrier Board with tin balls

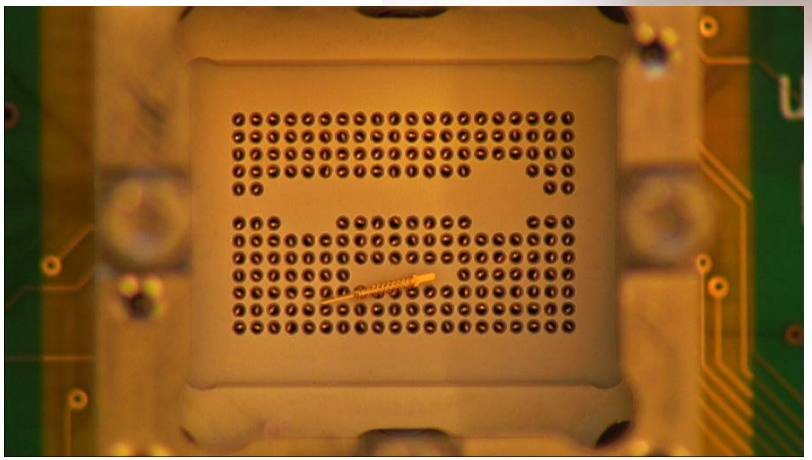
- A test sample of three Carrier Boards with bonded SALTRO-chips are ready
- There has been some problems with the application of the epoxy layer
- A new molding fixture has been fabricated and new epoxy materials are being tried out.

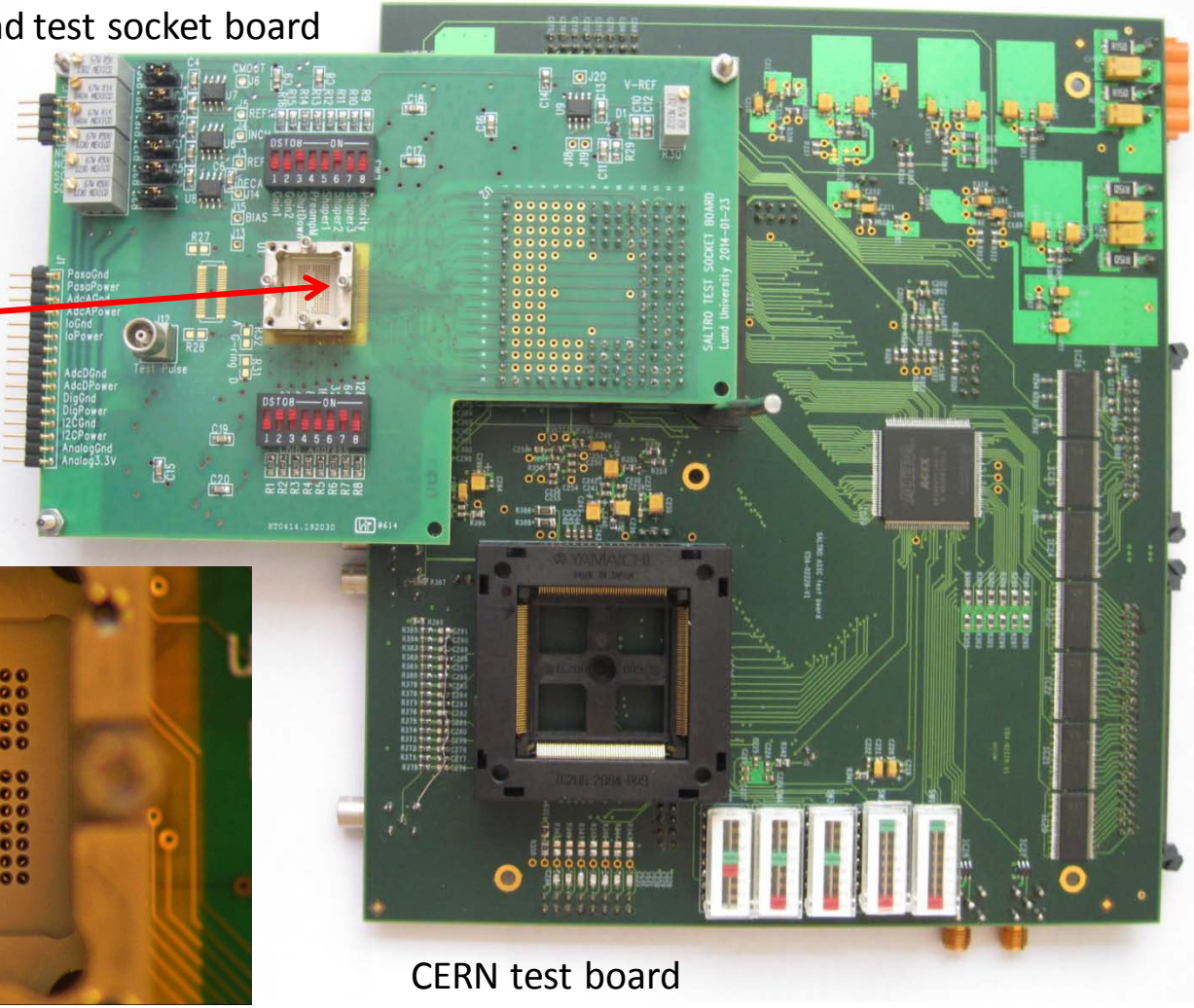
Test set-up for testing SALTRO16-chips on Carrier Boards

Lund test socket board

Test socket



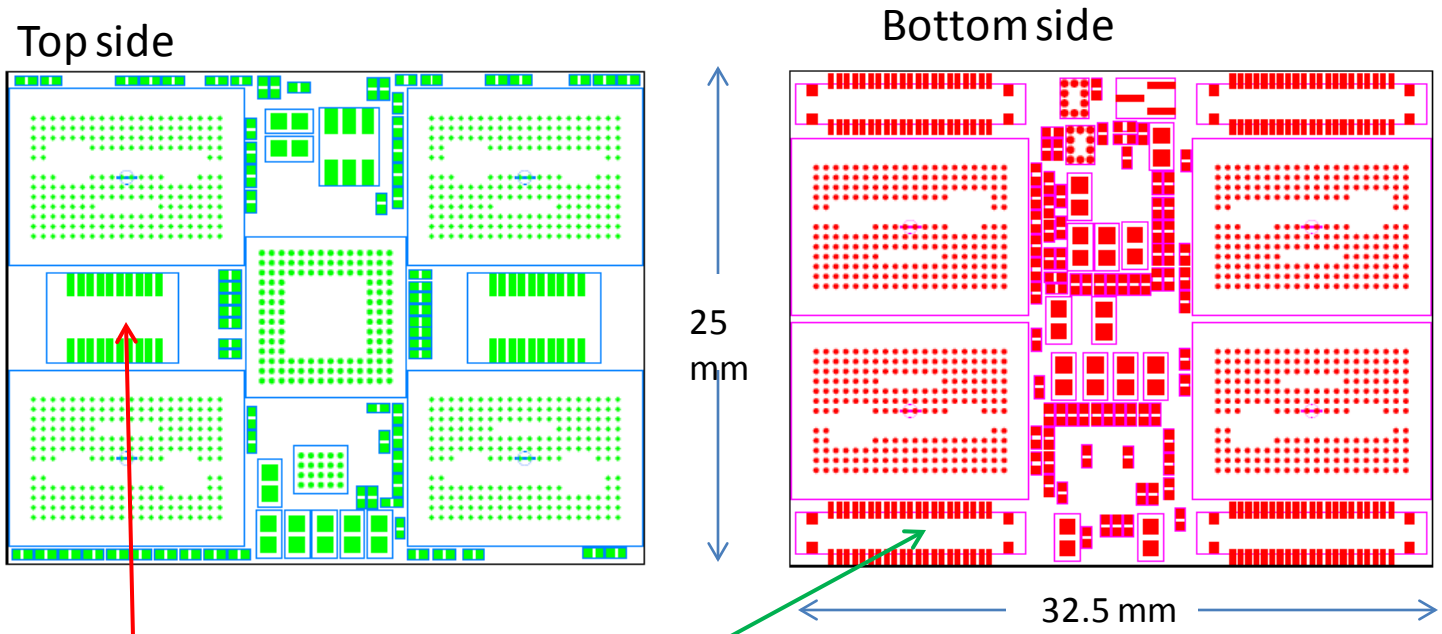




CERN test board

- Some modification of the CERN test board was necessary to fit our system
- The test set-up is assembeled and the communication to the CERN SALTRO test board has been established with packaged SALTRO16 chips.
- We are witing for the first three mounted Carrier Boards to arrive.

The final MCM-board



- The MCM-board will be redesigned in HDI-technology (High Density Interconnect)
→ The number of layers can be reduced (from 20 layers to 10 ?).

- This is a useful exercise for the design of the final front end electronics.

- The Panasonic connectors, which link the MCM-board to the padplane have arrived.

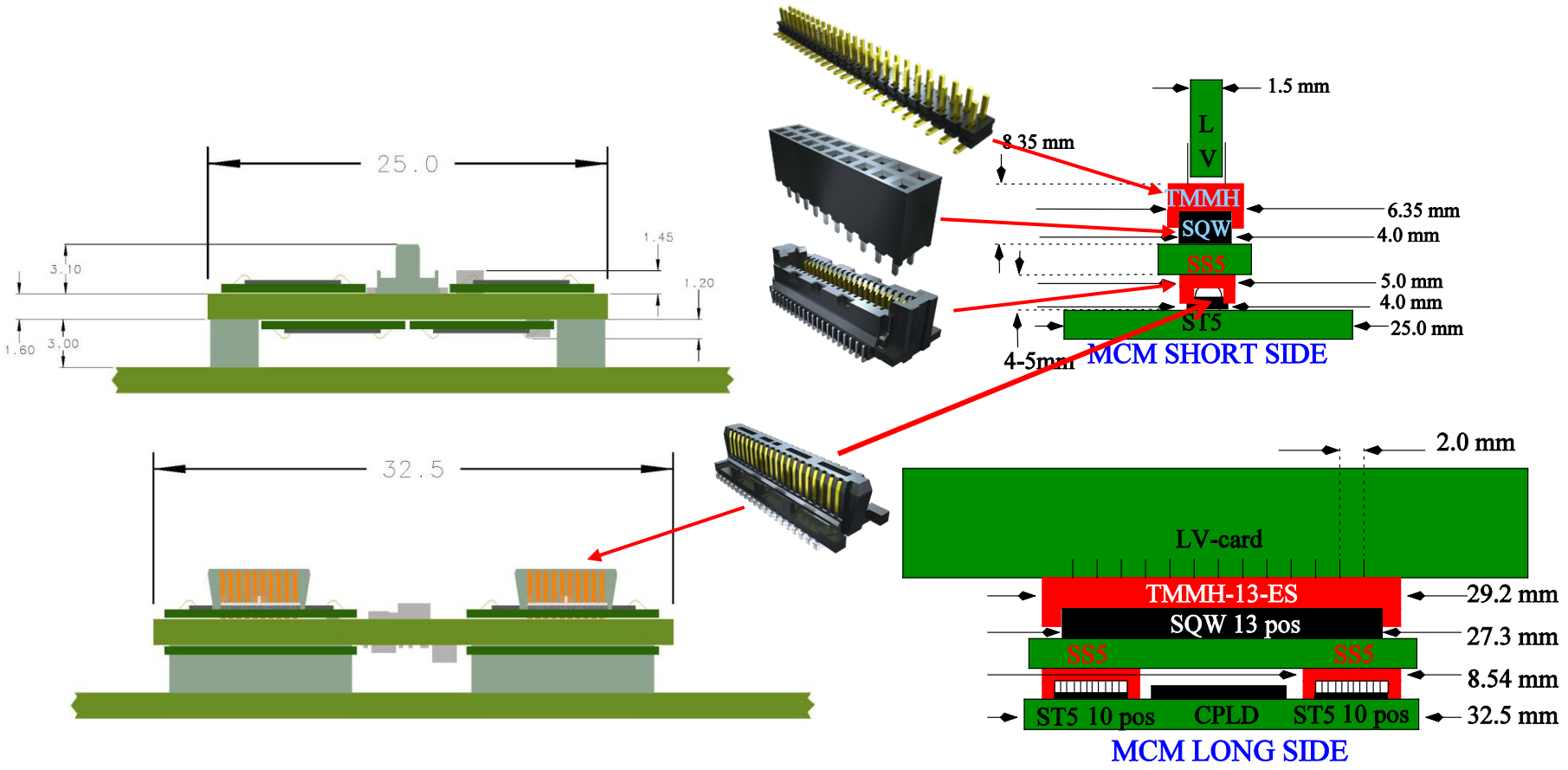
- The Samtec connectors on the top side of the board have also been delivered.

- We plan to produce a mock-up system to make sure that the mounting of the Carrier Boards and the connectors does not create problems.

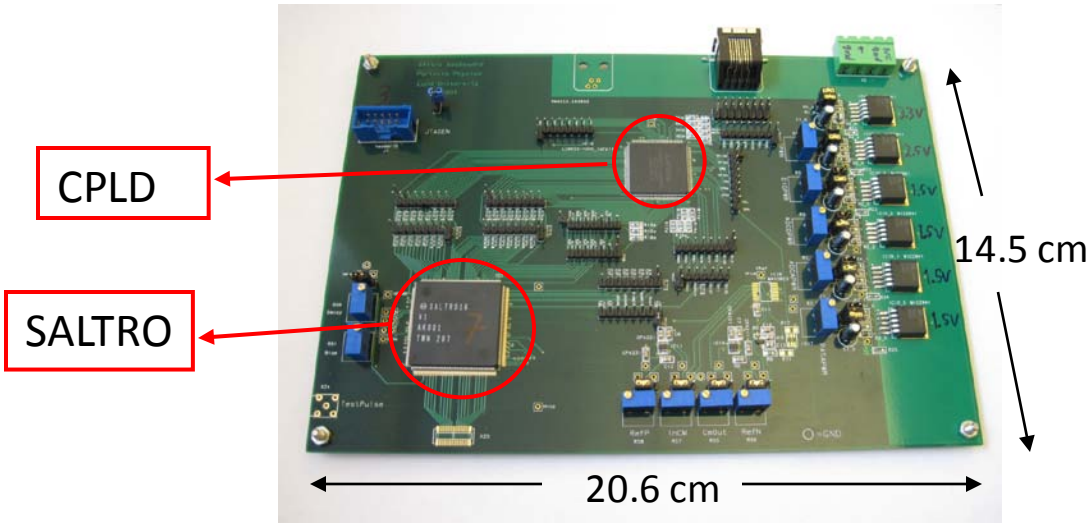
Complication with connectors

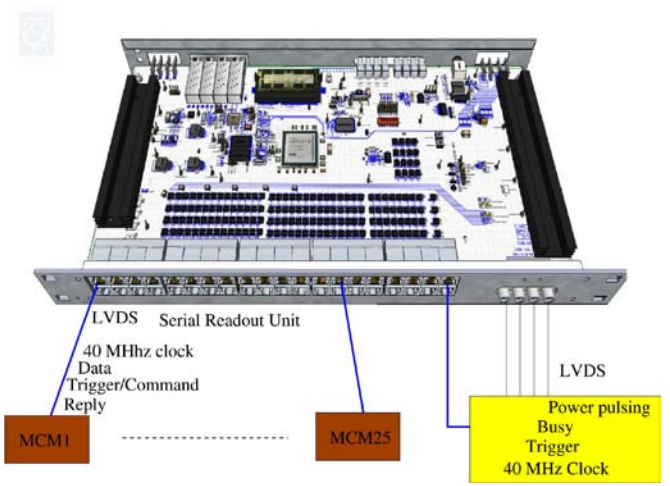
The problem with the male connectors on the upper side of the MCM-board is that the female partner can not be mounted on a vertical LV-board. This has forced us to introduce an adaptor board and a pair of additional connectors, which are suited for such mounting. The MCM-board plus the adaptor board can be regarded as a unit, which will not be separated.

The mock-up system will also be used to test that everything fits together



The MCM-development board (stand alone board)



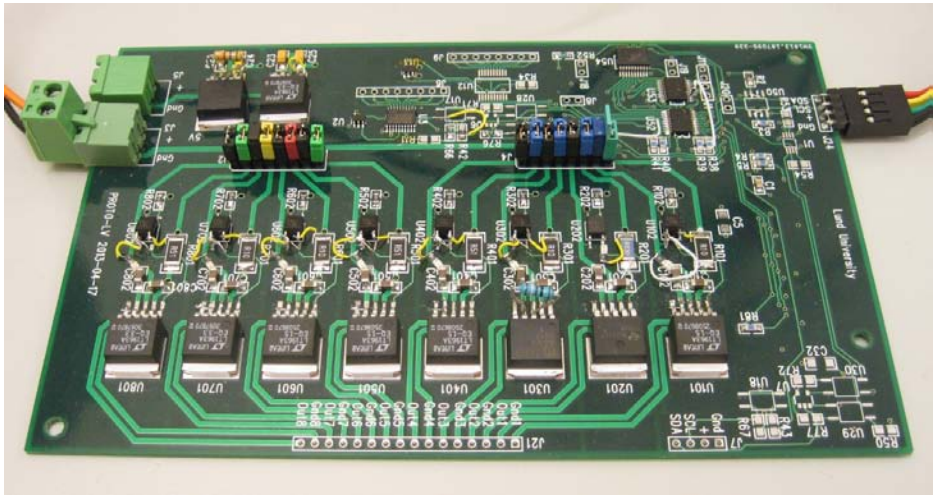


- The purpose is to develop firmware for communication between the SALTRO-chip and the CPLD (Brussels/Wuhang), and the SRU (Wuhang), respectively.
- SALTRO-chip in CQFP208 packagin
- Three MCM-development boards have been prepared (Lund, Brussels and Wuhan Univ.) and sent to Brussels for mounting of SALTRO-chips.

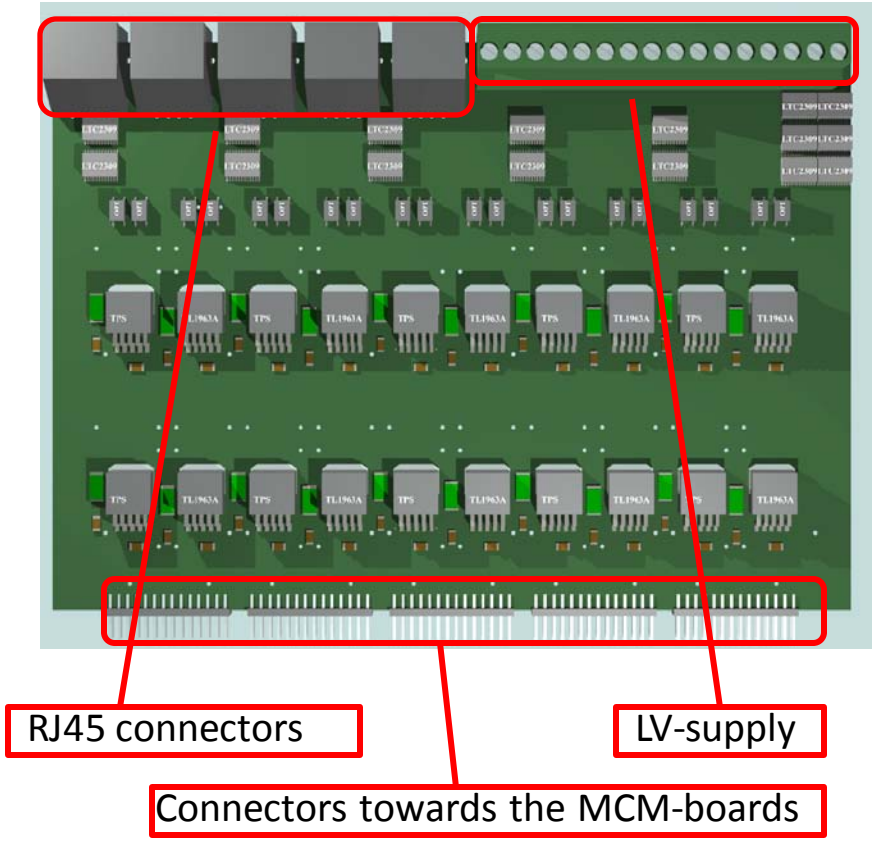
- The first tests in Brussels were succesful
  - The firmware for the CPLD was installed and communication between SALTRO and CPLD was established.
  - Communication with the SRU could also be established
- Readout via ALICE DDL worked but data was corrupt due to the firmware, which was not adapted to our system.
- We have decided to use ethernet connection for readout and control

LV-prototype board and the final LV-board

LV-prototype board
Dimensions 16 x 10 cm



Final LV-board
Dimensions ≈180 x 122 mm



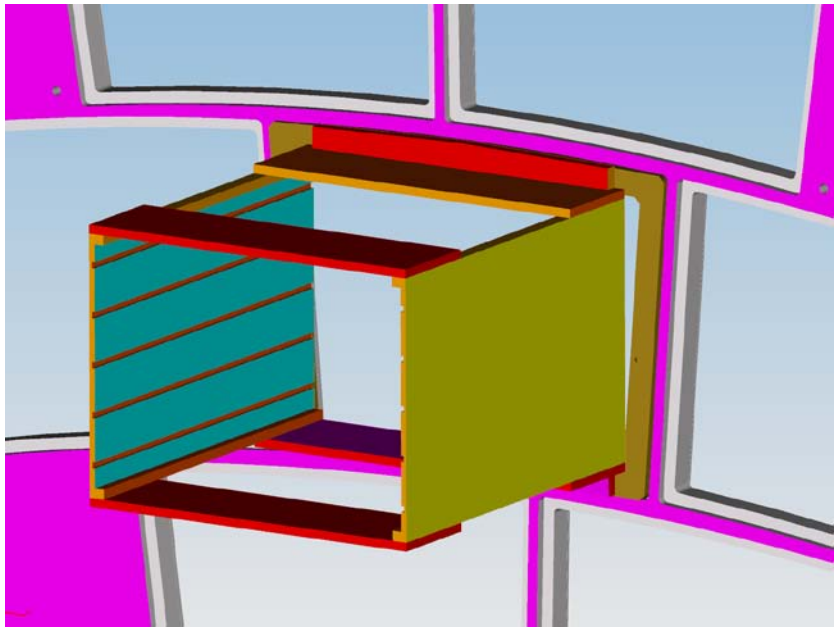
- The Low Voltage Prototype Board is used to test the concept of the final LV-board.

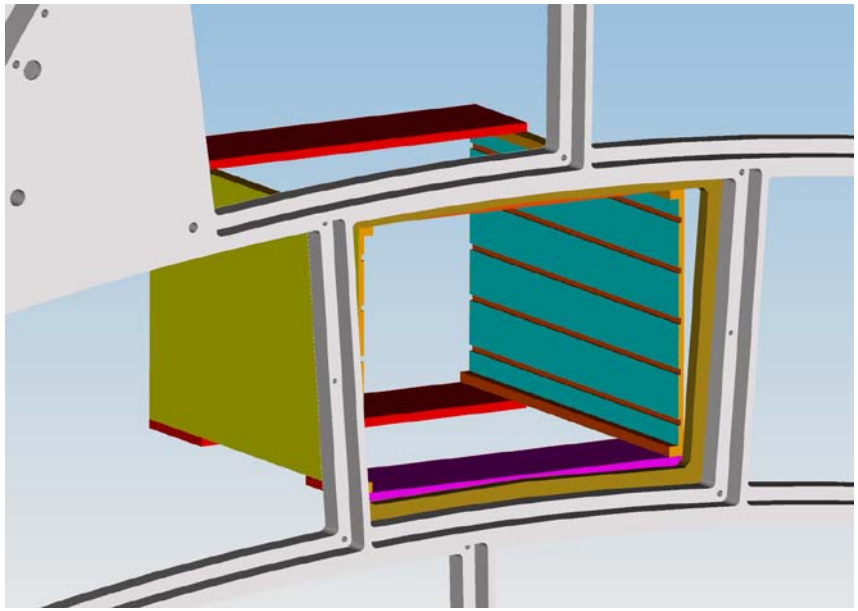
- It will also supply the test set-up with voltage and provide some configuration.

- The board is ready and has been succesfully tested together with the test set-up.

- For the final LV-board the concept is ready. We are waiting for the positioning of the cooling pipes and the final design of the mechanical support.

Ideas on the mechanics support structure

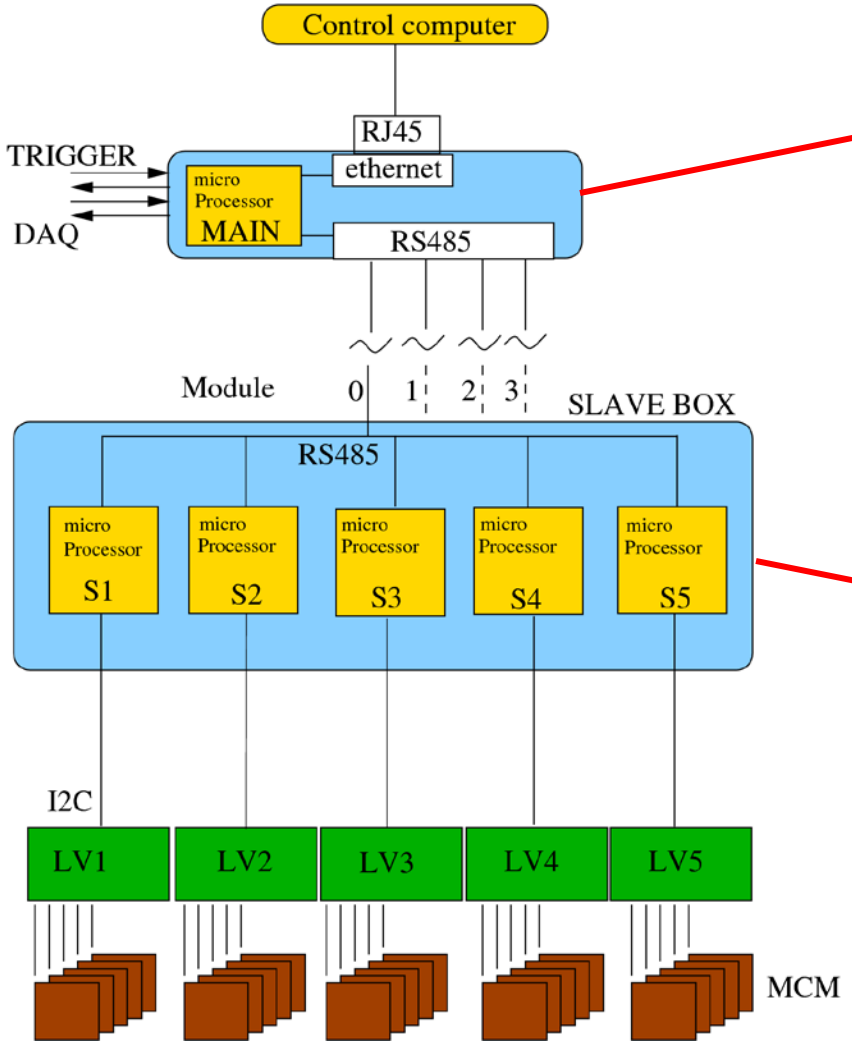


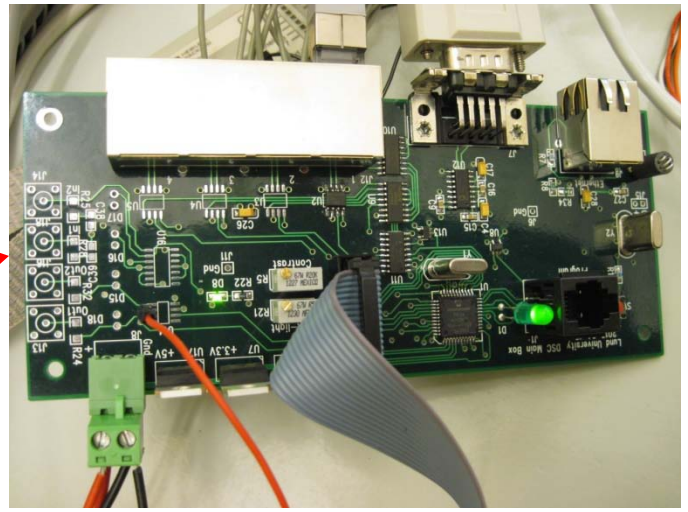


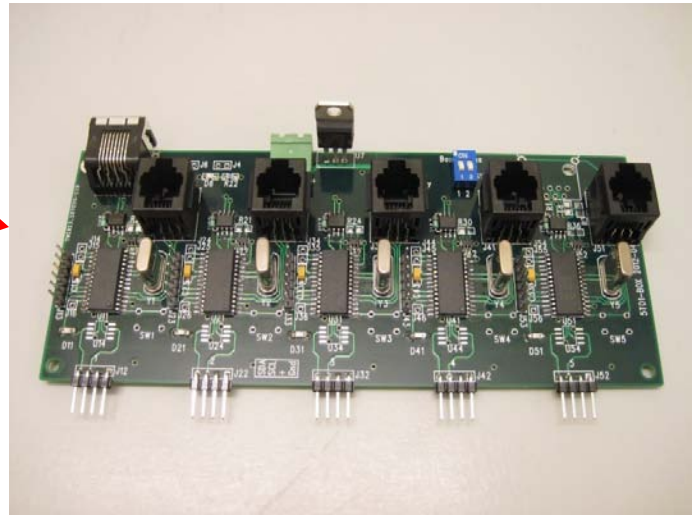
- The LV-box will be made out of aluminium with grooves in the side walls to guide the LV-boards onto the connectors on the MCM-board.
- There is some space on the sides and on top and bottom for connection of HV and cooling, although it probably needs some innovative solutions.
- This construction is open for discussion, but needs a decision soon.

The Detector ControlSystem

~700 parameters from the LV- and MCM-boards has to be monitored per module
DOOCS will be used







- The two boards have been successfully tested
- Will also be used for tests of SALTRO-chips mounted on Carrier Boards

Summary of the status and the next steps

- The test set-up for testing SALTRO-chips mounted on Carrier Boards is assembled and ready for tests of the chips.

- Three Carrier Boards with bonded chips have been produced although the application of the epoxy layer is still missing. When the top side is completely ready, tin balls are going to be applied on the bottom side and tests can start.

- Production of a mock-up system with dummy Carrier-, MCM- and adaptor boards to verify the soldering procedure and check that the various parts fit together.

- The final MCM-board is being redesigned using HDI technology.

- The design of the final LV-board can only be finished when the layout of the cooling pipes is defined and the dimensions of the mechnical support structure are settled.

- Modification of the firmware for the CPLD and the SRU (Brussels/Wuhang) and further tests of the communication . Debugging (Lund)

- Development of an Ethernet based DAQ-system and common DAQ integration.

All these activities are going on in parallel