DEPFET Based Ultra-light All-silicon Modules for Vertexing at a Future Linear Collider

- **Summary of the latest achievements at Belle II**
- **Integration and low-mass modules**

Ladislav Andricek, MPG Halbleiterlabor, München

For the DEPFET Collaboration

Cornerstone specs for a DEPFET system @ILC

:- small pixels (~20µm) for excellent single point resolution (~3µm)

:- minimal material

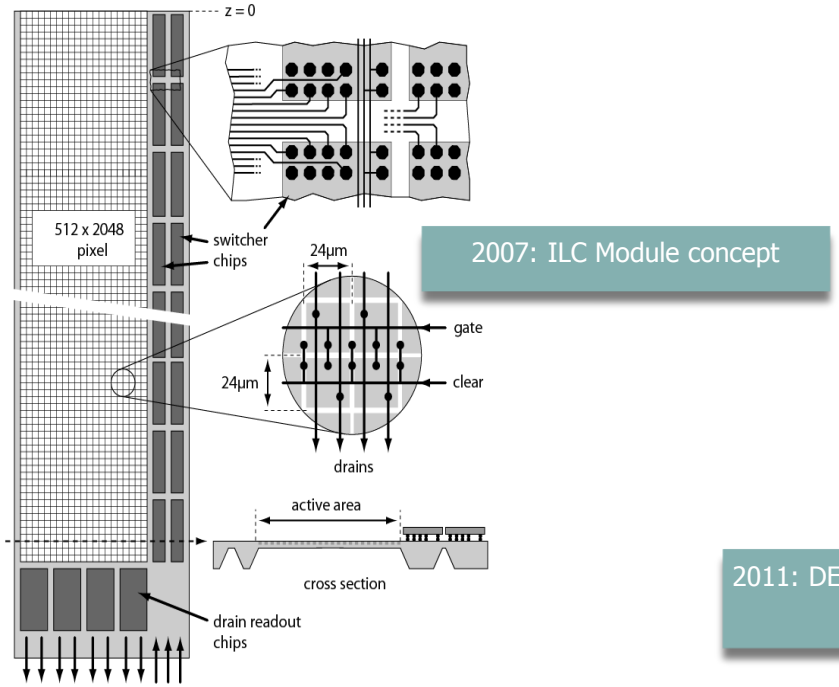
→ thin sensors with large S/N; minimize support, services, and cooling material

:- the DEPFET runs in a rolling shutter mode (read-out during the bunch train)

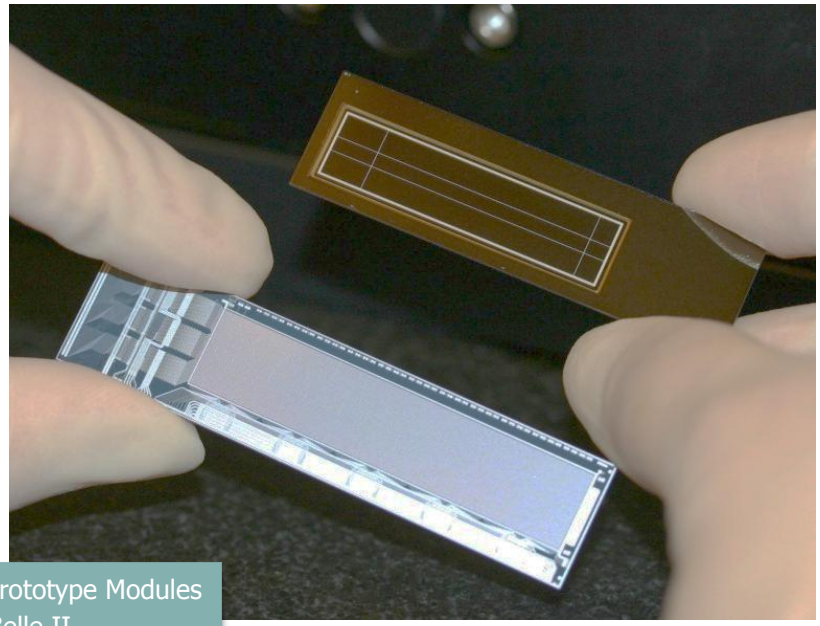
→ due to background, take as many frames as possible to minimize occupancy!

→ our goal is ~1/50µs frame rate, 1/50ns row rate (innermost layer)

:- radiation tolerant up to ~1Mrad and ~10^{12} n_{eq}/cm^2 for 10 years operation (e^- in the MeV range)



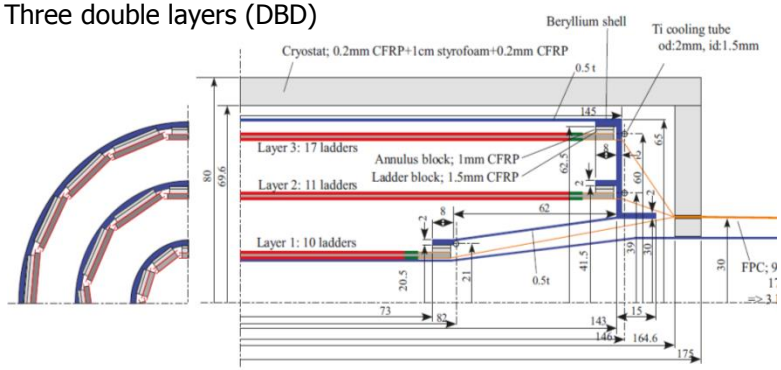
2007: ILC Module concept



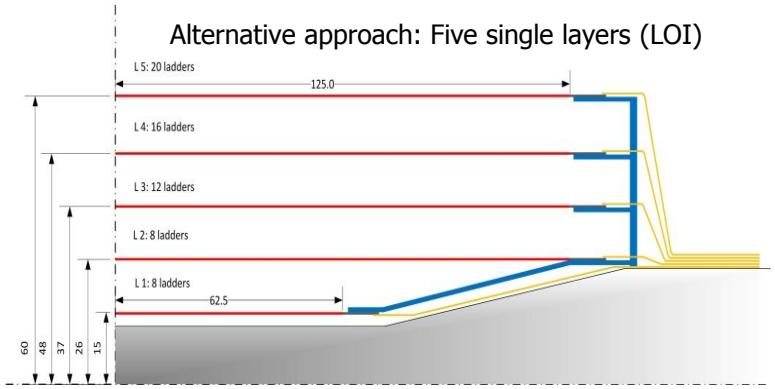
2011: DEPFET prototype Modules for Belle II

The ILD VXD ←→ Belle II PXD

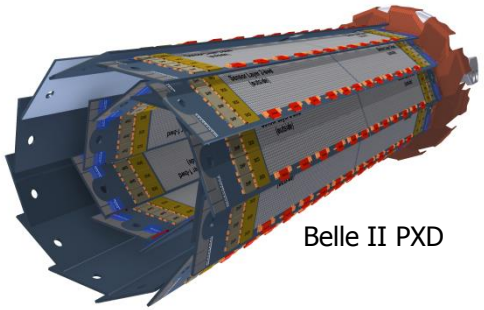
Three double layers (DBD)



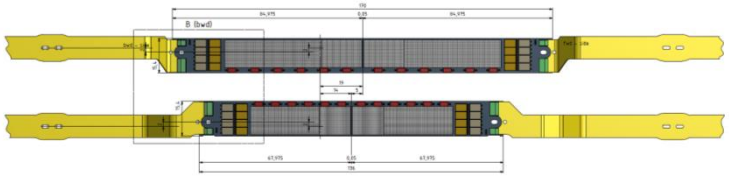
Alternative approach: Five single layers (LOI)

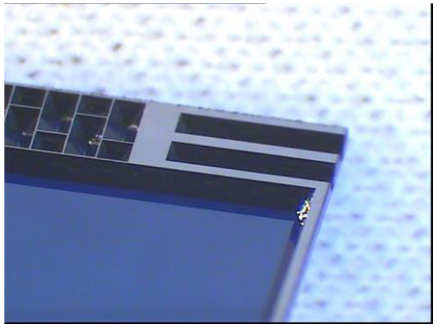


	ILD LOI 5-layer layout	Belle II	
Radii	15, 26, 38, 49, 60	14, 22	mm
Sensitive length	123 (L1), 250 (L2-L5)	90 (L1), 122 (L2)	mm
Sensitive width	13 (L1), 22 (L2-L5)	12.5 (L1-L2)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	20x20 (L1-L5)	55x50 & 60X50 (L1), 70x50 & 85x50 (L2)	μm^2
r/o time per row	50 (L1), 250 (L2-L5)	100	ns
Number of pixels	800	8	Mpix



Belle II PXD





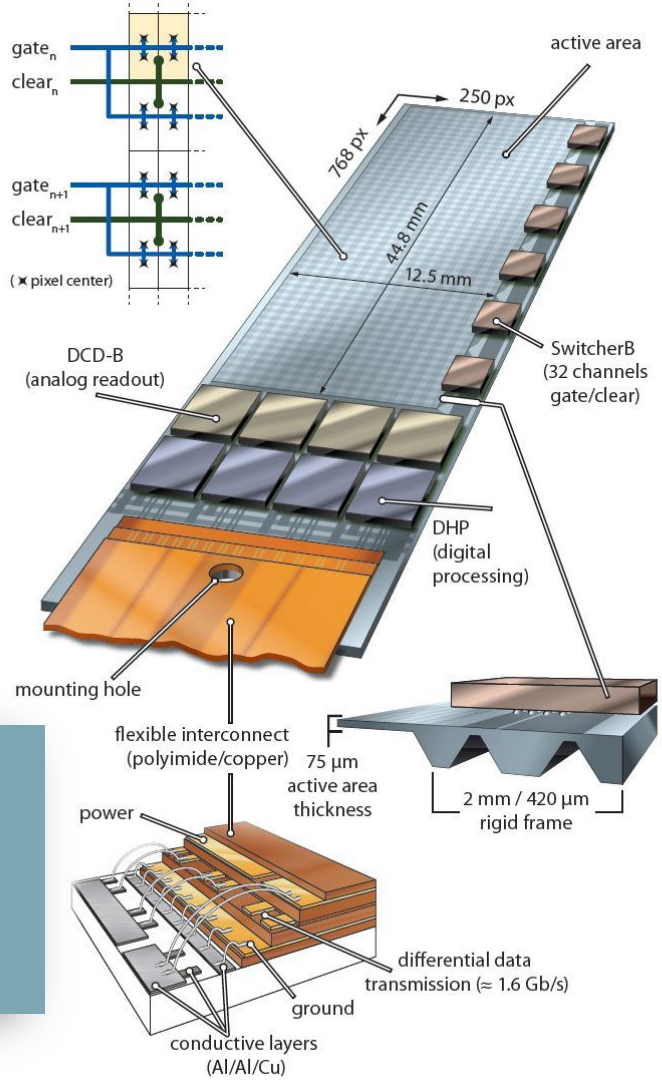
Belle II PXD ladder:
(almost) prototypes for L1 and L2 of ILD LOI layout!!

DEPFET all-silicon module

DCDB (Drain Current Digitizer)
Analog front-end

Amplification and digitization of DEPFET signals.

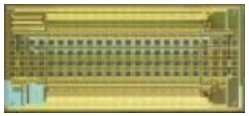
- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- new version **w/ 50ns** sampling time under test
- UMC 180 nm
- Rad hard design



Key to low mass vertex detectors

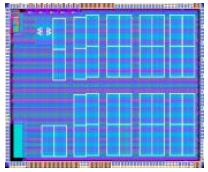
→ **highest integration!**
- ↳ Thin sensor area
- ↳ EOS for r/o ASICs
- ↳ (perforated) silicon frame w/ steering ASICs

SwitcherB - Row Control



AMS/IBM HVCMOS 180 nm
- Size 3.6 × 1.5 mm^2
- Gate and Clear signal
- 32x2 channels
- Fast HV ramp for Clear
- Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)
First data compression



TSMC 65 nm
- Size 4.0 × 3.2 mm^2
- Stores raw data and pedestals
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)

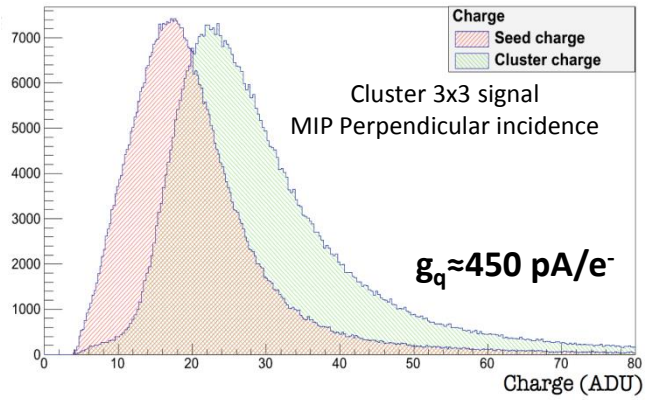
Sensor and r/o electronics: Beam tests with the full system

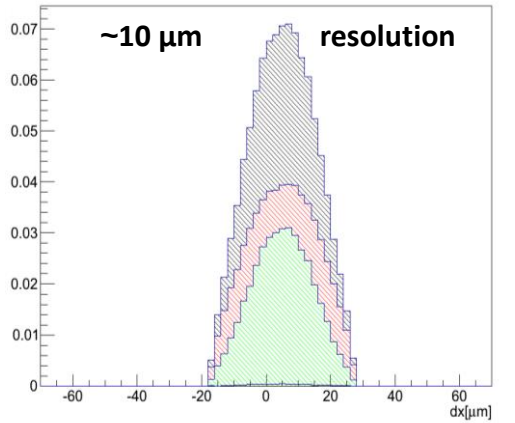
PXD6 Belle II design

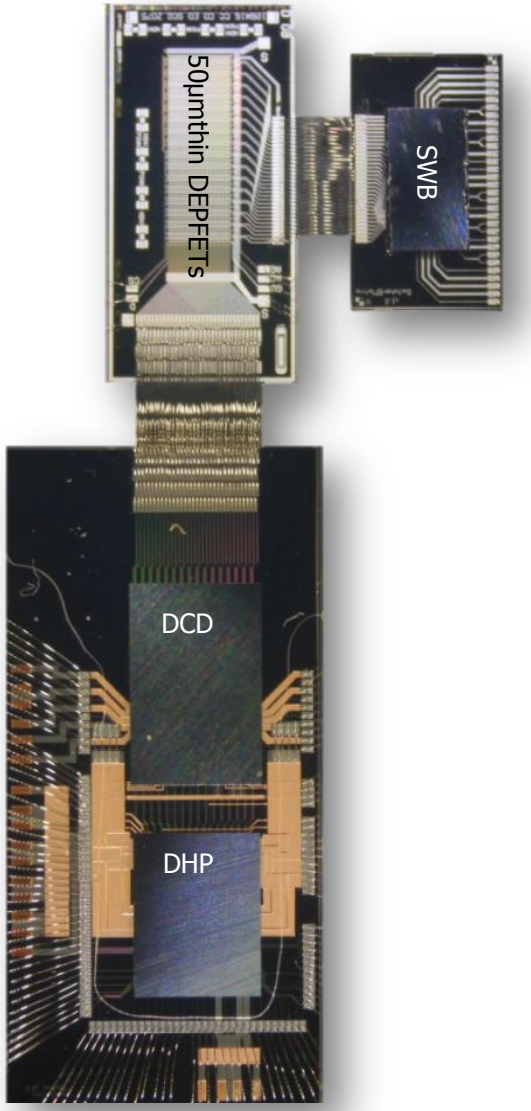
- ▷ Thin (**50** µm) sensor 32x64 pixels
- ▷ Pitch 50x75 µm^2

- ▷ SwitcherB and DCDB at full speed
- ▷ Belle II prototype power supply
- ▷ DCDB readout at 320 MHz → **100 ns row time**

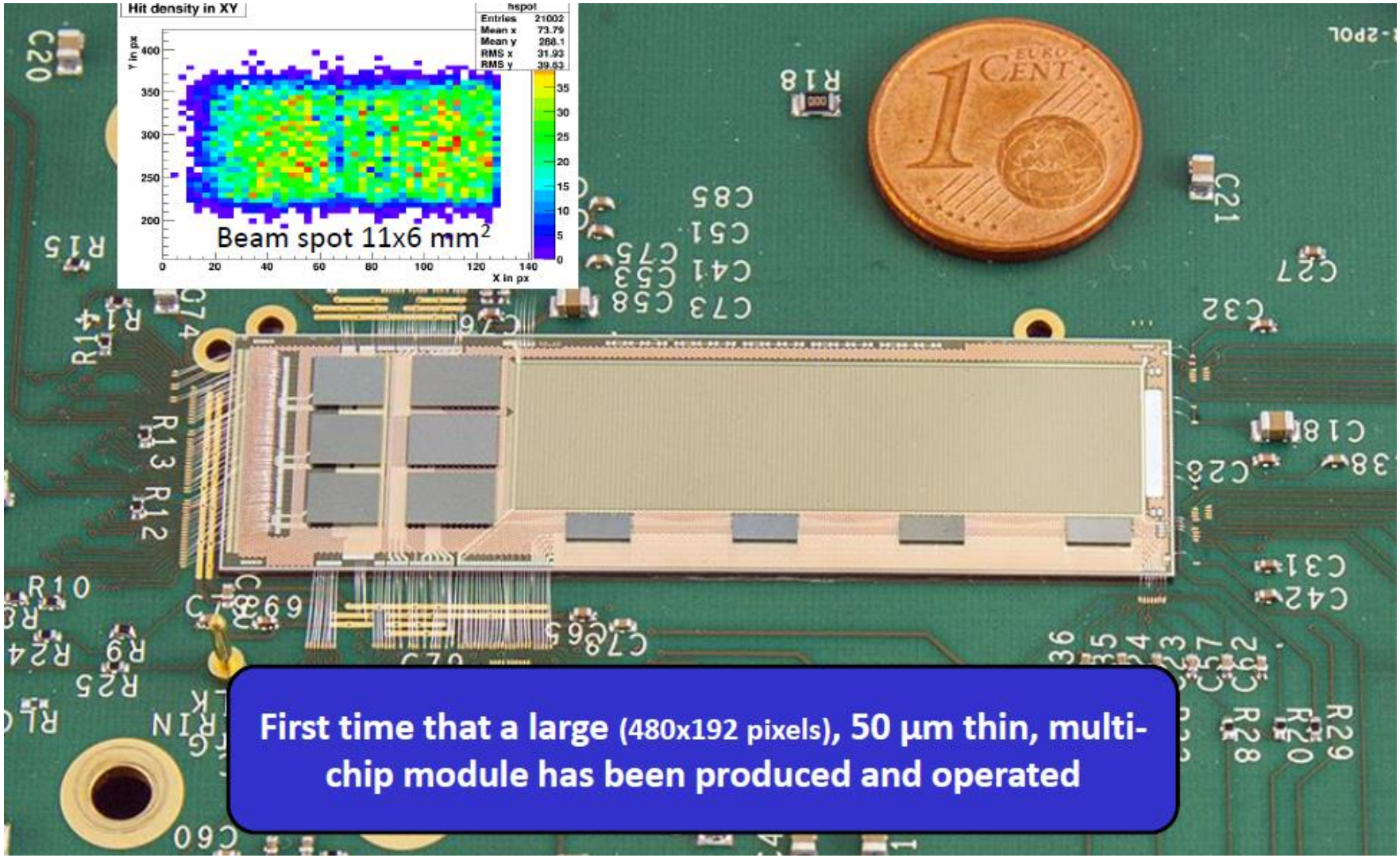
- ▷ 99% Efficiency
- ▷ S/N for MIPs: 20-40 depending on gate length



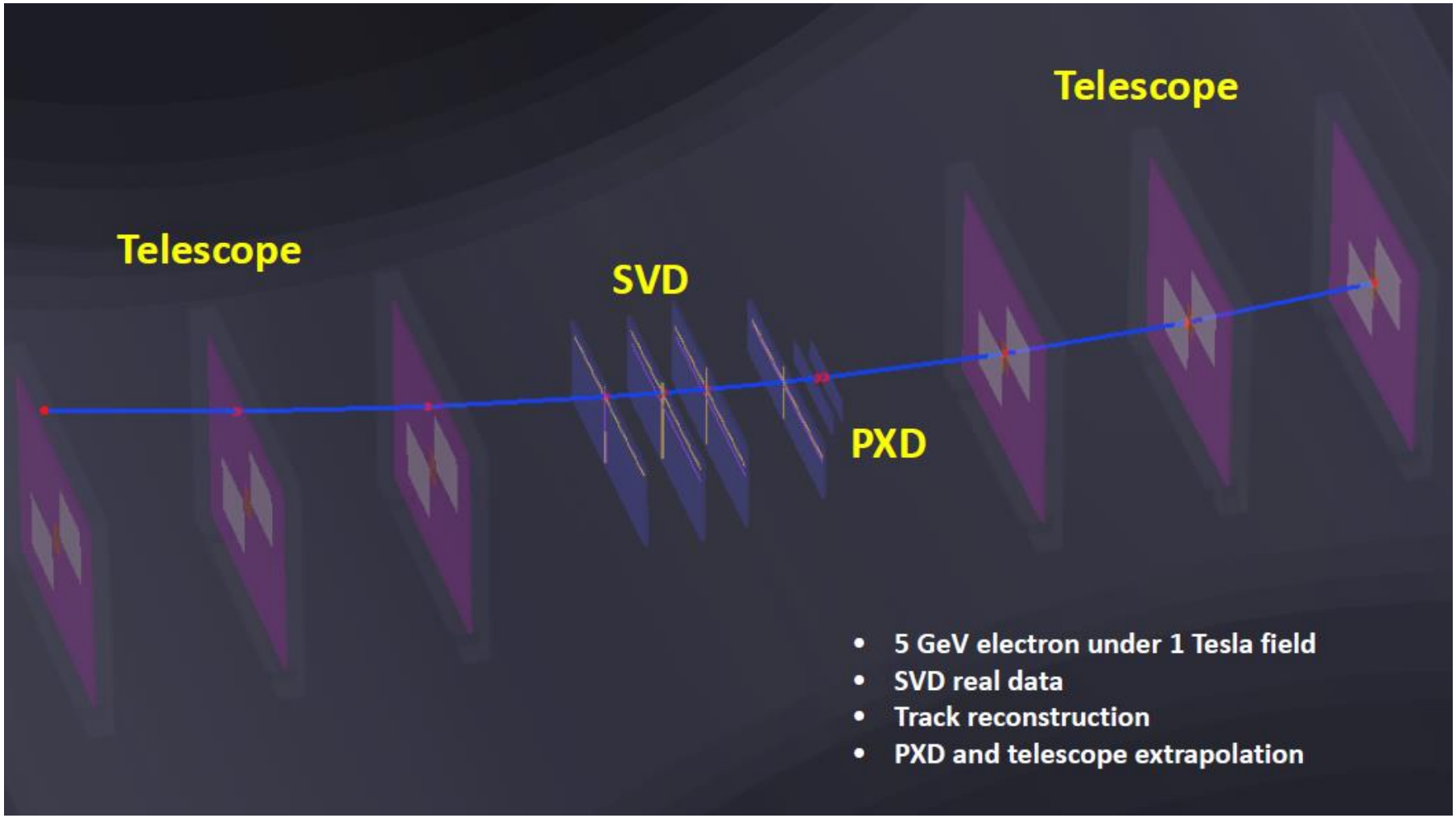




Belle II system test in the DESY Beam

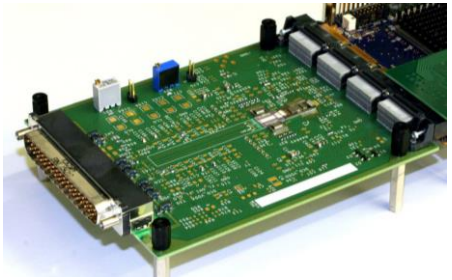


Belle II system test in the DESY Beam



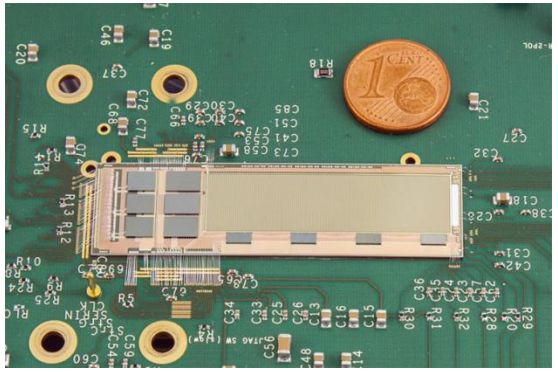
Towards a real ladder

Transition from test systems to integrated modules

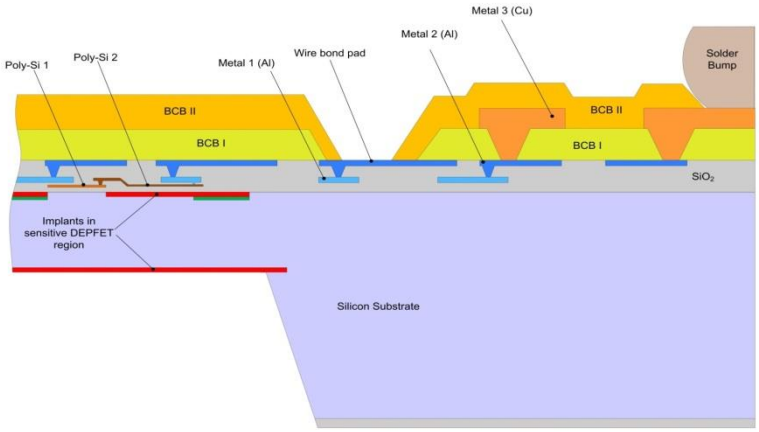


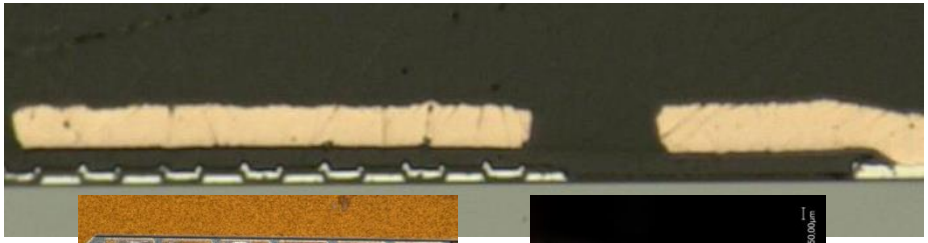
» PCB for the various matrices ….. "hybrids"

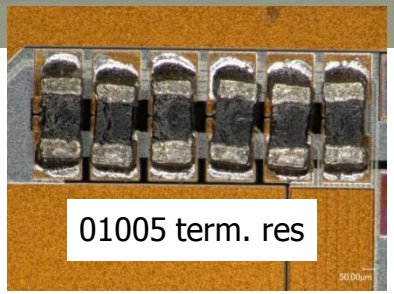
» first bump bonded chip on PXD6 prototype matrices
- ↳ 2 metal layers, not the final geometry, simple 3rd metal
- ↳ need still support PCB for I/O
- ↳ not perforated balcony

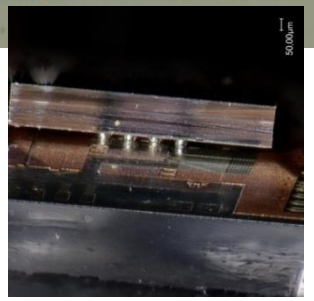


» Belle-II PXD Module (two modules form a ladder)
- ↳ **three metal layers, Cu as LM only on periphery**
- ↳ MCM: 4 DCD, 4 DHP, 6 Switchers → ~3000 bonds/module
- ↳ **Cu as UBM, bumps partly on thinned perforated frame**
- ↳ passive components soldered to substrate
- ↳ I/O and power over Kapton cable

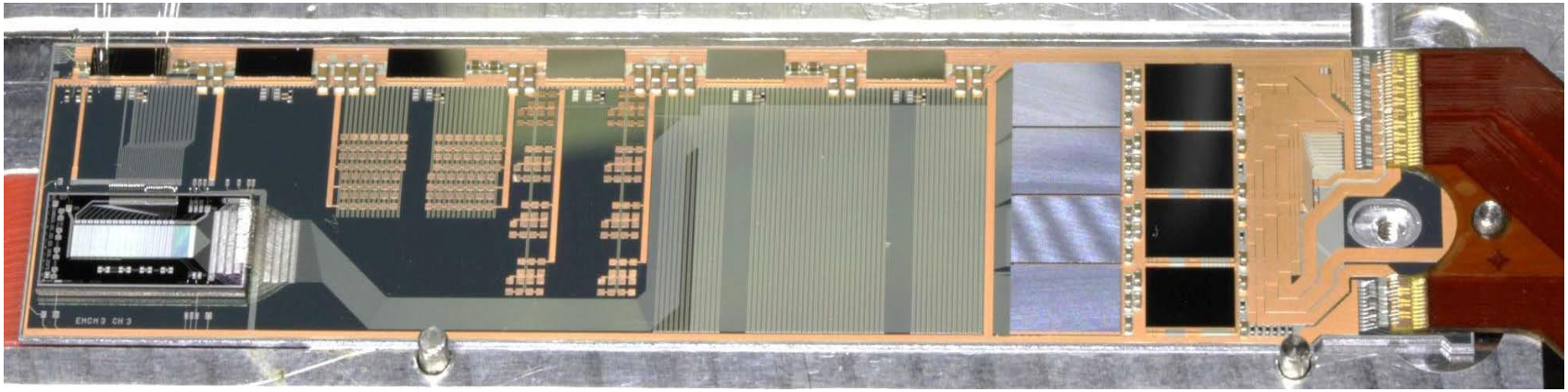


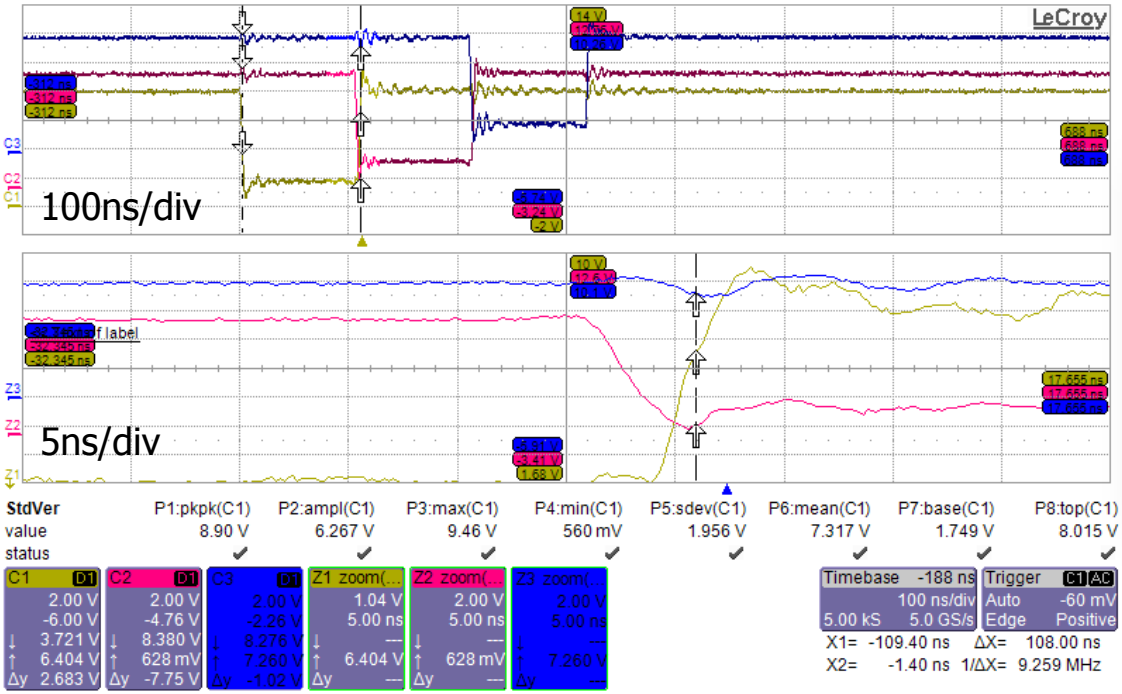






Test vehicle E-MCM





Extensive test program

- Interconnect technology
- Powering, control, DAQ
- Signal integrity, timing …
- …

Lessons learned are being applied to final module layout

DEPFET at the ILC: the challenges

☑ :- small pixels (~20µm) for excellent single point resolution (~3µm)

☑ :- speed: the DEPFET runs in a rolling shutter mode (read-out during the bunch train)

→ **~1/100ns row rate state of the art** (at Belle II)

→ our **goal is ~1/50ns** row rate

↳ under investigation with new DCDB pipeline

↳ Variable pixel size in z would help to reduce #pixels per column

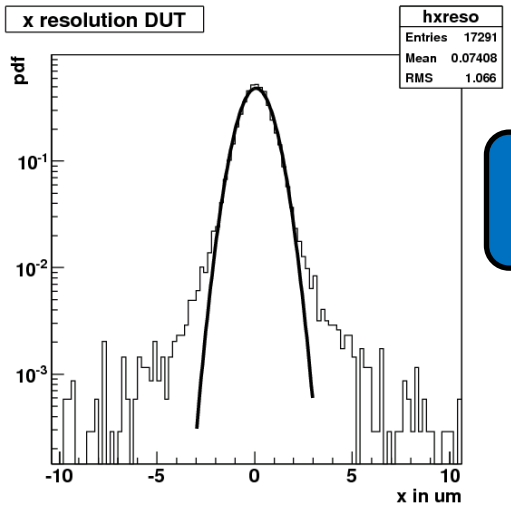
➔ :- minimal material down to very small angles

→ thinner sensors with large S/N

→ minimize support, services, and cooling material

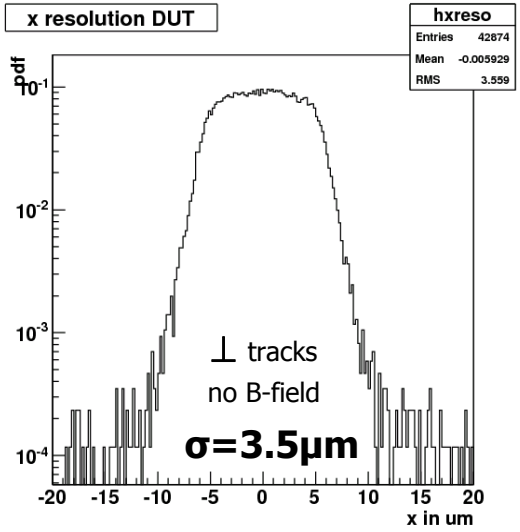
→ **low mass cooling**

→ **forward region??**



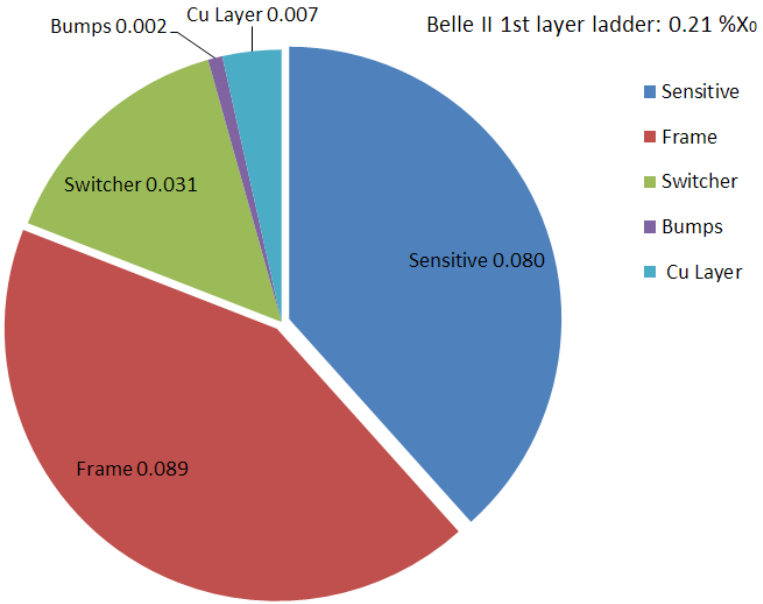
Test Beam Data
20x20x450 µm³
Single point resolution: 1 µm

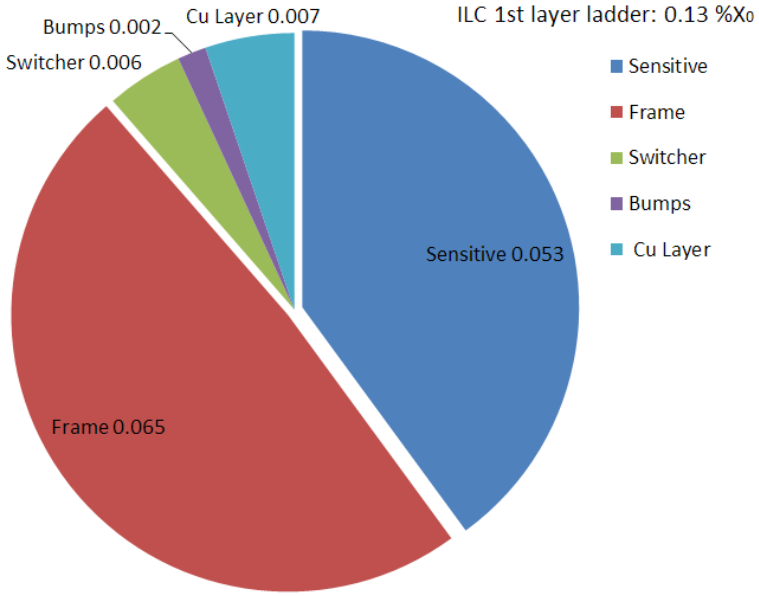
ILC (Simulation)
20x20x50 µm³
Single point resolution: 3.5 µm



'Physical limitations to the spatial resolution of solid-state detectors' arXiv:1404.4535

Reducing material in the barrel region

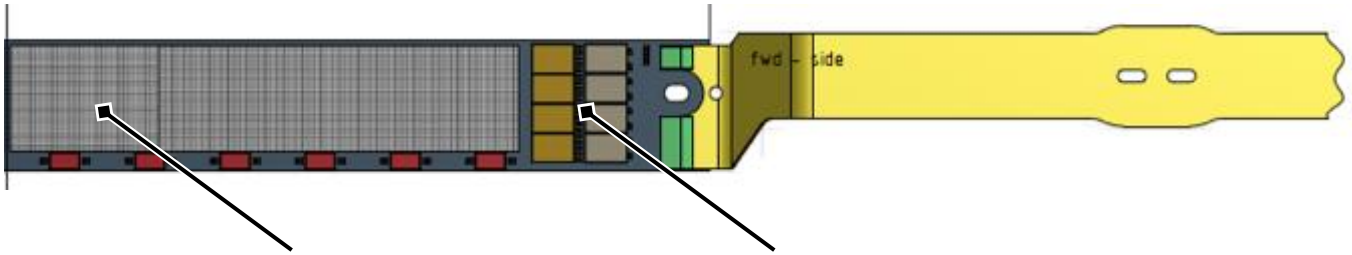




	Belle II	ILC
Frame thickness	525 µm	400µm
Sensitive layer	75 µm	50µm
Switcher thickness	500µm	75µm
Cu layer	only on periphery	only on periphery
Total	0.21 %X0	0.13 %X0

→ less material with small modifications/improvements of module technology within reach

Thermal management and material

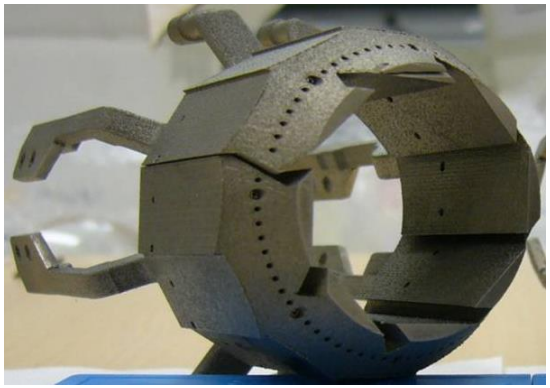


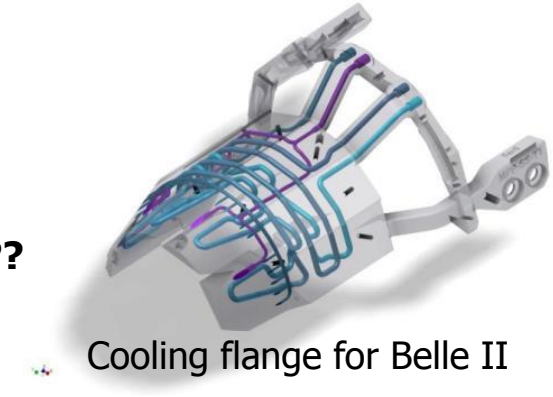
1W sensor&SWB → gas cooling

8W DCD&DHP

- Belle II
  - 9W/half ladder, 8W at EOS
  - Active (CO_2) cooling at EOS, cooling block
- Power distribution at ILC very similar
- Power pulsing → 1/200??, 1/100??, 1/50??
- Air cooling mandatory (and most likely possible)
- at EOS still high power density, active cooling might be needed

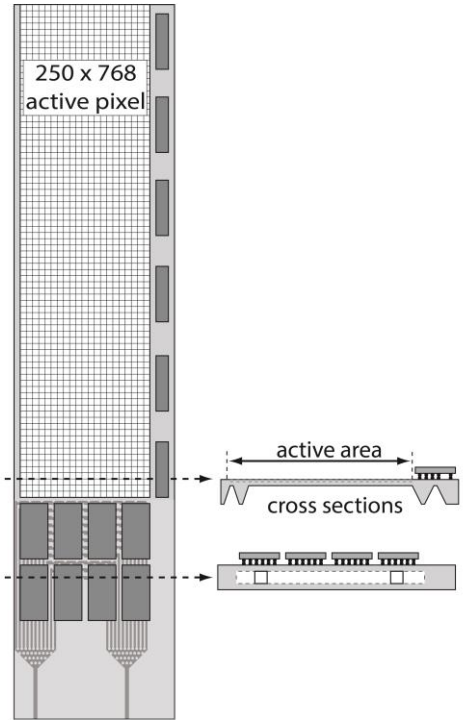
  → How about silicon integrated cooling channels there ????

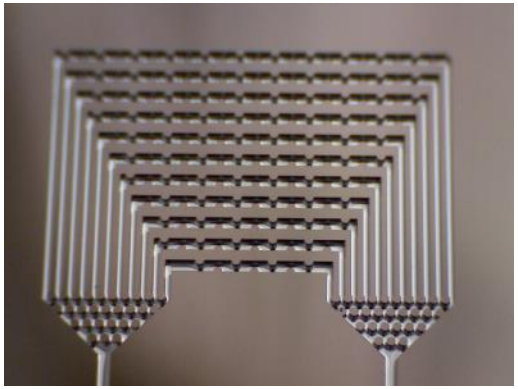


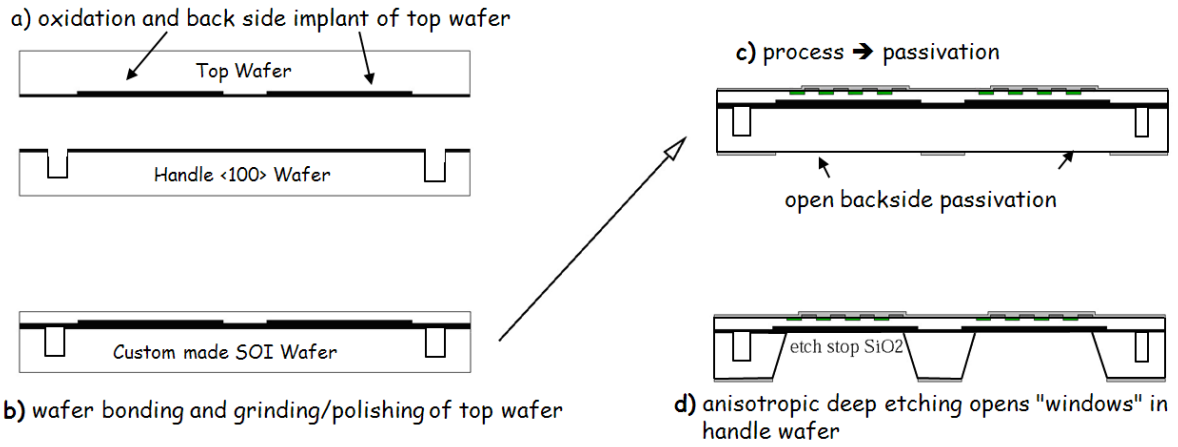


Cooling flange for Belle II

Integrated micro-channels



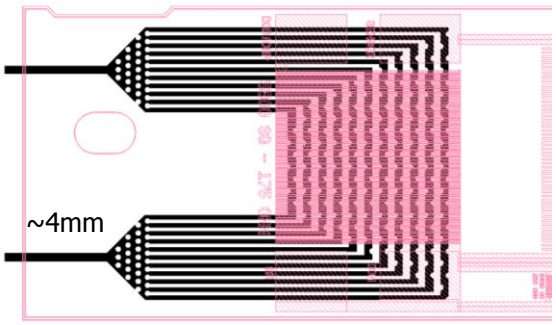


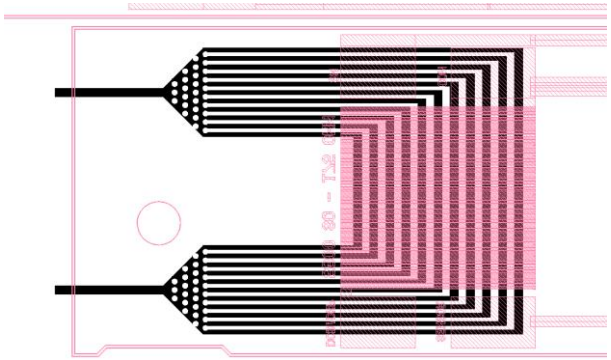


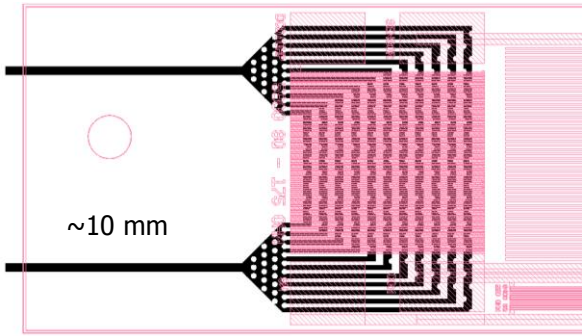
A spin-off of SOI approach : thinned all-silicon module with integ. cooling

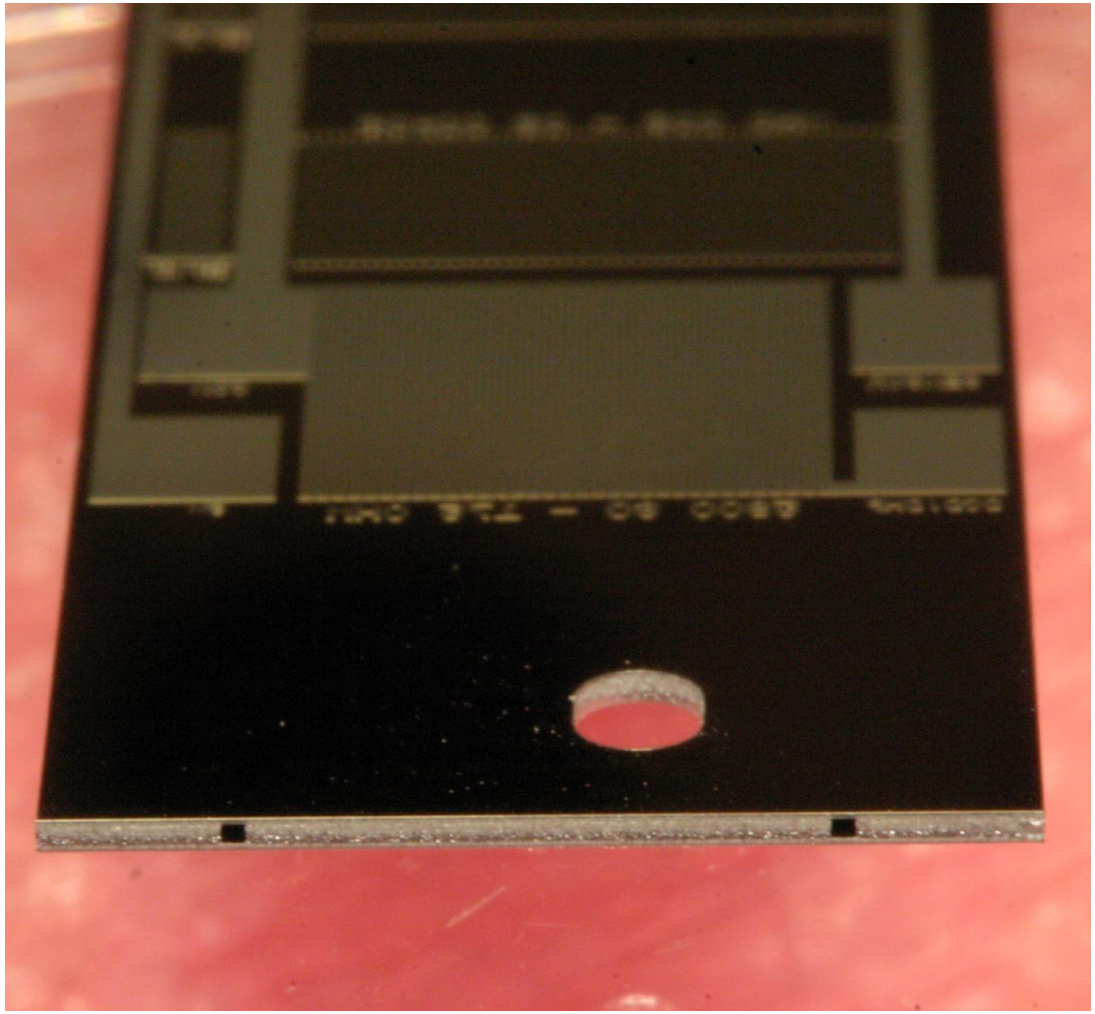
:- idea: integrate channels into handle wafer beneath the ASICs
:- channels etched before wafer bonding → cavity SOI (C-SOI)
:- full processing on C-SOI, thinning of sensitive area
:- micro-channels accessible only after cutting (laser)

feasibility study



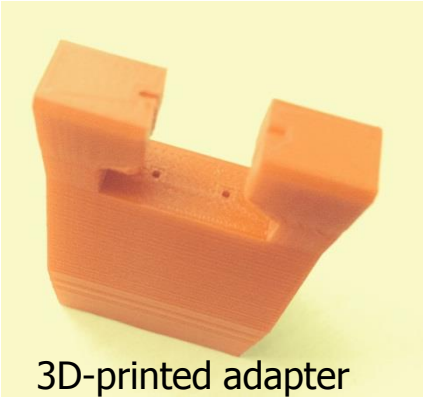




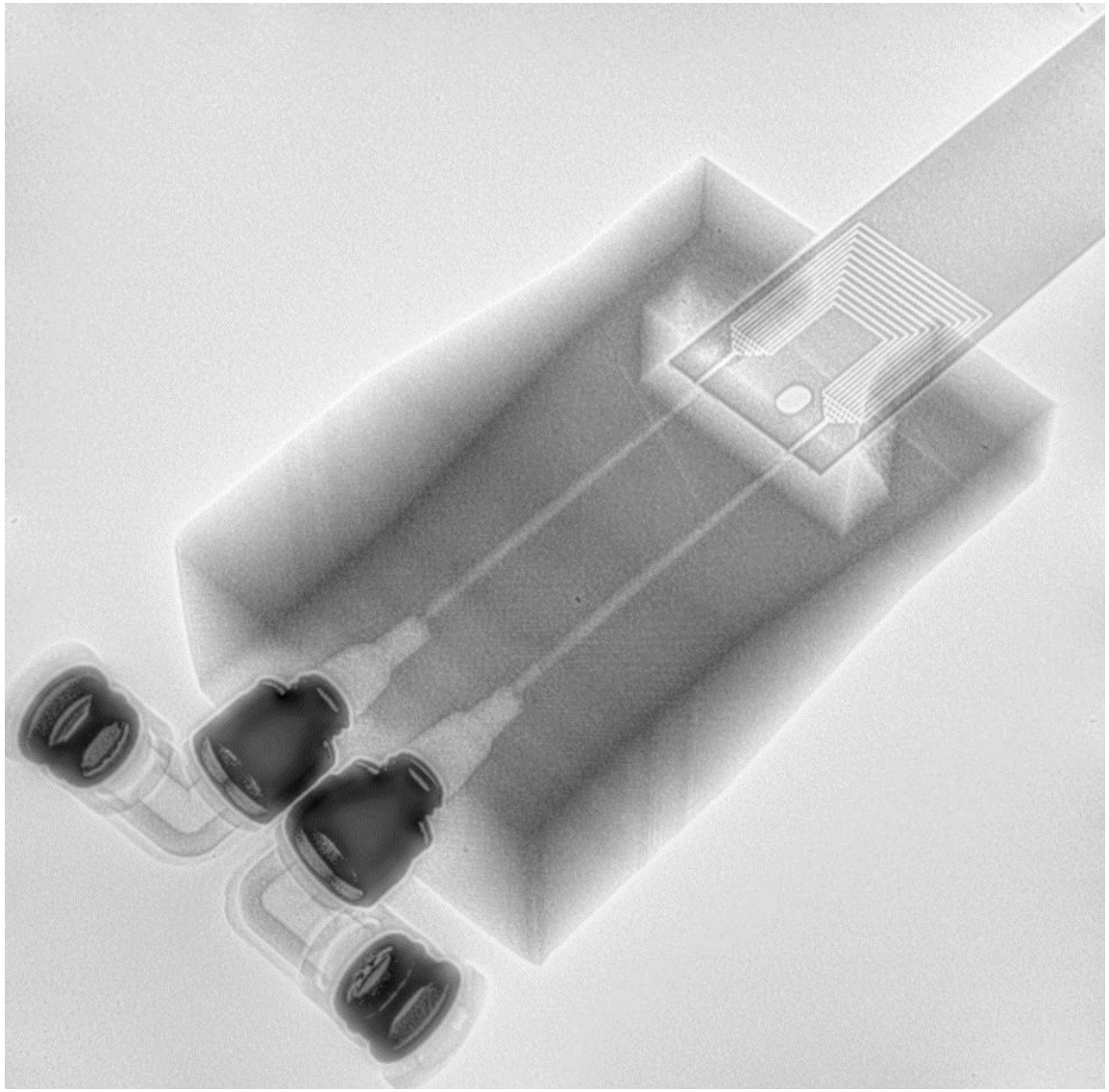


feasibility study

PEEK tubes with 360 µm OD



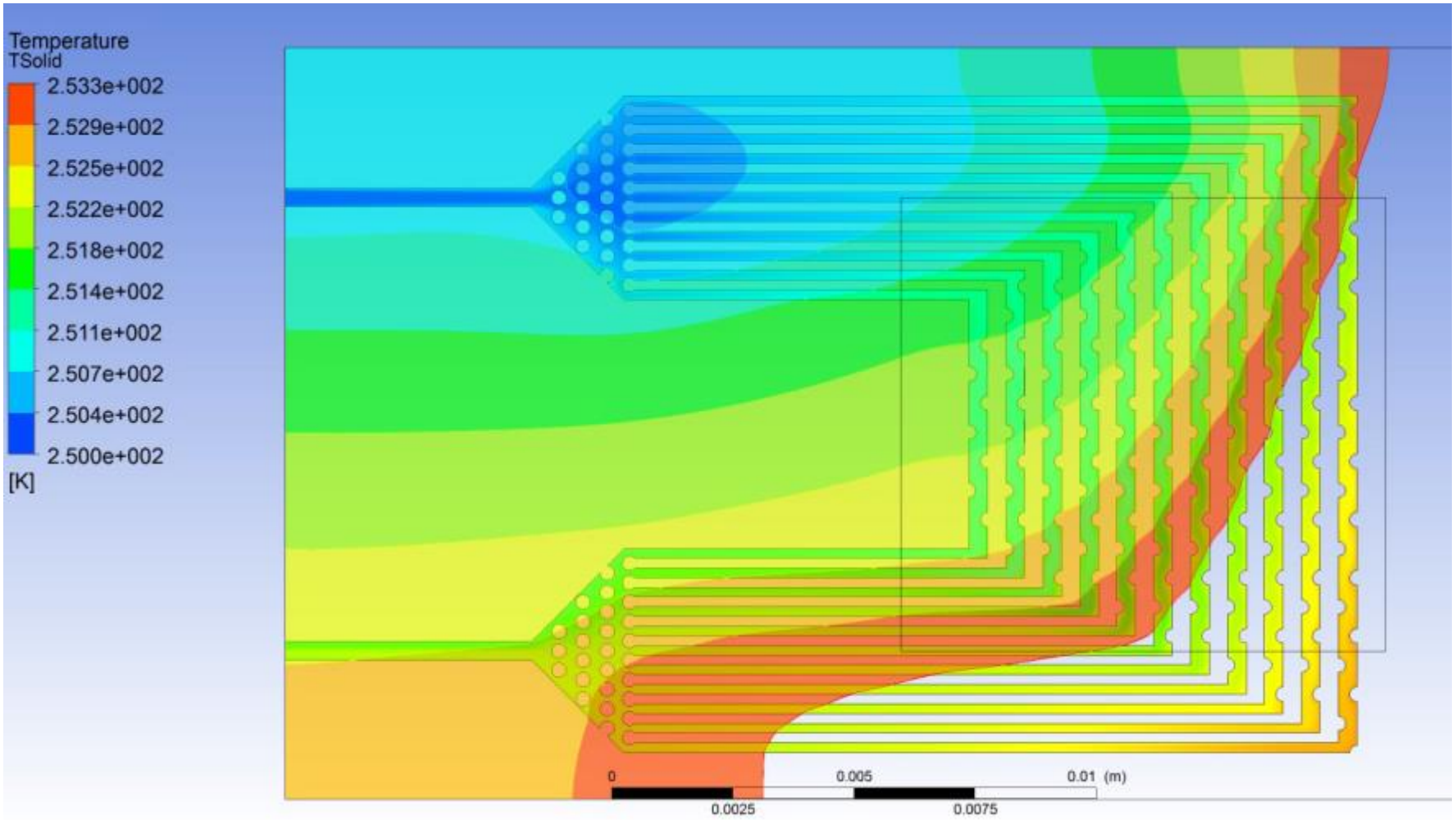
3D-printed adapter



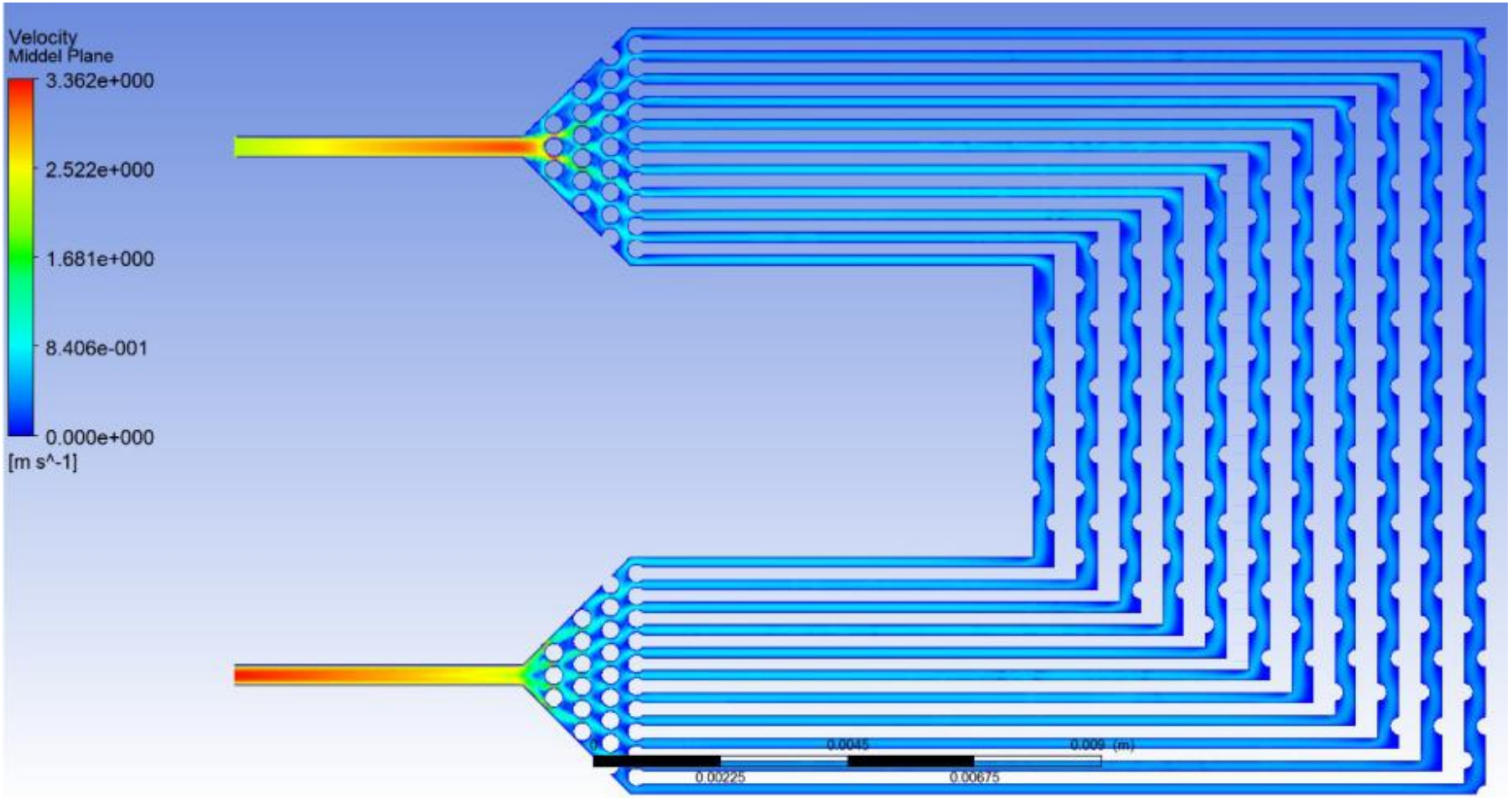
Water cooling

Very effective cooling! "Large" ΔT expected and confirmed by simulation (just water!!)

Simulated temperature profile

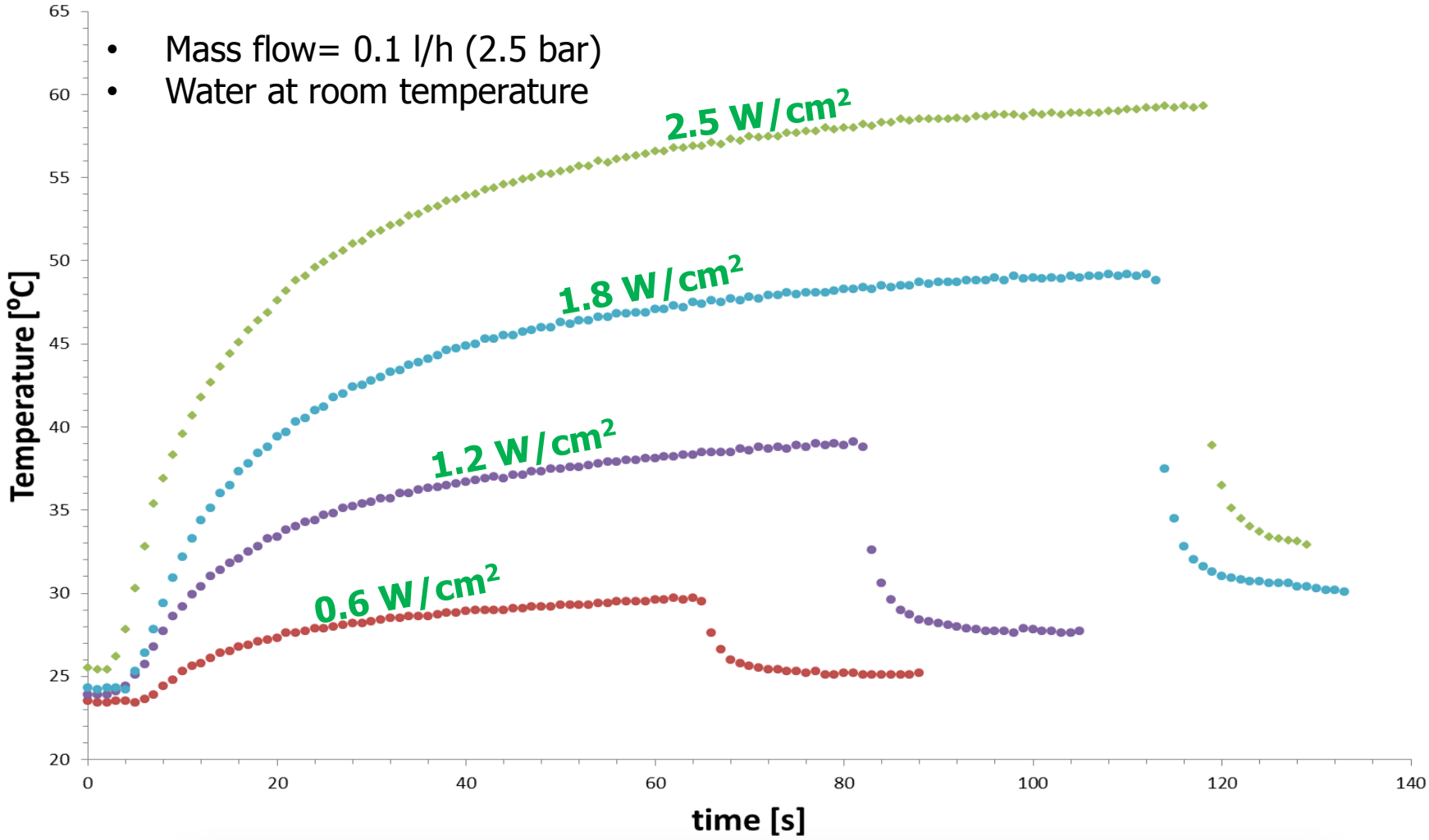


Simulated velocity profile (water)



→ non-optimal corners, new layout currently under study

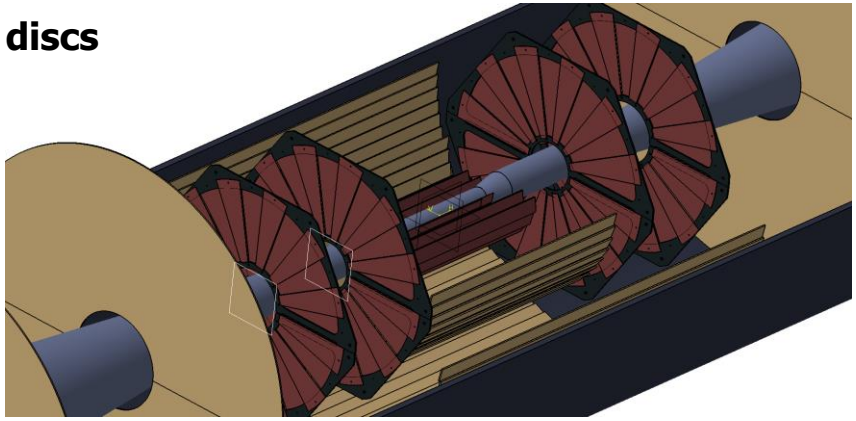
temperature vs. time



Extremely encouraging first results!! To be continued in the framework of AIDA H2020

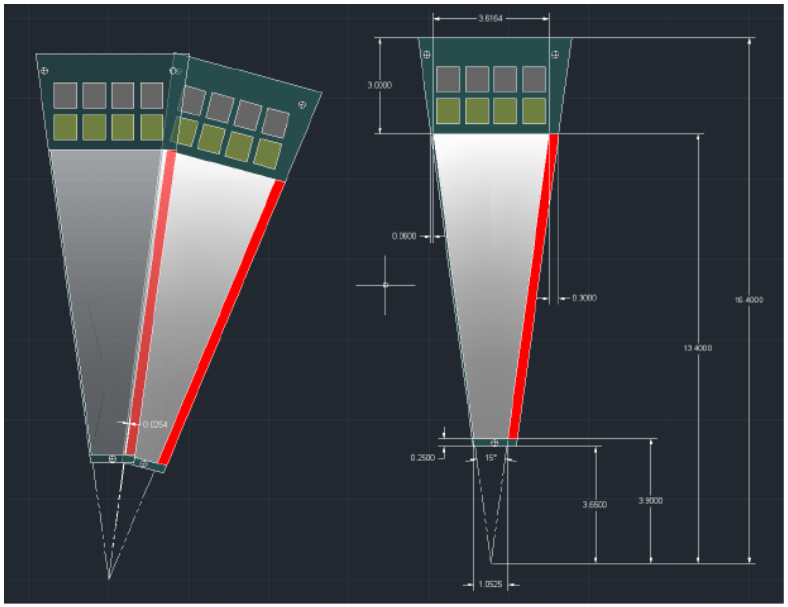
Stepping forward – all-silicon petal

LC Detector concepts require pixelated forward discs



» SiD : vertex detector end-cap
» ILD : forward tracking discs

→ Adapt all-silicon ladder to the forward region: **"all-silicon" DEPFET pixel petal**

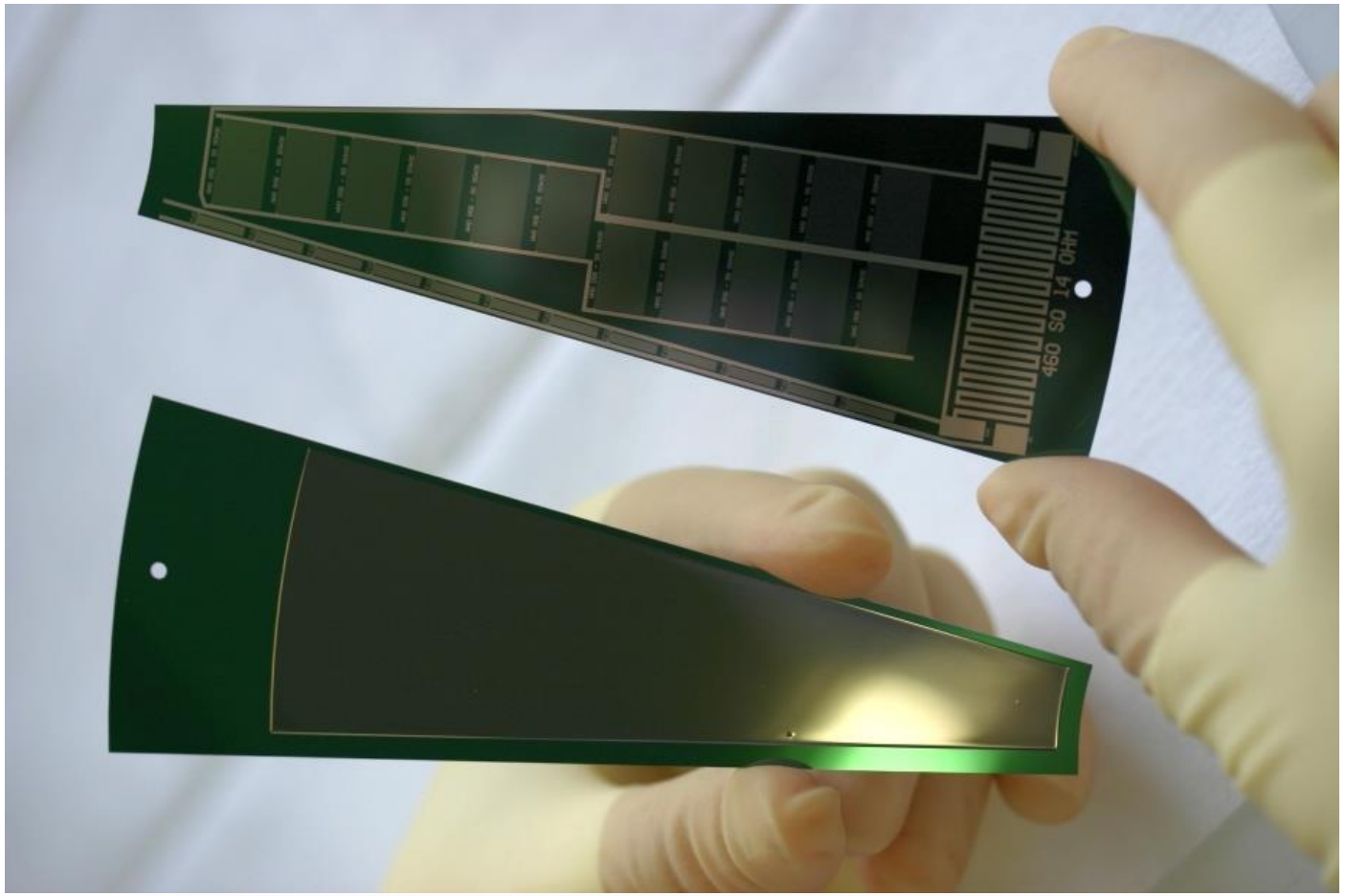


Concept

» Thin sensitive region: R= 3.9 to 13.4 cm
» Radially varying pixel size
» r/o at the outer edge with bump bonded ASICs
» Steering ASICs on frame

» Technology as for the barrel all-silicon ladder
  ↳ SOI wafer, etched back to SiO2
  ↳ if needed add narrow radial support bars

- all-silicon petal



Total silicon area:	~34 cm²
"sensitive" unsupported thin silicon (here 75µm):	~21 cm²
Material (500 µm support, 75 µm sensitive):	~0.18% X0
→ 400µm support + 50 µm sensitive:	~0.14% X0

Summary

- **The DEPFET Belle II all-silicon module is to a large extent a prototype for a ILC vertex detector**
  - **Read-out and steering ASICs flip-chipped to the sensor silicon**
  - **average material budget 0.21 %X_0 including all support material**

- **Further reduction of the material budget possible → 0.13 %X_0**
  - **Reduce support silicon by ~125 µm**
  - **Thinner steering ASICs on the "balcony" (~75µm)**

- **New exclusively ILC related activities are:**
  - **Micro-channel cooling at the end-of-stave**
  - **feasibility study for all-silicon DEPFET forward discs**

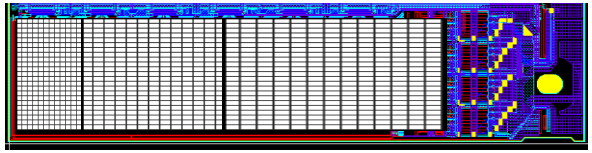
Requirement II: higher read-out speed

» 100ns per r/o → 2048 rows per half-ladder, 2-fold r/o → **~1/100µs frame rate state of the art**

» possible improvements (with current f/e electronics and ADC)

↳ **Sensor technology**: a third metal layer in the sensitive area is within reach

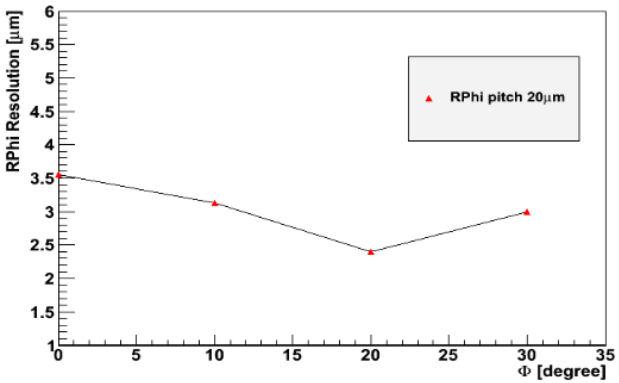
→ 4-fold read-out with small pixels → **1/50µs frame rate**



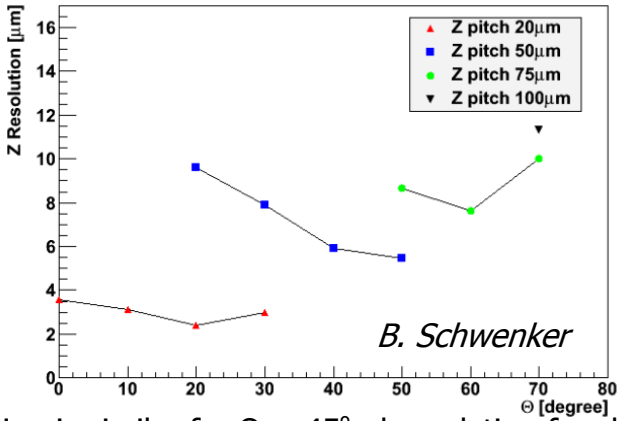
↳ **optimization** of cluster size for shallow(er) tracks

→ Introduce three regions in z with ~25µm/50µm/100µm pixel pitch in z (similar to Belle II)

→ #rows reduced by factor ~2 → **1/25 µs frame rate possible**



rφ-resolution varies between 2.3 - 3.5 µm



z-resolution is similar for Θ < 45°, degradation for shallower tracks

→ state of the art is factor 2 too low for ILC vertexing
↳ improve technology
↳ optimize pixel size, improve technology

Requirement I: better single point resolution

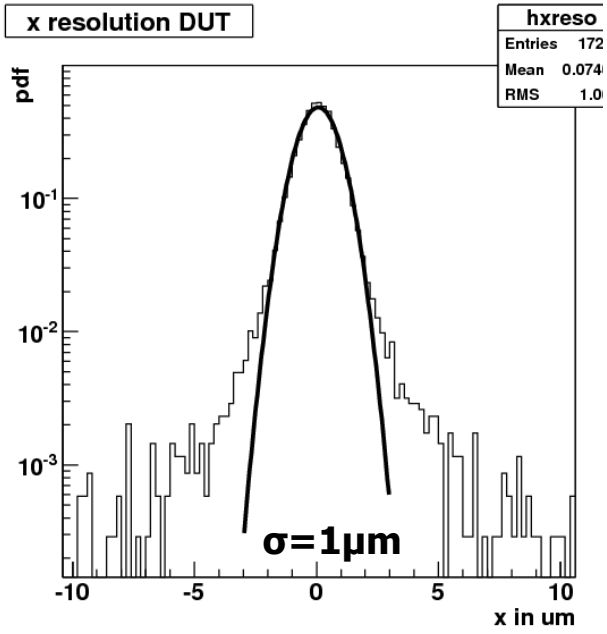
Test Beam Data
20x20x450 µm³
Single point resolution: 1 µm

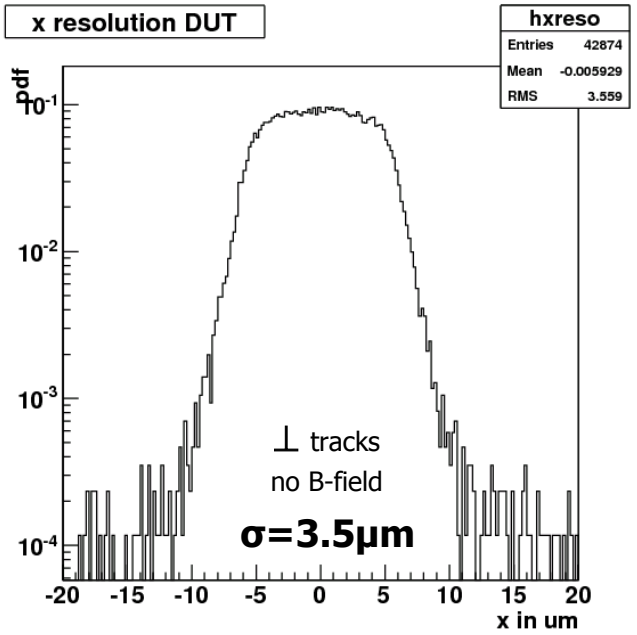
→

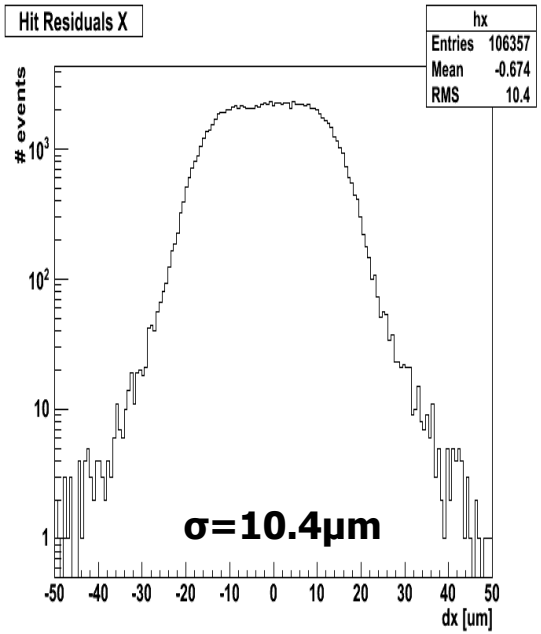
ILC (Simulation)
20x20x50 µm³
Single point resolution: 3.5 µm

←

Test Beam Data
50x50x50 µm³
Single point resolution: 10.4 µm

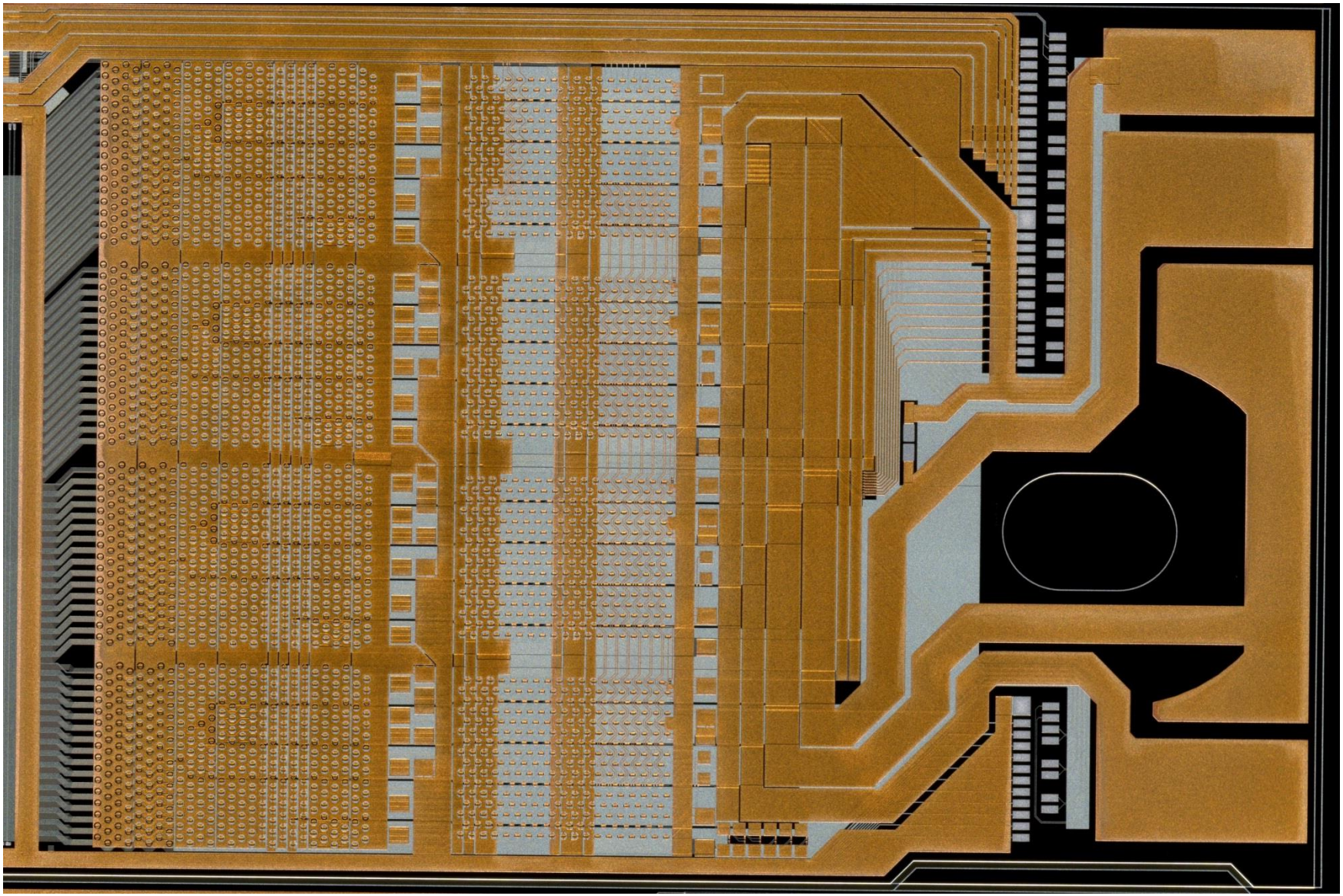




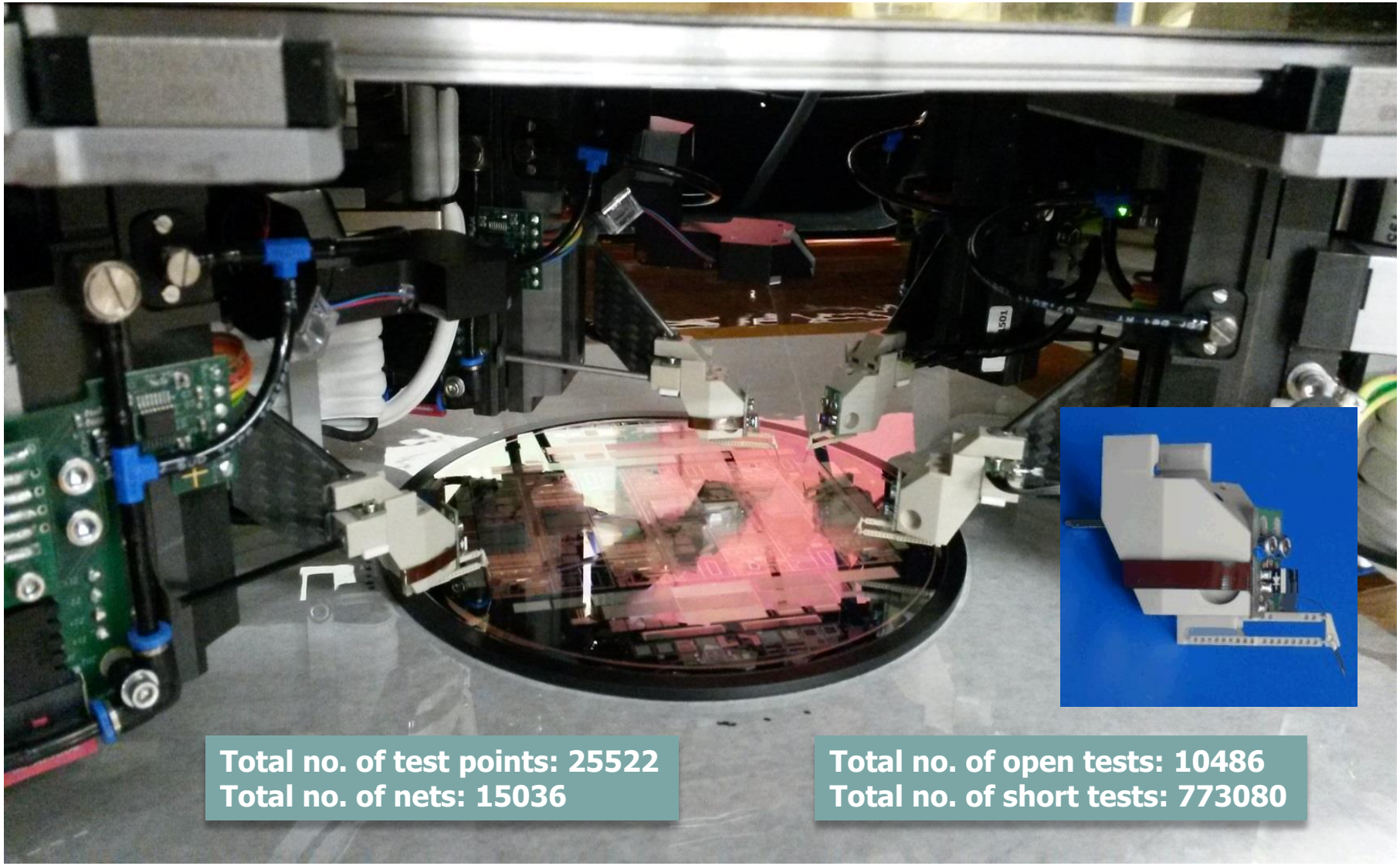


→ Required single point resolution with small DEPFETs achievable

The end of stave (EOS)



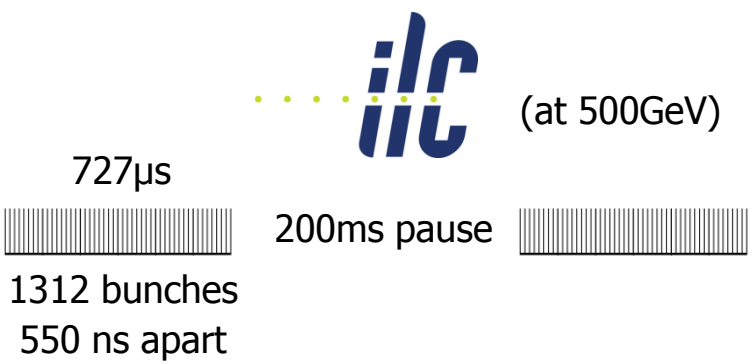
flying needle tester

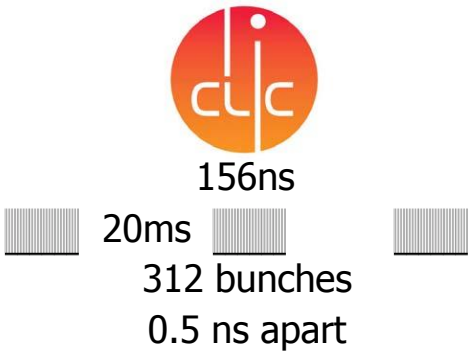


Vertexing at a LC

- From the pixel sensor point of view there is no such thing like "the" linear collider!
  - ILC with various CM energies
  - and CLIC with up to 3TeV

- Beam structures of ILC and CLIC are very different

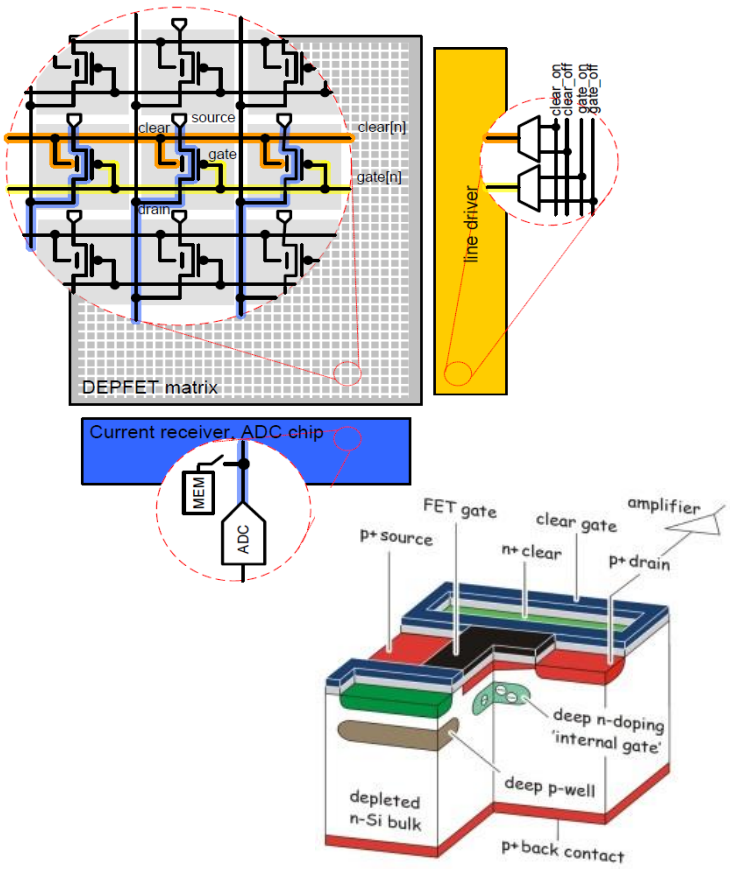




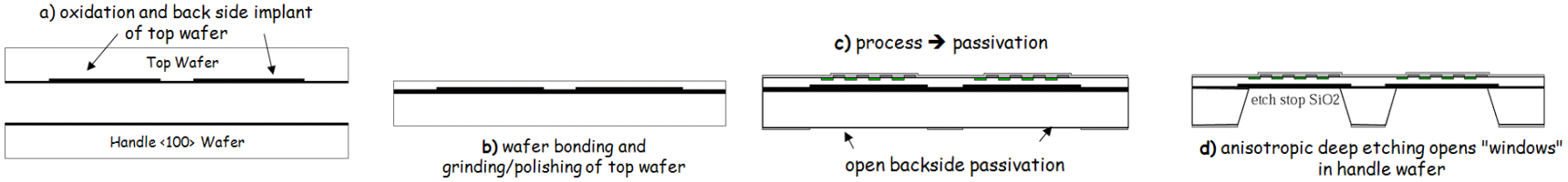
- The DEPFET approach takes advantage of the beam structure at the ILC
  - record and transmit 15-20 frames per train in "rolling shutter" mode
  - Stand-by during pause to reduce over-all power consumption

- CLIC would (probably) require time stamping of frames read during train

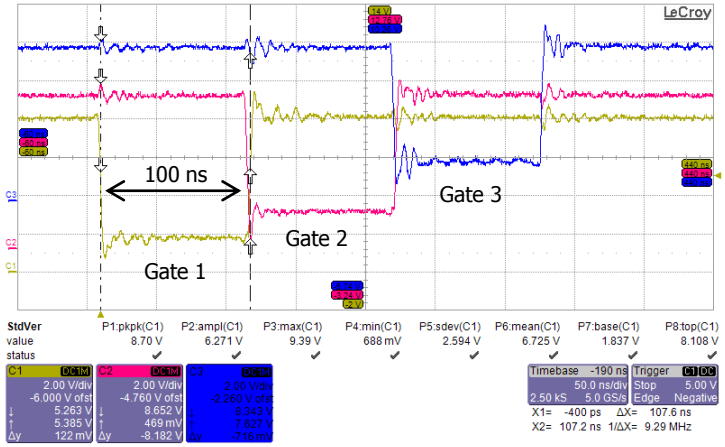
DEPFETs in a nutshell

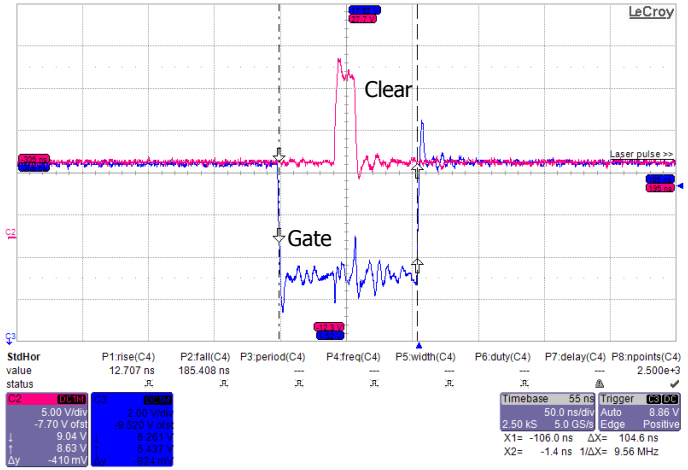


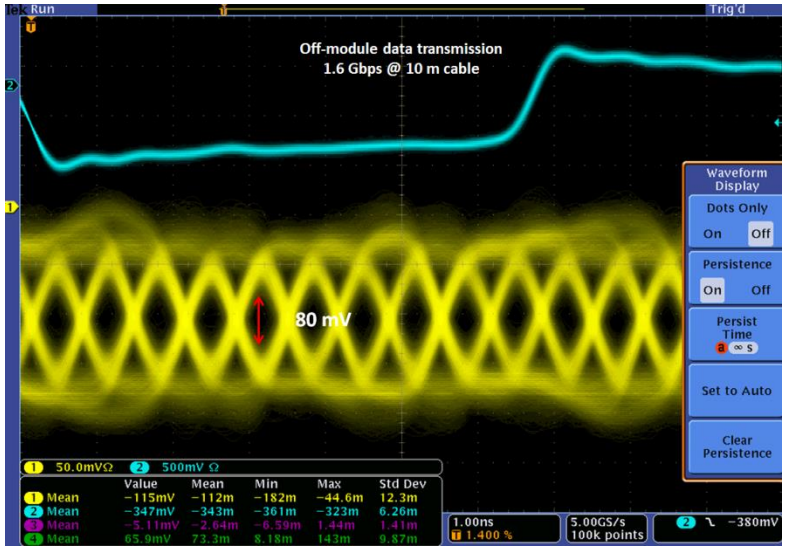
- **fully depleted sensitive volume**
  - fast signal rise time (~ns), small cluster size
- In-house fabrication at MPG HLL
  - **Wafer scale devices possible**
  - **Thinning to (almost) any desired thickness**
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- **Charge collection in "off" state, read out on demand**
  - potentially low power device
- **internal amplification**
  - charge-to-current conversion
  - r/o cap. independent of sensor thickness
  - **Good S/N for thin devices → ~40nA/µm for mip**

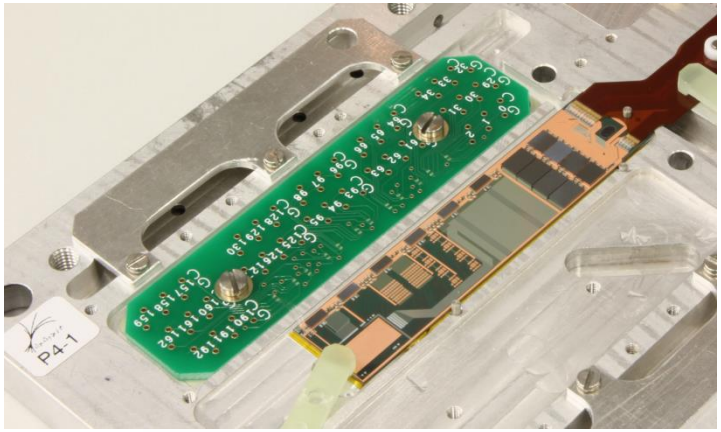


First test results – Gate, Clear and signal transmission



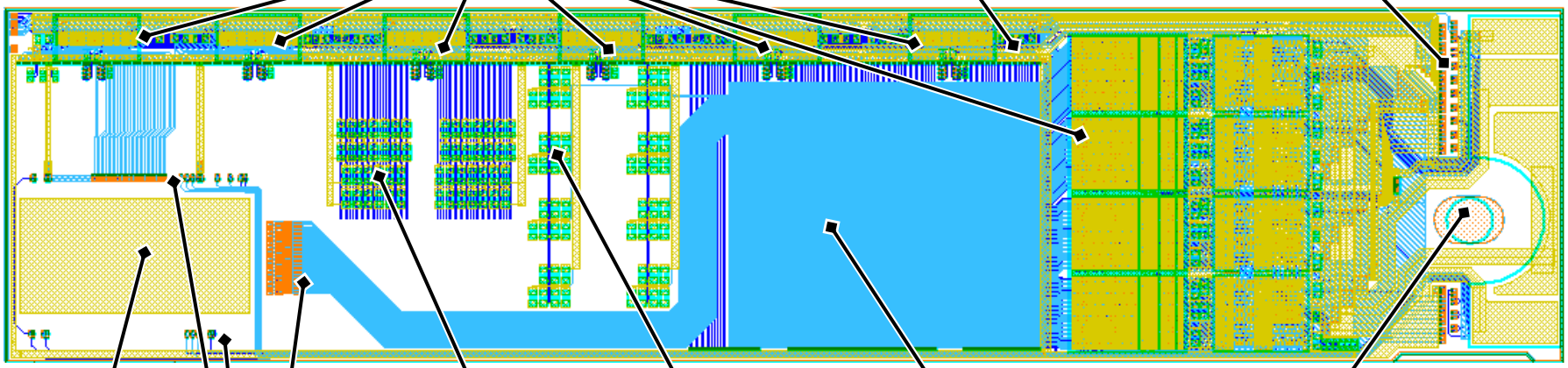






Next step is to mount a small DEPFET Matrix and test performance on the Bench and in a test beam

E-MCM – everything but the DEPFET



- Electronic Multi-Chip Module
- basically an electrically active prototype of half-ladder
- even beam tests are possible with small piggy-back matrix