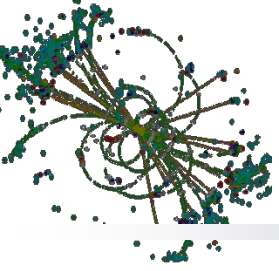# Chronopixel status

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University of Oregon, Eugene

In collaboration with J.E.Brau, D.M.Strom (University of Oregon, Eugene, OR), C.Baltay, W.Emmet, D.Rabinovitz (Yale University, New Haven, CT)
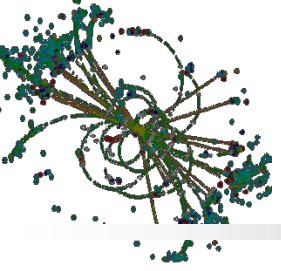
EE work is contracted to Sarnoff Corporation

Outline of the talk

- **Very brief reminder of Chronopixel concept:**
  - **Chronopixel is a monolithic CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and record the time (time stamp) of each hit.**
- **Original concept.**
- **Project milestones.**
- **Summary of prototypes 1 and 2 tests.**
- **Changes in prototype 3**
- **Sensor options discussion**
- **First results of prototype3 tests**
  - **main problem discovered in prototype 2 is <u>solved</u> !**
  - **noise, calibration, etc.**
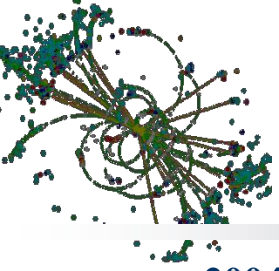- **Results discussion**
- **Summary and plans**

Our initial ultimate design concept

○ **Ten years ago we thought, that to provide full charge collection by the sensor electrode, we need DEEP PWELL implemented by manufacturer, to prevent competing charge collection by bodies of PMOS transistors.**
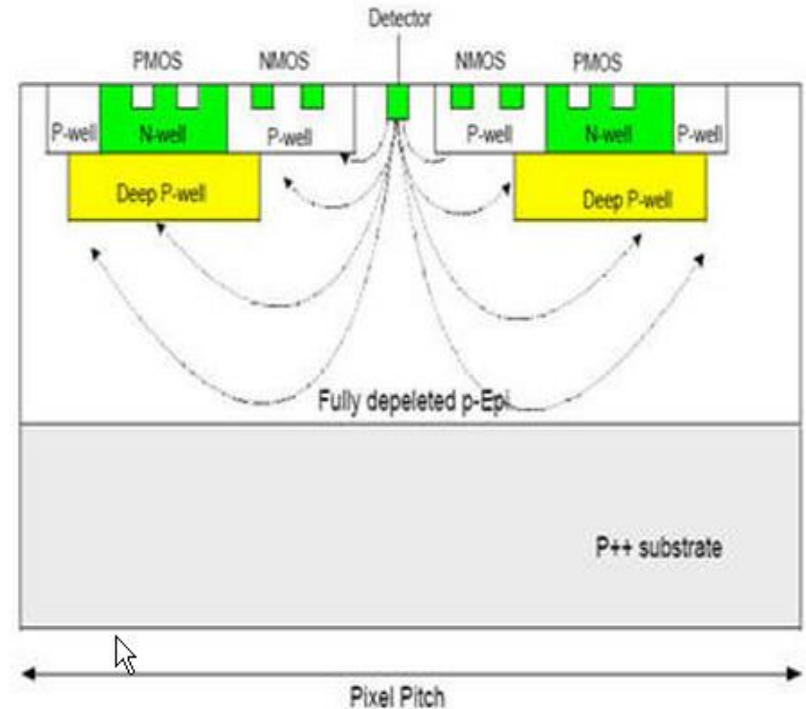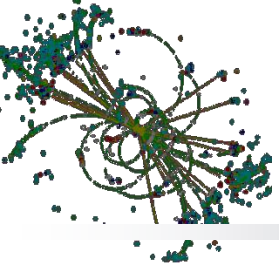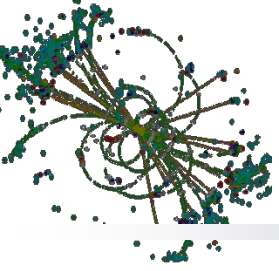
Timeline

- **2004 – talks with Sarnoff Corporation started.**
  - Oregon University, Yale University and Sarnoff Corporation collaboration formed.
- **January, 2007**
  - Completed design – Chronopixel
    - **2 buffers, with calibration**
- **May 2008**
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 μm $\Rightarrow$ ~50 μm pixel
    - Epi-layer only 7 μm
    - Low resistivity (~10 ohm*cm) silicon
- **October 2008**
  - Design of test boards started at SLAC
- **September 2009**
  - Chronopixel chip tests started
- **March 2010**
  - Tests completed, report written
- **May 2010**
  - contract with Sarnoff for developing of second prototype signed
- **September 2010**
  - Second prototype design started

- **October 2010 - September 2011**
  - Sarnoff works stalled
- **February 2012**
  - Submitted to MOSIS for production at TSMC. (48x48 array of 25 μm pixel, 90 nm process)
  - Modification of the test stand started as all signal specifications were defined.
- **June 6, 2012**
  - 11 packaged chips delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
  - Tests at SLAC started
- **March 2013**
  - Test results are discussed with Sarnoff and prototype 3 design features defined
- **July 2013**
  - **Contract with Sarnoff signed**
- **April 2014**
  - **Design submitted for fabrication**
- **August 13, 2014**
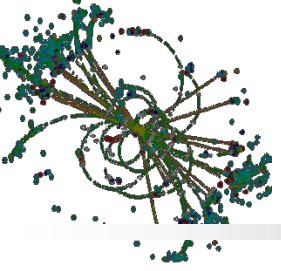 - Packaged chips arrived at SLAC

Prototype 1 summary

- Tests show that general concept is working.
- Noise figure with "soft reset" is within specifications (0.86 mV/35.7μV/e = 24 e, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is 2.7 times larger required (250 e).
- Sensors leakage currents ($1.8 \cdot 10^{-8}$A/cm^2) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz.
- No problems with pulsing analog power.
- Pixel size was 50x50 μm^2 while we want 15x15 μm^2 or less.
- However, CMOS electronics in prototype 1 could allow high charge collection efficiency only if encapsulated in deep p-well. This requires special process, not available for smaller feature size?
- Digital comparators offset compensation circuit limited our ability to reach required accuracy
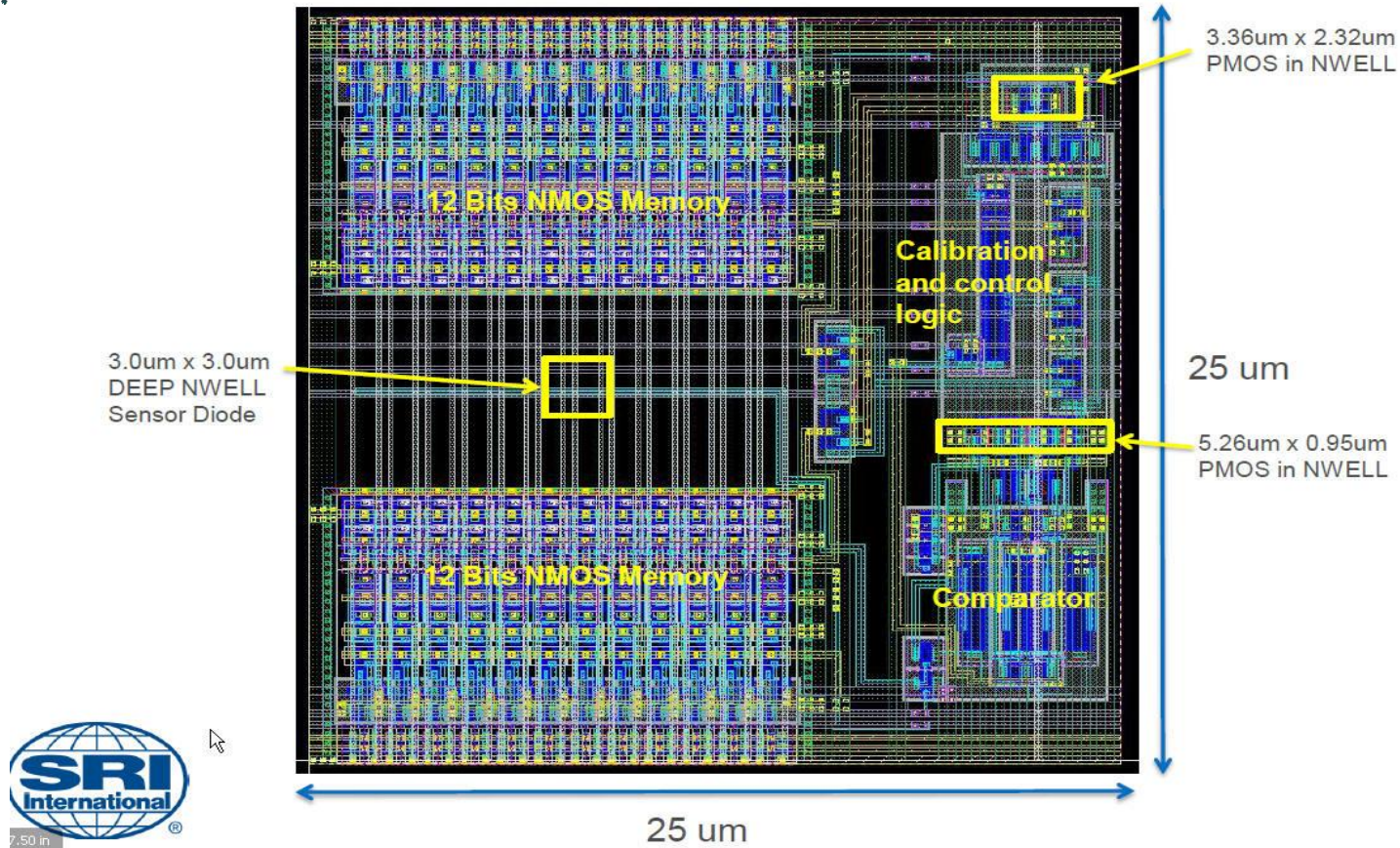
Prototype 2 features

- Design of the next **prototype** was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all **electronics inside pixels** only from **NMOS** transistors. It can allow us to have **100% charge** collection **without** use of **deep P-well** technology, which is expensive and rare. To reduce all NMOS logics power consumption, **dynamic memory cells design** was proposed by SARNOFF.

- **New** comparator offset compensation ("**calibration**") scheme was suggested, which **does not have limitation in the range** of the offset voltages it can compensate.

- We agreed **not to implement sparse readout** in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.

- In September of 2011 Sarnoff suggested to build next prototype on **90 nm** technology, which will allow to reduce pixel size to **25μ x 25μ**

- We agreed to have **small fraction** of the electronics **inside pixel** to have **PMOS** transistors. Though it will reduce charge collection efficiency, but will **simplify comparator** design. It is very **difficult** to build good comparator with **low power** consumption on **NMOS only** transistors.
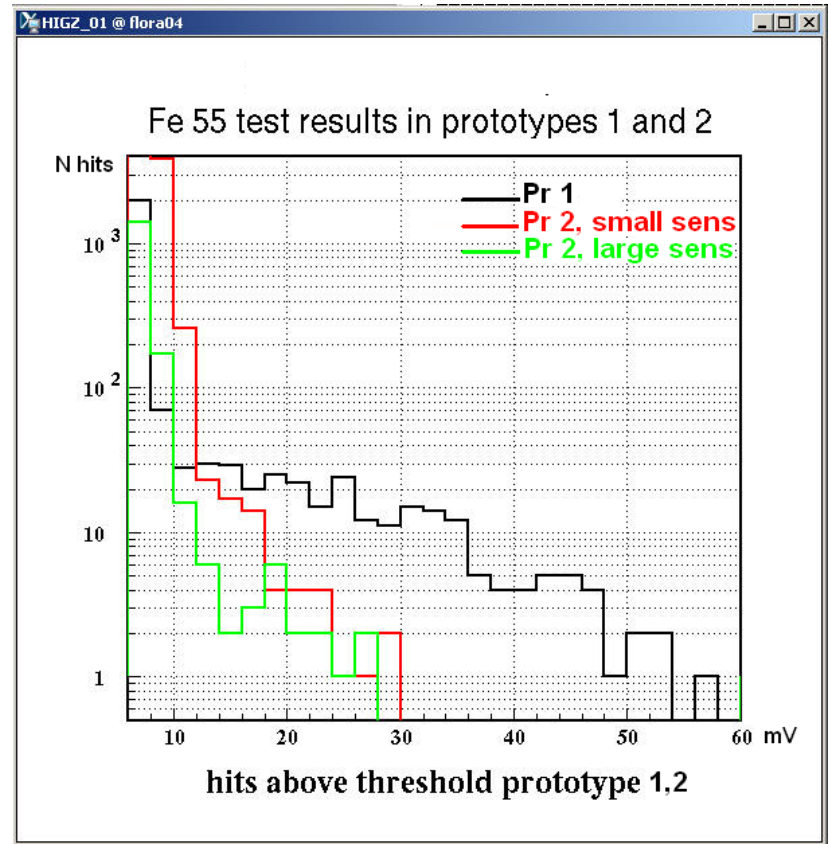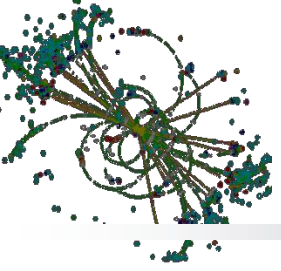
Prototype 2 pixel layout

3.36um x 2.32um
PMOS in NWELL

12 Bits NMOS Memory

Calibration
and control
logic

25 um

3.0um x 3.0um
DEEP NWELL
Sensor Diode

5.26um x 0.95um
PMOS in NWELL

12 Bits NMOS Memory

Comparator

25 um

12

All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP NWELL), half of the pixels have it's size increased to 4x5.5 μ^2 .
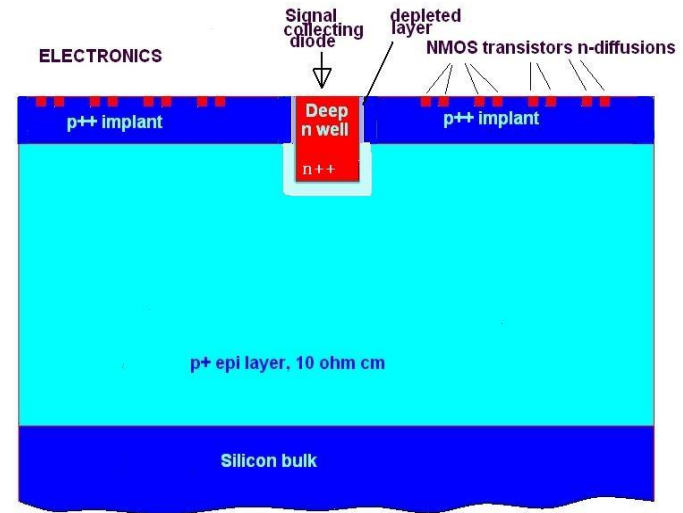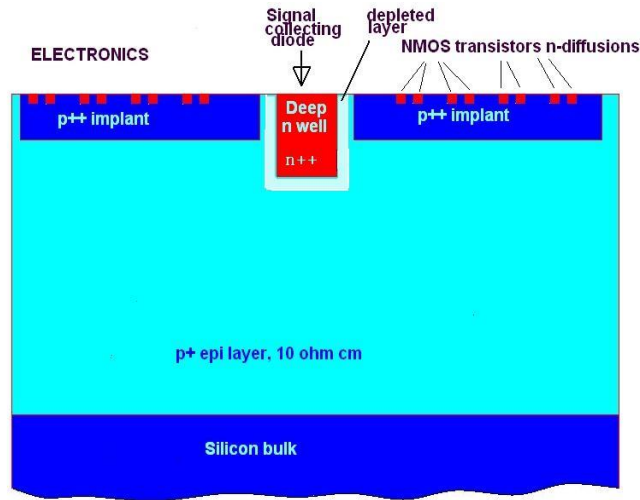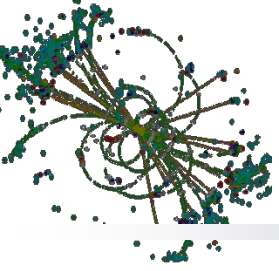
Test results – sensor capacitance

○ **Comparison of the Fe 55 signal distributions for prototype 1 and 2. Prototype 2 has 2 sensor size options – 9 μ² and 22 μ² ("small" and "large" on the plot) . The maximum signal value is slightly larger for sensor of smaller size, as one would expect, however we would expect larger difference in maximum signal values here. But capacitance of the sensor from this measurements (~9 fF) appeared much larger than our expectation (~1-2 fF).**


Fe 55 test results in prototypes 1 and 2

Pr 1
Pr 2, small sens
Pr 2, large sens

hits above threshold prototype 1.2

What got wrong?

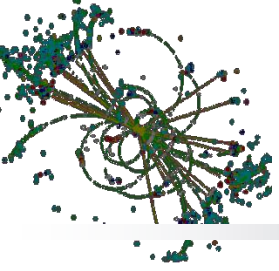o **We hoped, that pixel cross-section will look like what is shown on left picture. But it appeared, that in 90 nm design rules it is not allowed to have window in the top p++ implant around deep n-well, which forms our sensor diode. Resulting pixel cross-section is shown on right picture. Very high doping concentration of p++ implant leads to very thin depletion layer around side walls of deep n-well, which creates additional large capacitance.**
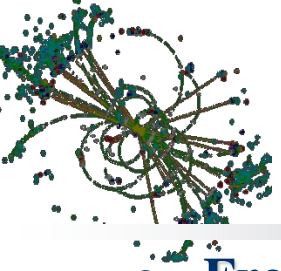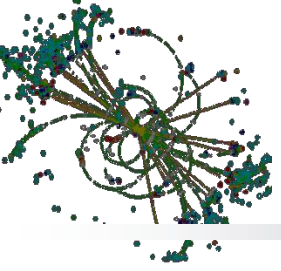
Summary of prototypes tests

○ **From both, first and second prototype tests we have learned:**

- ↪ **1. We can build pixels which can record time stamps with 300 ns period (1 BC interval) - prototype 1**

- ↪ **2.We can build readout system, allowing to read all hit pixels during interval between bunch trains (by implementing sparse readout) - prototype 1**

- ↪ **3.We can implement pulsed power with 2 ms ON and 200 ms OFF, and this will not ruin comparator performance - both prototype 1 and 2**

- ↪ **4. We can implement all NMOS electronics without unacceptable power consumption - prototype 2. We don't know yet if all NMOS electronics is a good alternative solution to deep P-well option.**

- ↪ **5. We can achieve comparators offset calibration with virtually any required precision using analog calibration circuit.**

- ↪ **6. Going down to smaller feature size is not as strait forward process as we thought. Sensor capacitance became an issue, limiting signal/noise ratio. And the main problem here seems to stem from 90 nm process design rules.**

Prototype 3 wish list

○ **Wish list, accepted by Sarnoff for the next prototype:**

  ✇ **1. Find a way to decrease sensor capacitance (they think they know how, and their calculations show decrease by factor 10).**

  ✇ **2. Take care about crosstalk : separate analog and digital power and ground, shield trace, connecting sensor to source follower input from busses, caring strobes and clocks (by changing metal layers designations)**

  ✇ **3. Implement 2-way calibration process**

  ✇ **4. Remove buffering of sensor reset pulse inside the chip. It will allow us to control the amplitude of this pulse, which is especially important with decreased sensor capacitance.**

  ✇ **5. Remove unnecessary multiplexing of time stamp (pure technical shortfall of prototype 2 design, which may limit speed and increase feed through noise).**

  ✇ **6. Improve timestamp memory robustness (right now about 1% of memory cells fail to record time stamps correctly).**
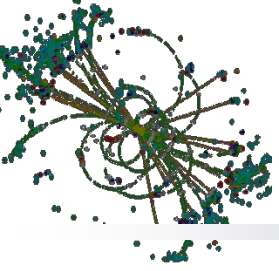
Two-way calibration implemented

○ **In prototype 2 calibration of comparator offsets begun with voltage on calibration capacitor large enough to cover all possible offsets range, and during calibration went only one way (lower and lower) until comparator reached balanced state. It had few disadvantages – as the voltage steps should be not more than 1 mV, calibration required large number of steps. And any noise pulses during calibration would move level only in one direction, so we would end up with voltage few sigma noise lower, than we want. So, we requested two-way calibration scheme. It was implemented as shown on right and simulated with SPICE model to make sure it will work.**

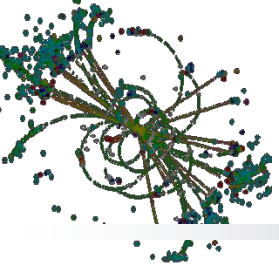Prototype 3 Pixel Mods (Power Supply Splits: up/down calibration)
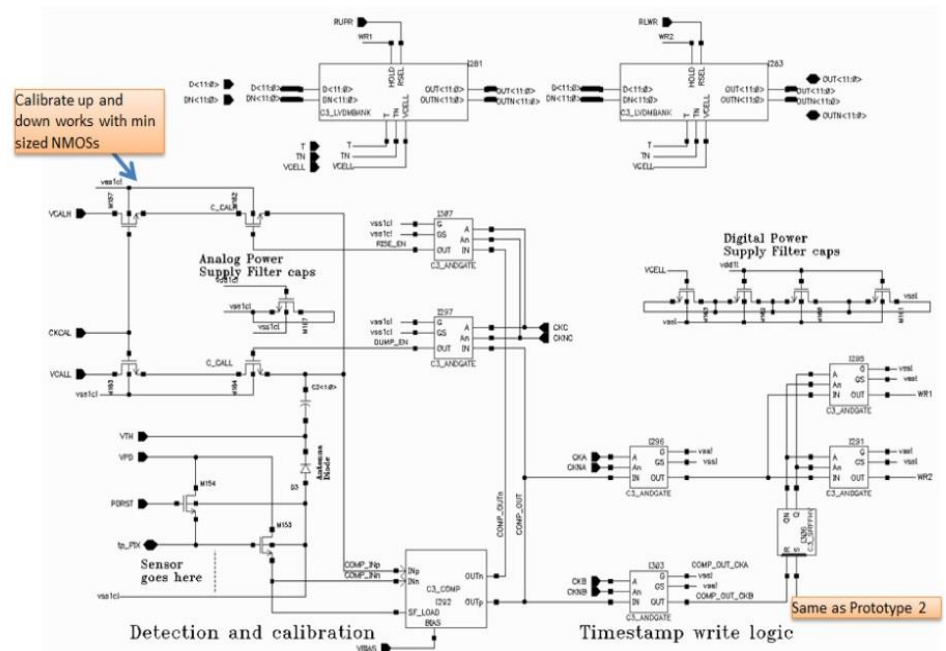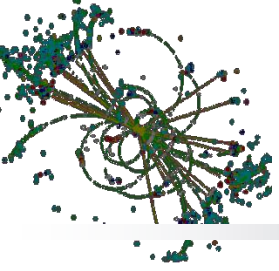
Sensor options in prototype 3

- **6 different sensor options were implemented on the same chip – 8 column allocated for each option:**
    - **1 – same as in prototype 2 – for comparison**
    - **2 – deep NWELL diode in the window in P++ layer – this violate design rules, but the waver for design rules was accepted by TSMC**
    - **3 – shallow NWELL diode also in the window – also violates design rules, but waver was accepted**
    - **4 – "Natural transistor" (NTN) allowed by design rules to be in the P++ layer window – transistor is formed directly on P+ epi layer. Large source and drain diffusion areas, gate connected to both source and drain and form sensor output**
    - **5 – also NTN but with 2 fingers, source and drain are narrow, gate also connected to both, as in option 4**
    - **6 – same as 5, however gate is not connected to source and drain, but connected to external bias voltage.**
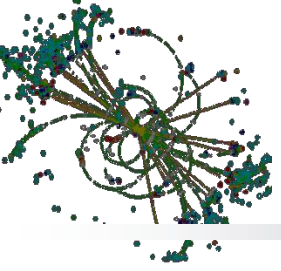
Options with NWELL diode – violating design rules
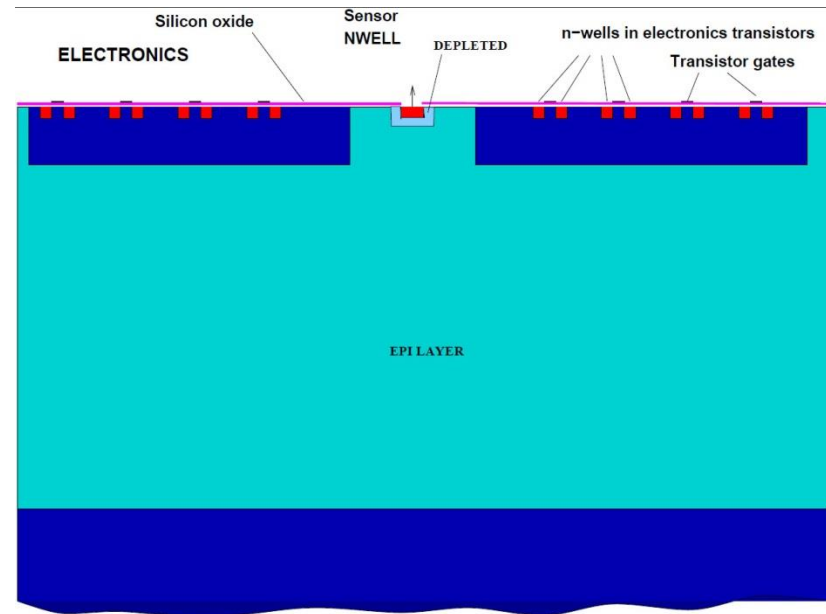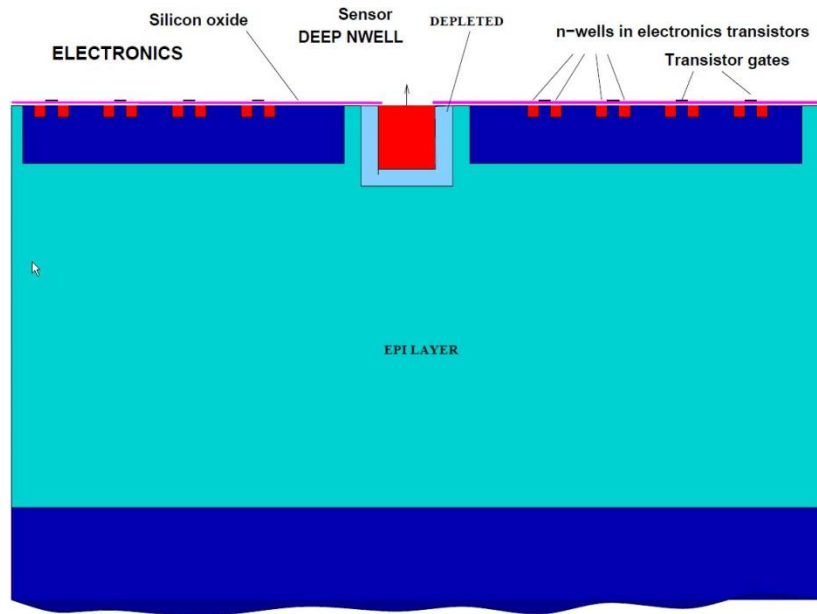
It will be interesting to compare **deep and shallow** nwells. **Deep** has **larger area**, so larger **charge collection efficiency**, however, **larger capacitance. Shallow** option has **smaller area**, but because P++ acts as **charge reflector**, the charge collection **efficiency** may be defined **not by diode size**, but by **window size**. It depends on **how deep is P++** implant, of course.

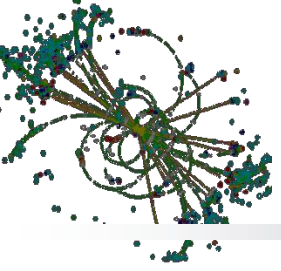# Options with "Natural transistor"
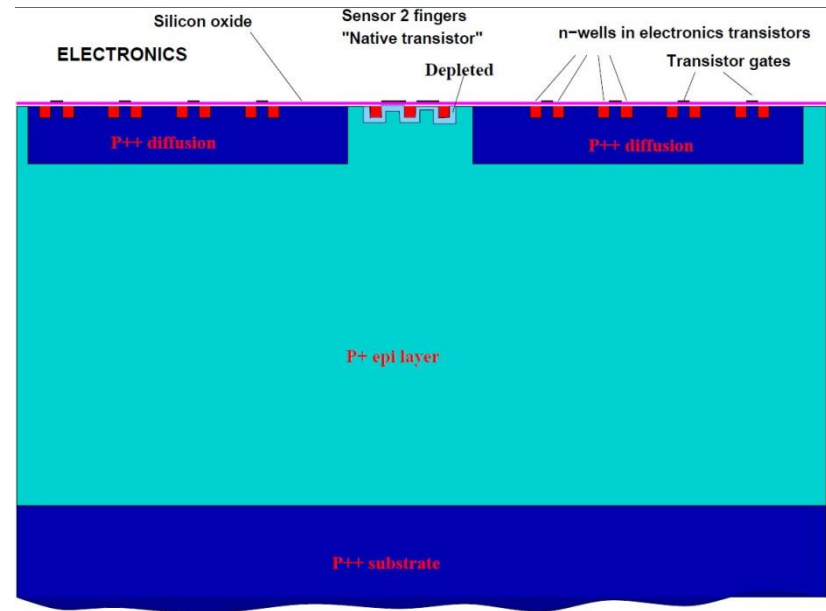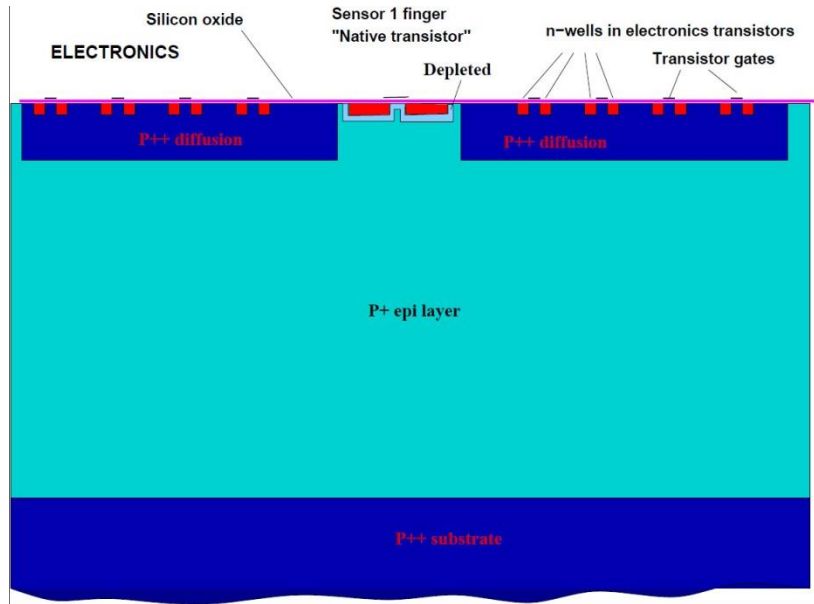
In **1 finger** option the **size of nwells** forming source and drain is **larger,** so we can hope for **better charge collection** efficiency. However, sensor **capacitance** may be **larger also.** There is 2 **2-finger** options – one with **gates connected** to **source and drain**, another – to **external bias.** It will be interesting to see how these two options behave
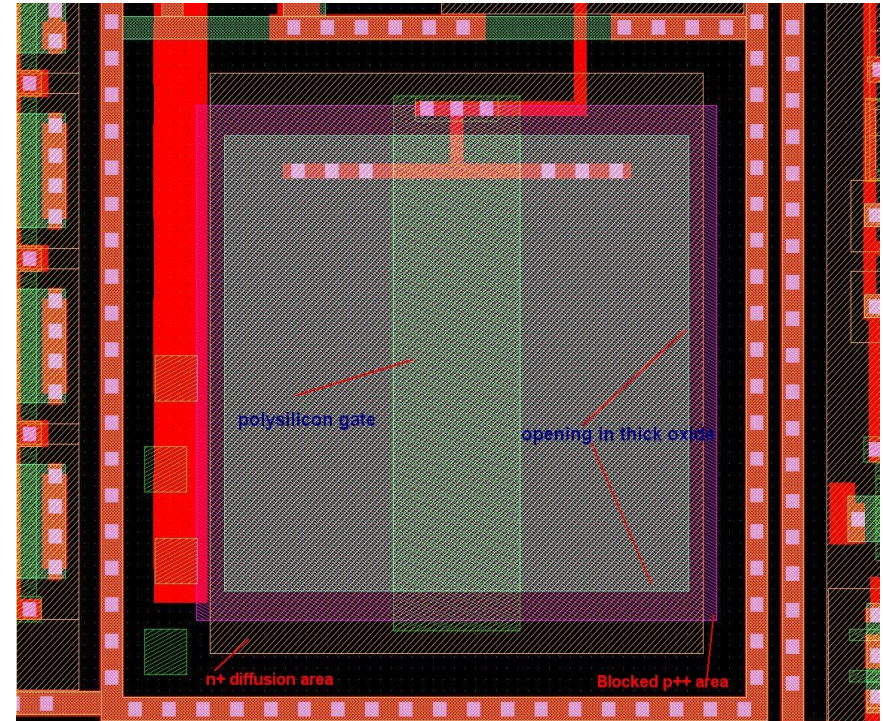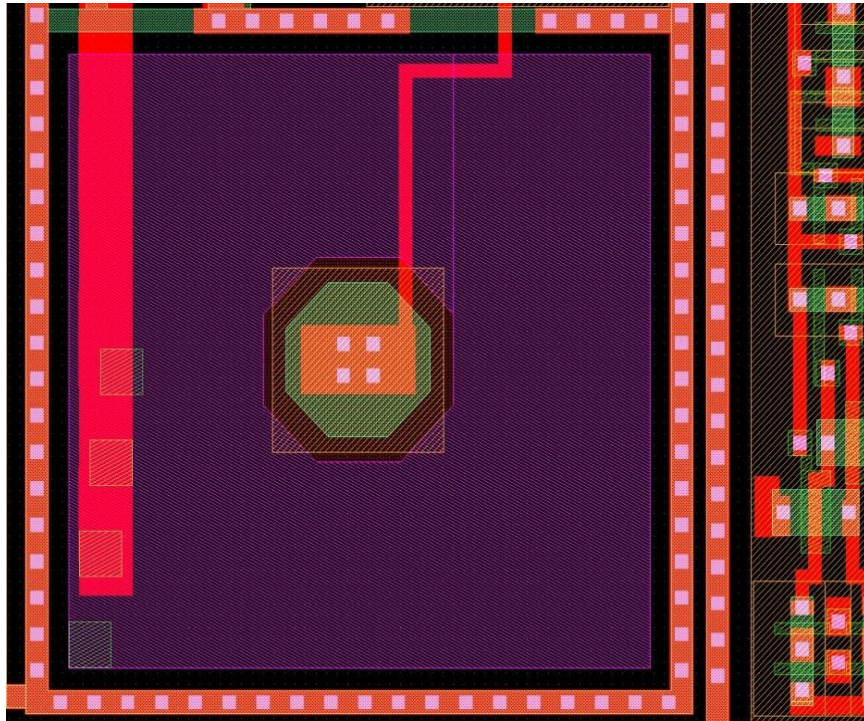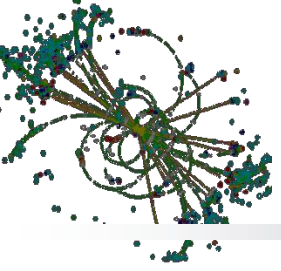
Sensor options in real layout
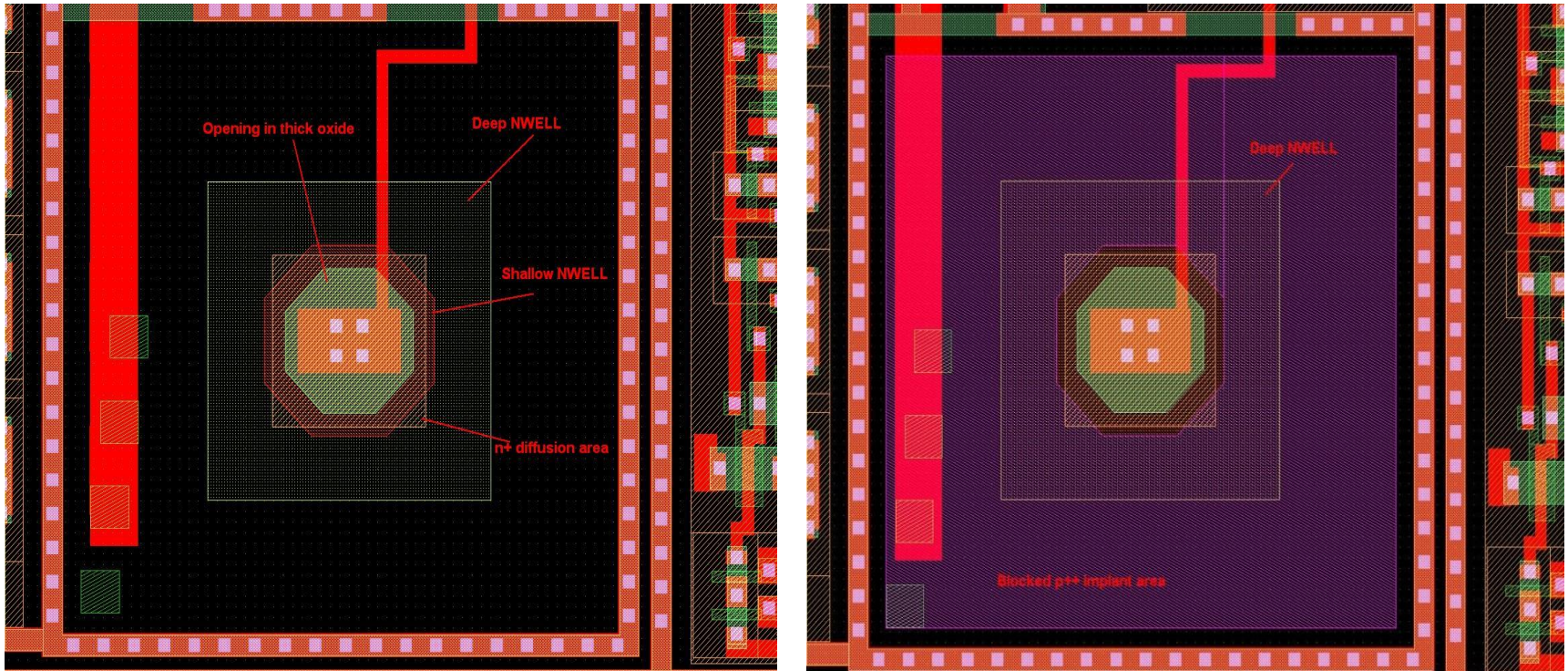
Prototype 2 sensor (left) implemented as option 1 in prototype 3 and Deep NWELL option of **prototype 3** (right). This option violate design rules, not allowing blocking p++ implant.
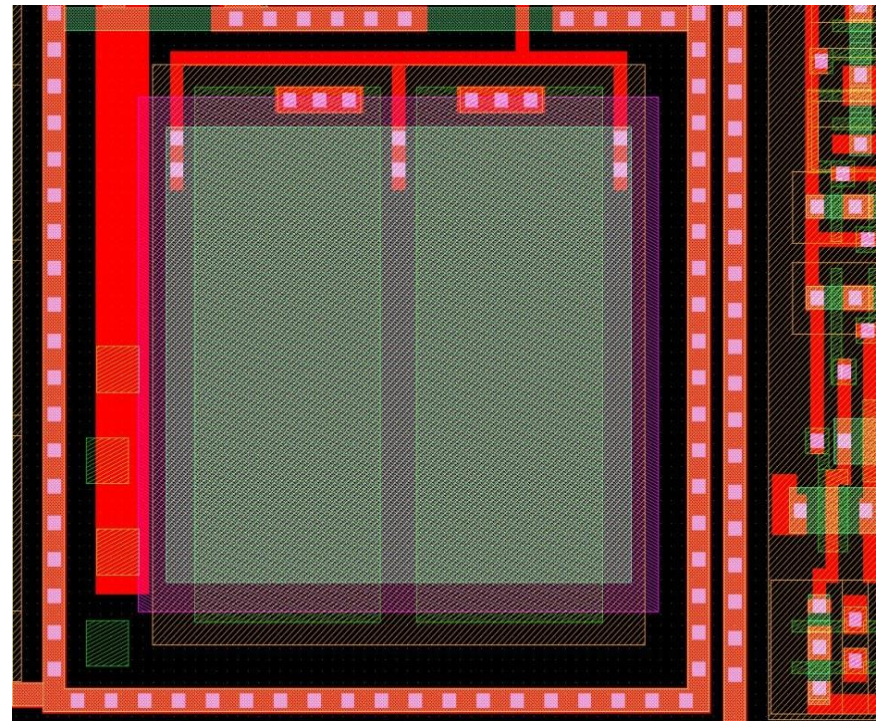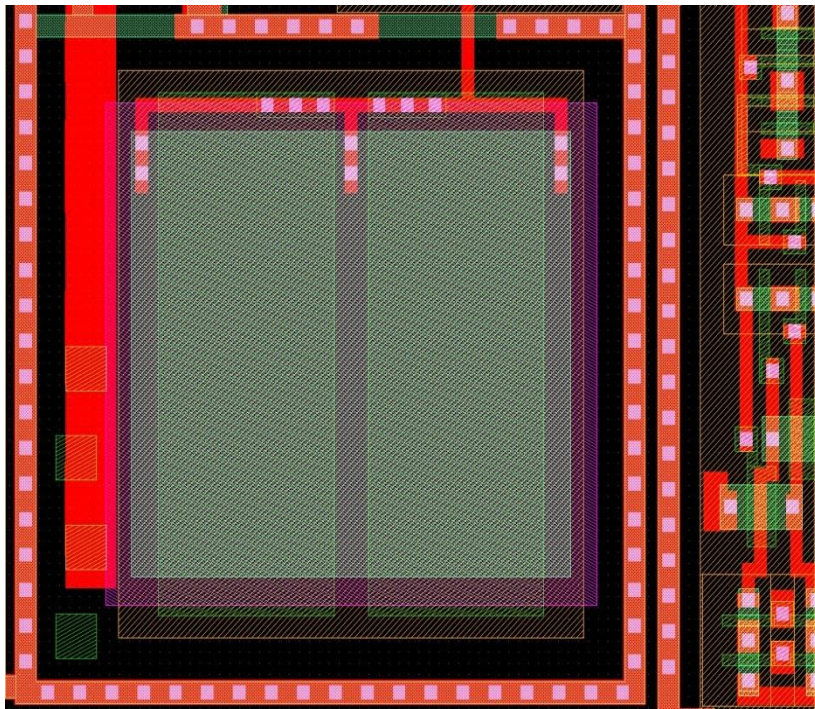
Sensor options in real layout

polysilicon gate

opening in thick oxide
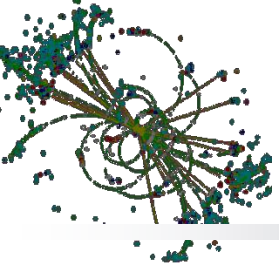
n+ diffusion area

Blocked p++ area

Shallow NWELL sensor (left) - option 3 in prototype 3 and Natural Transistor with 1 finger option 4 of **prototype 3** (right). Option with shallow NWELL violates design rules, natural transistor - not

Options 5 (left) and 6 (right) – Natural Transistor with 2 fingers – with gates connected to source and drain (left), and connected to external bias – right.
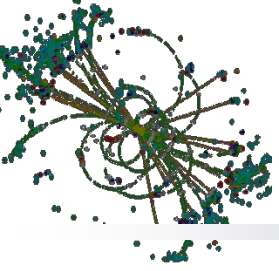
How different sensor options perform

- It was assumed, that we can achieve smaller capacitance of a sensor, compare to prototype 2. But which option can give the smallest capacitance was not obvious. And, in general, how small this capacitance can be depends not only on the sensor capacitance, but also on the parasitic capacitances of reset transistor and source follower.

- First hint on the values of the sensor capacitance could be seen on the picture at right – here are color coded values of the voltage change on the sensor due to reset pulse coupling. Because the coupling capacitance between reset transistor gate and sensor is the same for all sensor modifications, such coupling will be larger for the sensors with smaller capacitance. We see, that sensor option 3 has the larges value of coupling – means smallest capacitance
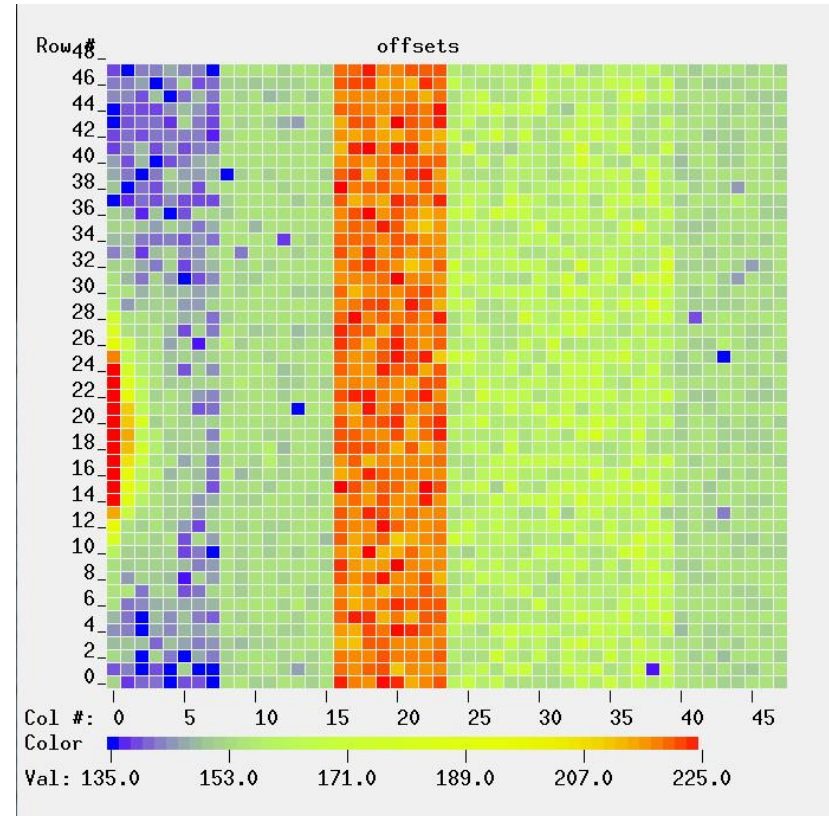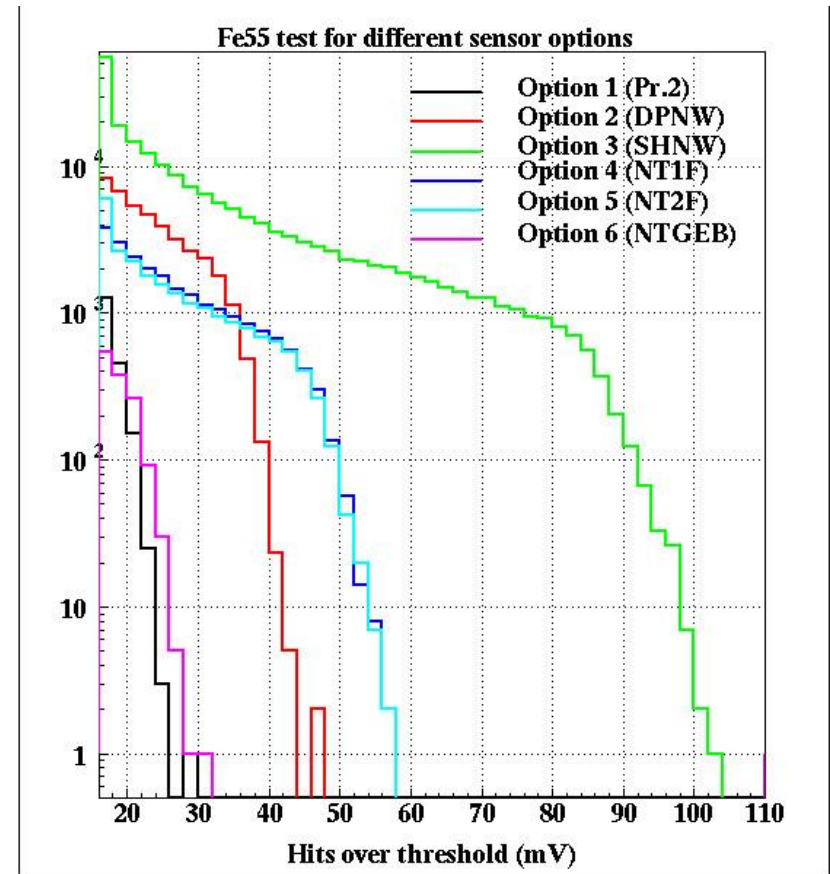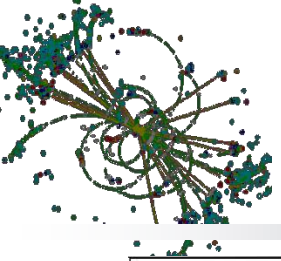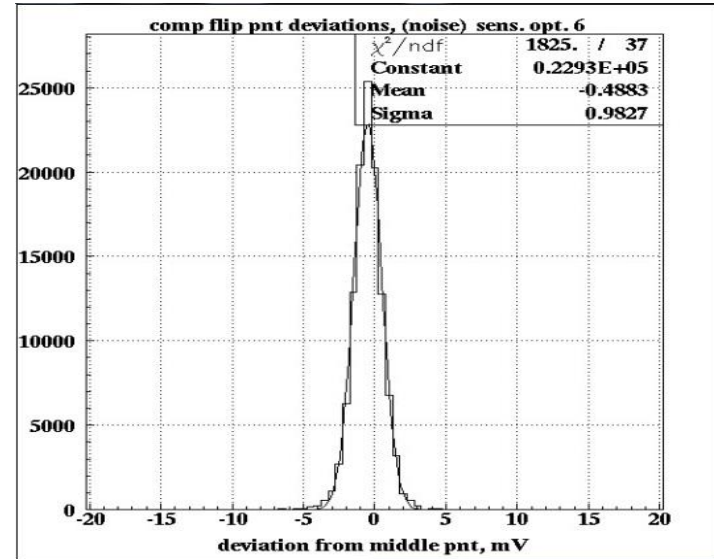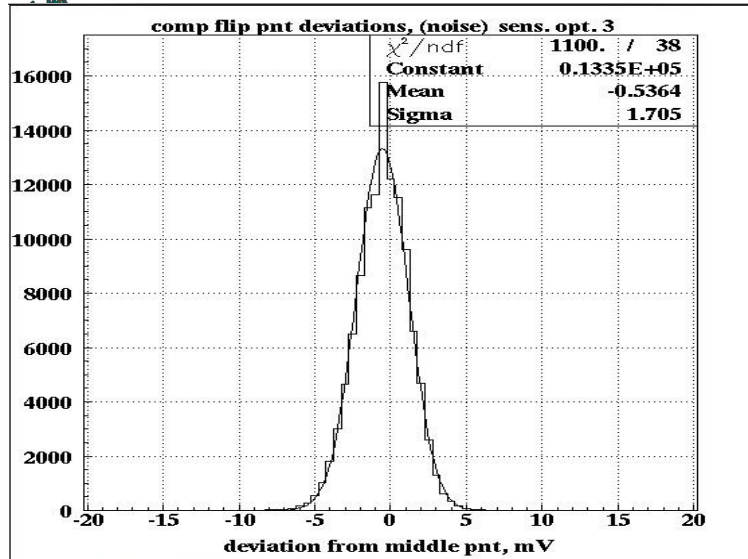
Fe55 test

- More precise method of measuring sensor capacitances consist in the observation of signal from radioactive source Fe55. It emits low energy (5.9 KeV) X-rays. Such X-rays are absorbed in the silicon, and all their energy goes into creation of electron-hole pairs. The energy to create one such pair is well known, and is 3.66 eV for Si. So, from maximum observed signal we can calculate capacitance. Taking into account, that Fe55 has about 10% of decays with energy 6.49 KeV, we can get following capacitances:

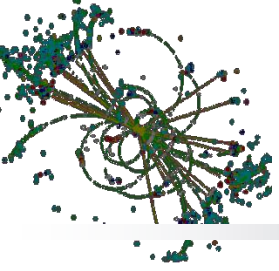- Opt. 1 – 9.04 fF, opt 2 – 6.2 fF, opt 3 – 2.73 fF, opt 4 and 5 4.9 fF and option 6 – 8.9 fF

Fe55 test for different sensor options

Option 1 (Pr.2)
Option 2 (DPNW)
Option 3 (SHNW)
Option 4 (NT1F)
Option 5 (NT2F)
Option 6 (NTGEB)

Hits over threshold (mV)

Sensor noise measurements

- **Plots above show noise measurements for sensor options with minimum capacitance (option 2, C=2.73 fF) on left, and maximum capacitance (option 6, C=8.9 fF) on right. Qualitatively they agree with expectation – larger capacitance – smaller noise, but they are larger, than expected from KTC noise formula. That means, that there are additional noise pick up, and table on the next page will give you estimated values of such pick up.**
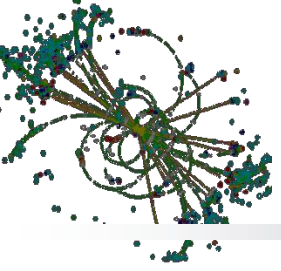
Noise observed vs expected

Table at the right shows measured noise values (mV) for different sensor options, and comparison with expected values from KTC noise formula and computed from Fe55 test capacitances. Interesting to notice. that extra noise pick up is largest for smallest capacitance, which is not a surprise, if pick up occurs through capacitive coupling to the sensor. Option 1 seems does not follow this rule – it has largest capacitance, but not smallest pick up. However, it can be understood from the fact, that these pixels are closest to the sensor edge, where most pulsed control signals are formed.

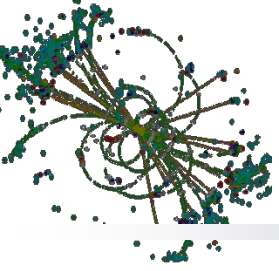| Option	sigma obs.	sigma exp.	Sqrt $(\delta^2_{ob} - \delta^2_{ex})$
1	1.12	0.67	0.9
2	1.08	0.8	0.73
3	1.7	1.21	1.2
4	1.21	0.9	0.8
5	1.23	0.9	0.84
6	0.98	0.67	0.72

Notice: for option 3 from the Fe55 test we have sensitivity 60μV/e, so noise 1.7 mV corresponds to 28 e, which is close to our original specifications of 25 e. However, see father discussion about option selection for final design.

Comparator offset compensation
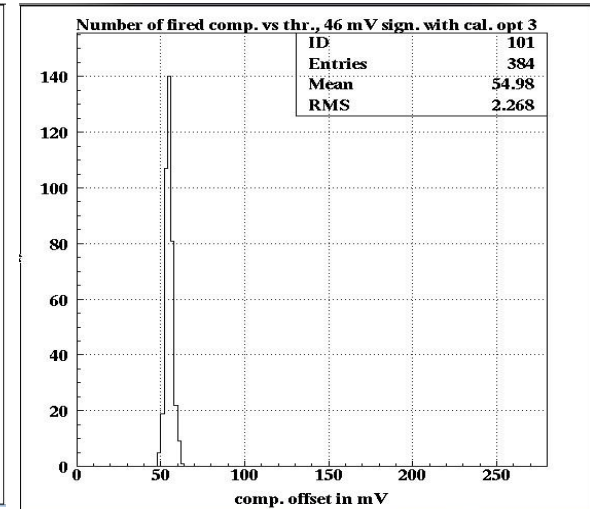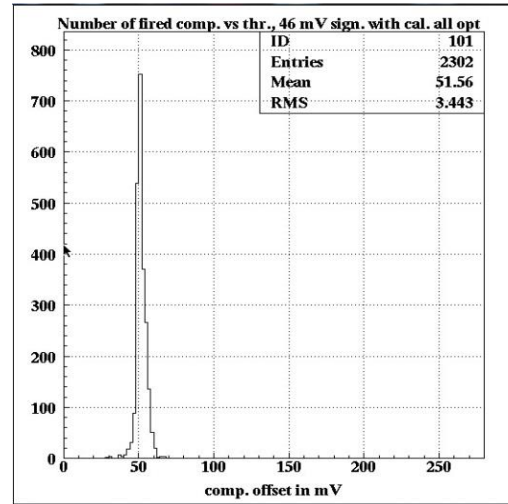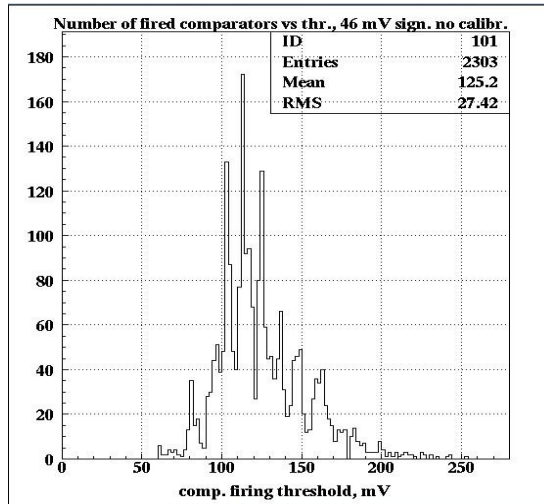
- Left picture shows distribution of comparator offsets before compensation (we call it calibration), middle – the same after compensation for all pixels, right – after compensation for pixels with sensor option 3. From the fact, that signal of 46 mV fires comparators at slightly larger threshold, and that this difference is different for different sensor options we can conclude, that such calibration is affected by additional noise pick up.

Discussion

- Looks like **option 3** – shallow diode violating design rule provides best performance – smaller capacitance, larger signal. However, we should remember, that sensor area in that case is only **2.74 μ²**, while options 4 and 5 – natural transistors – have sensor (n+ diffusion area) **19.36 μ²**. And sensor **area is important** for charge collection efficiency, because we have competing n-wells in our pixels with total area of **~13 μ²**. However, there may be another factors here. For example, if small sensor diode sits inside large hole in p++ implant, it is possible, that for most electrons, entered this hole probability to diffuse back and be collected by parasitic NWELLs is much smaller, **than to be collected by diode**, sitting in the hole. However, that depends on how **large is depleted region**, and will not they be **captured by oxide border.**

- In any case, <u>we need much more tests</u> **with minimum ionizing tracks** to find what the charge collection efficiency for different option is. And so far, native transistor option may appear as the best choice.

Summary and plans

- **Chronopixel R&D are moving forward, we have solved many problems and proved that concept is valid.**

- **Looks like the problem with large capacitance of sensors in 90 nm technology is solved!**

- **Much more work is needed to fully understand details of sensor operations. We absolutely need to measure sensor efficiency for minimum ionizing particles.**

- **Cross talk issues were addressed in prototype 3 by separating analog and digital powers and putting small decoupling capacitors into each pixel. However, we still see some effect of cross talks. It is not a show-stopper, as effect is relatively small, but we need to think about minimizing it.**

- **There is a lot of exiting work ahead!**