Detector tracking session summary

- Convenors:

J. Baudot*	T. Nelson
A. Bellerive	S. Redford
T. Matsuda	J. Strube

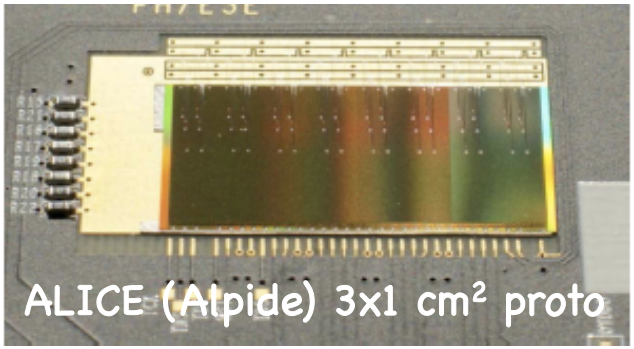
12 contributions

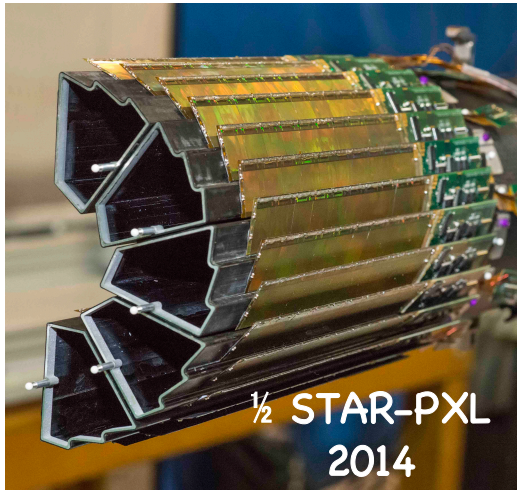
	Technology		Integration	
Vertex (pixels)	5	CMOS sensors, DEPFET, hybrid	3	Cooling, mechanical support, power pusling
Inner tracker (strips)	1	2D-microstrip	1	
External tracker (TPC)	2	GEM		

- 3 additional contributions in joint sw/tracking/calorimetry
  - Response simulation for vtx sensors
  - Tracking algorithms

Vertex: technologies

- **CMOS pixel sensors** M. Winter (IPHC)
  - Successful operation of 1st generation in STAR experiment
    - Binary output, 200 μs integration time
  - 2nd generation in preparation for ALICE
    - Integration time 5-20 μs demonstrated for 5μm resolution



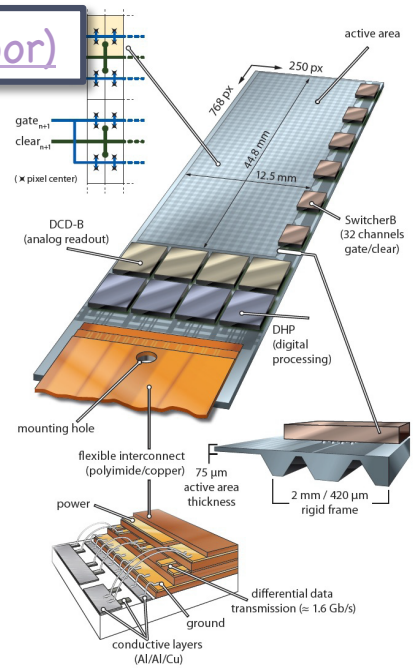


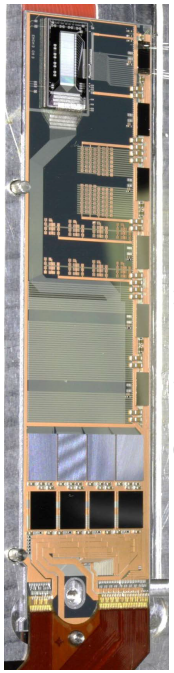
  - Potential reach
    - Spatial/timing combinations
      (3 μm/20 μs) (5 μm/5 μs) (8 μm/1 μs)
      Mixed in double-layer
    - Power driven (4 μm/60 μs)
      for outer layers
    - Adaptability wrt multiplicity

- **Chronopixel** N. Sinef (U.Oregon)
  - Ambitious design:
    - Charge & timestamp per hit within 15x15μm^2
  - 10 years effort (Sarnoff Corp.)
    - 3 prototypes : latest 2014
    - Proto 2 & 3 in techno 90 nm
  - Discri/timing functionalities solved
  - Need charge-collection assessment study & MIP detection efficiency

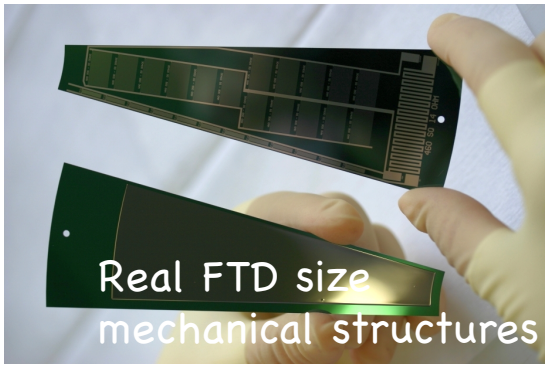
Vertex: technologies

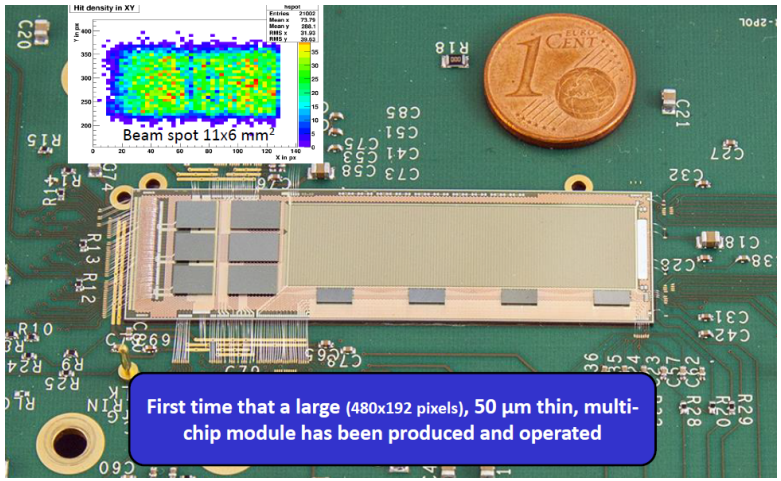
- **DEPFET** L. Andricek (MPG Halbleiterlabor)
  - Belle II PXD preparation
    - Smallest pixel size 50x55 μm^2
    - 100 ns row readout time
    - Mat. Budget 0.21 % X0
  - Toward ILC – barrel
    - Pixel size 20x20 μm^2
    - 50 ns row readout
    - Mat. Budget 0.13 % X0
  - Toward ILC – forward
    - Petal concept





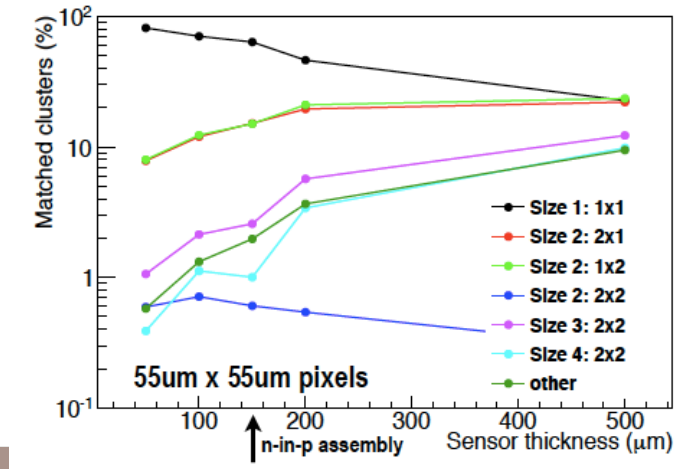
Real Belle II – size electronic layer



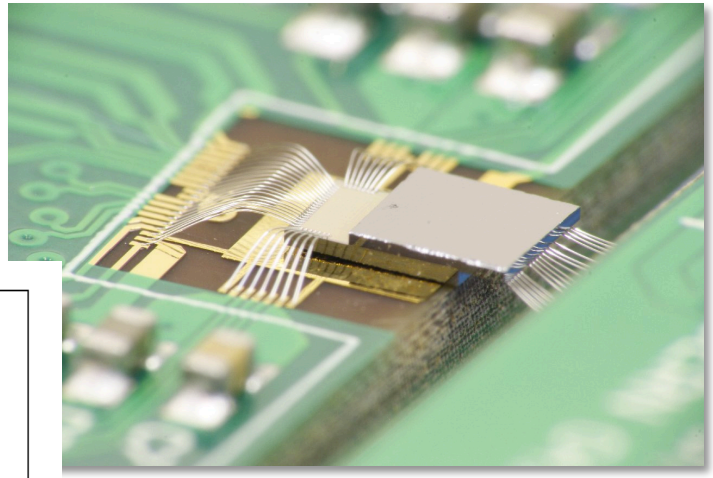


Vertex: technologies

- CLIC
  - 10 ns hit slicing needed
  - Pixel size goal 25x25 μm^2
- Hybrid pixels-1 S. Redford (CERN)
  - First readout chip: Timepix-1
    - Charge from TOT (10 bits)
    - 55 μm pitch
  - Systematic studies
    - with Timepix-1 (charge from TOT
    - Energy calibration
    - sensor thickness 50 to 300 μm
    - Edge & angle scans
    - bias voltage

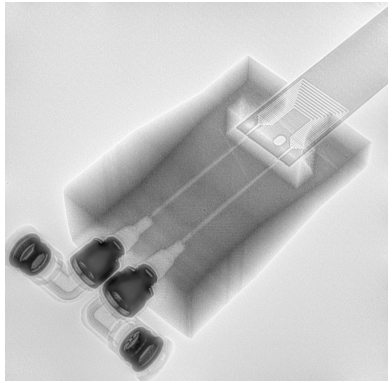


- Hybrid pixels-2 S. Arfaoui (CERN)
  - Readout chips:
    - Simultaneous charge (TOT) & time (TOA)
    - Timepix-3 (130 nm) / CLICPix (65 nm)
  - Sensor = HV-CMOS pixel (CCPDv3)
  - 25 μm investigation
  - Starting characterization

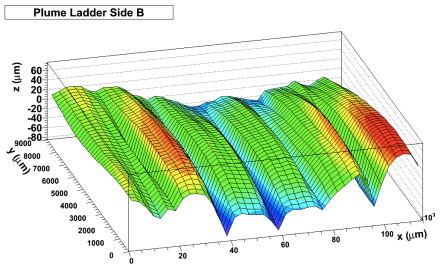


Vertex: integration

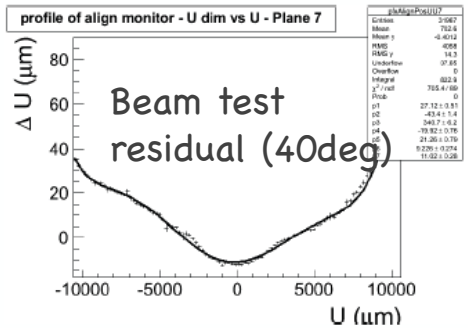
- **DEPFET ladder cooling** L. Andricek (MPG Halbleiterlabor)
  - μ-channel cooling
  - Road to minimal mat. Budget from Belle II → ILC



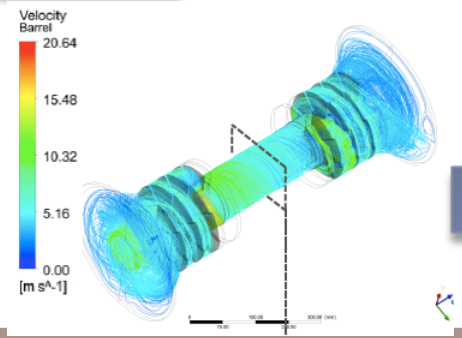
- **PLUME results** J. Goldstein (U.Bristol)
  - Double-sided CMOS pixel ladder
  - 0.6 % X0 proto tested in beam
    - Systematic studies / sp. resolution
  - 0.35 % X0 proto in fabrication

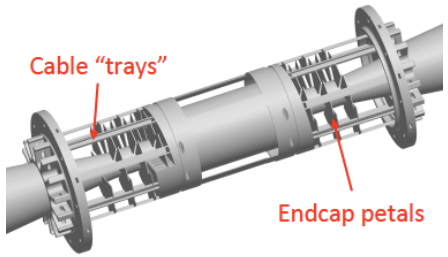


Surface survey



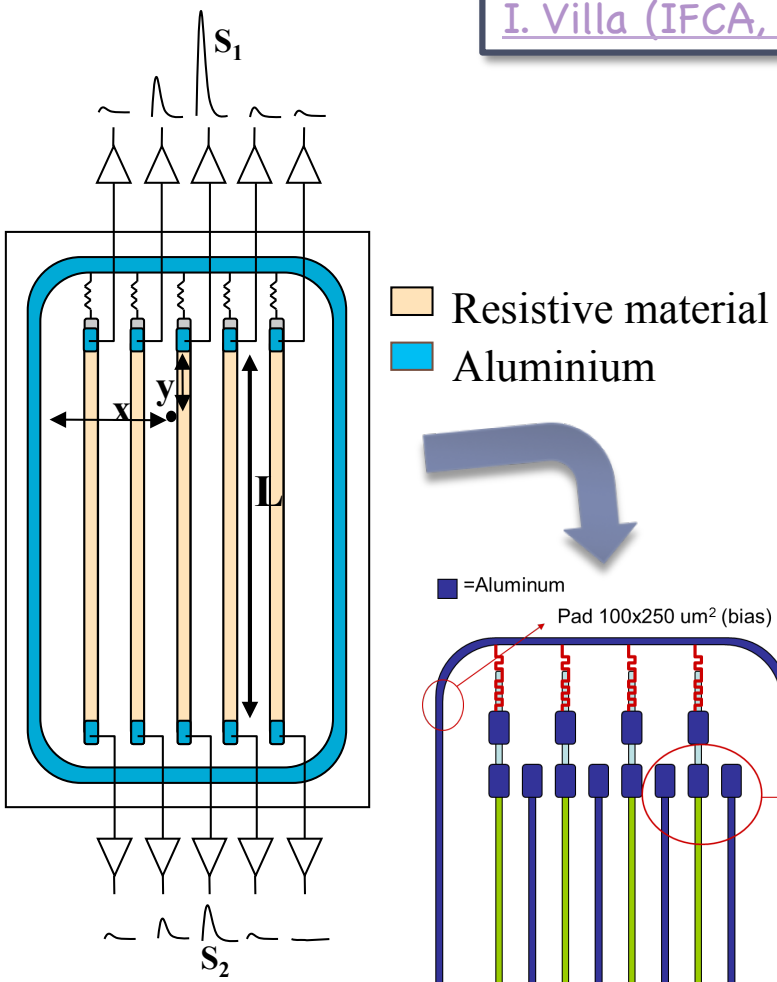
- **1:1 CLIC mock-up** F. Duarte Ramos (CERN)
  - Complete design
    - detail stave support
    - Barrel & forward
    - cables, air cooling
  - Unique opportunity to learn much

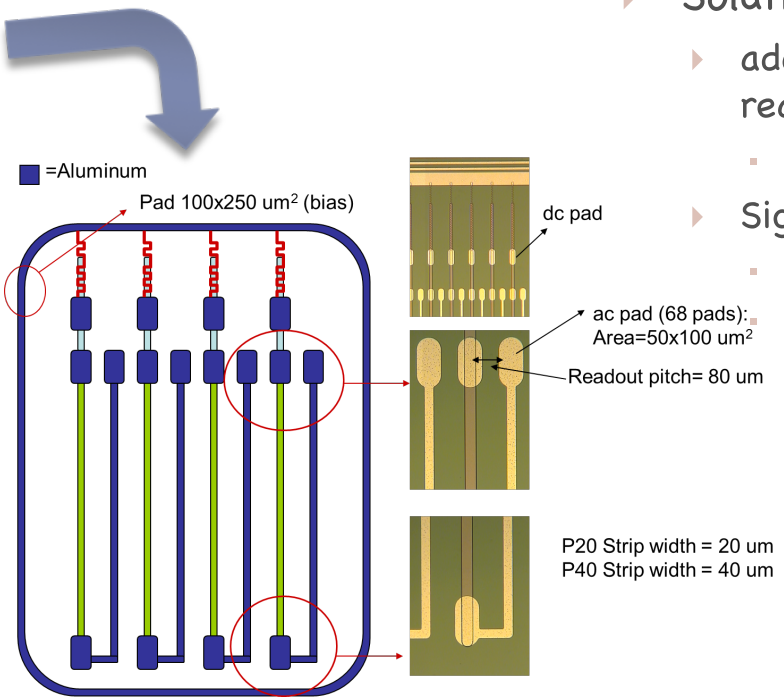




Silicon tracker: technology

I. Villa (IFCA, CNM)





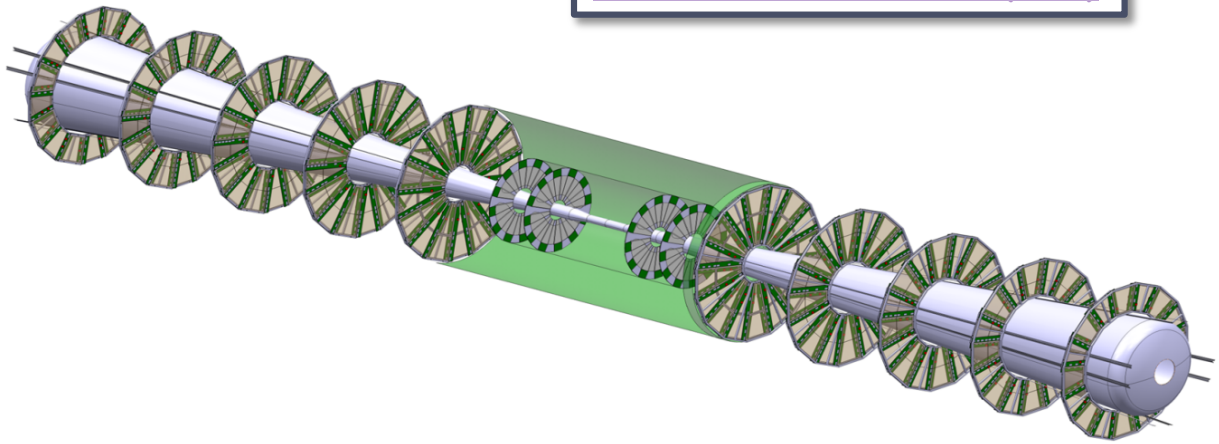
- 2D position microstrip sensor
  - Charge division principle
    - Validated in beam with prototype
      - With 25 ns readout
    - 2 issues
      - Cumbersome 2 sides readout
      - Signal loss already for 2cm long strip
  - Solutions
    - additional routing lines for same side readout
      - Solution seems viable
    - Signal amplification with low gain
      - Impact ionization with additional junction
      - Work under progress

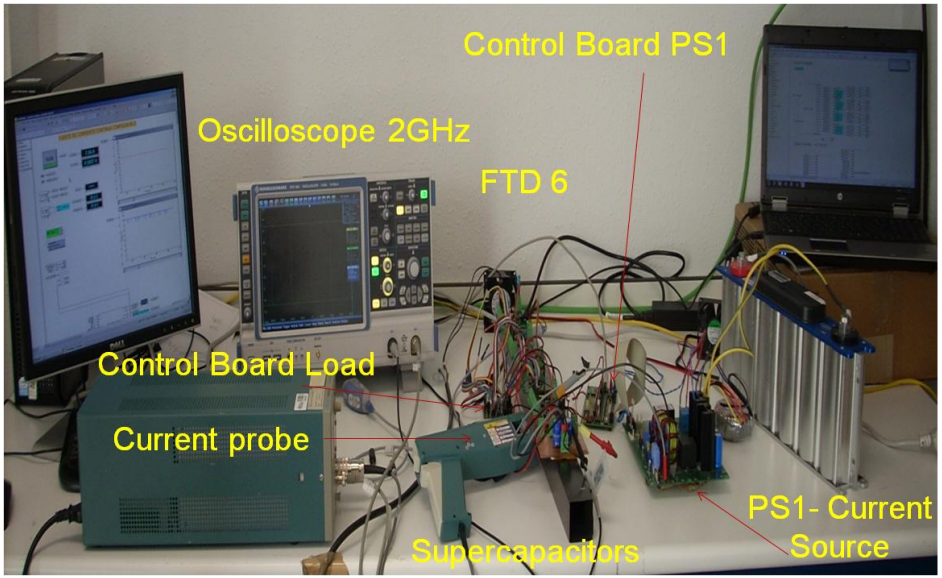
Silicon tracker : integration

- Powering the Forward Tracker Detector @ ILD

F. Arteche Gonzales (ITA)

  - Duty cycle expected: 2.5 %
  - Total consumption:
    - During train = 458 A (860 W
    - Between train = 92 A (171 W
  - System components
    - Supercapacitors
    - Low voltage regulators
    - Current source



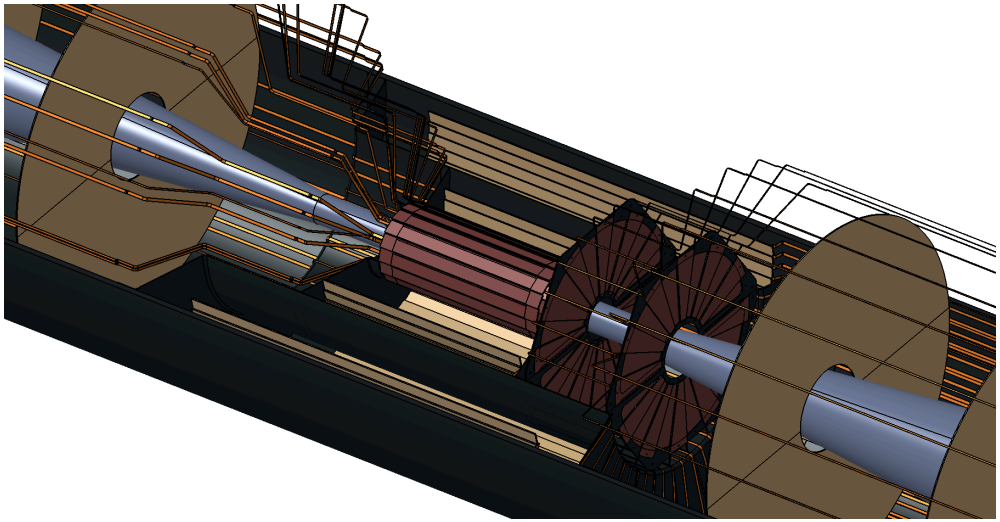


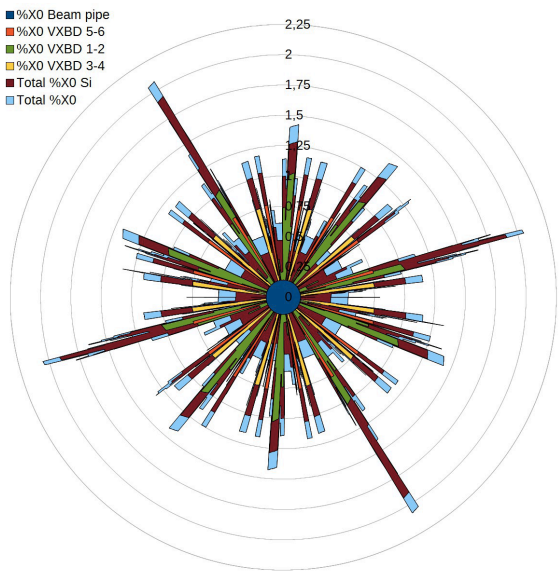
- Full setup experimental study
  - Radiation tolerance validated
  - Pulsing behaviour validated
  - Behaviour scrutinized under many scenari
  - Understanding through detailed electrical simulation

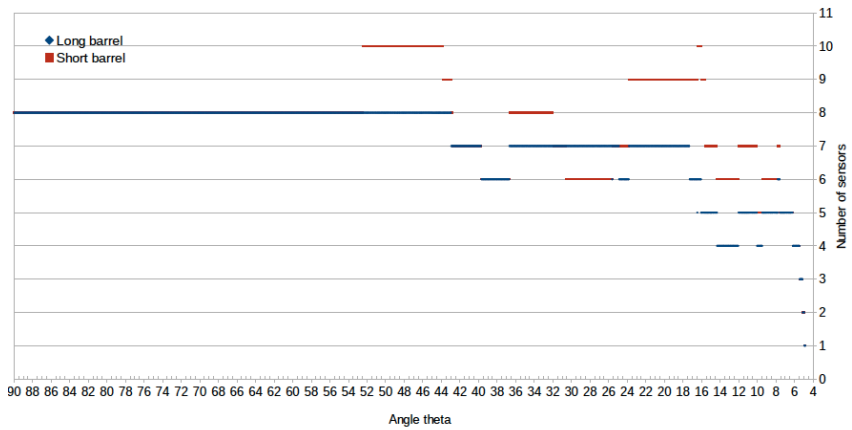
Silicon tracker: Integration

- **Full ILD model**
  - Based on DEPFET sensor
  - Design details
    - Support
    - Cables with pulsed power delivery
    - Cooling
- **Detailed analysis of mat. Budget impact**

M.-A.Vilarejo Bermudez (IFIC)

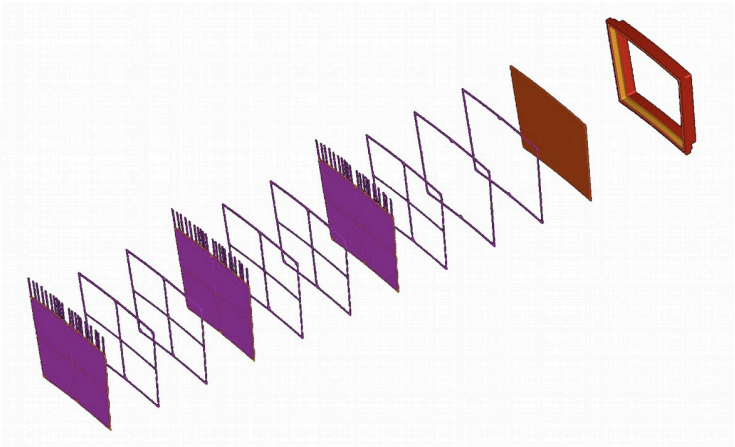


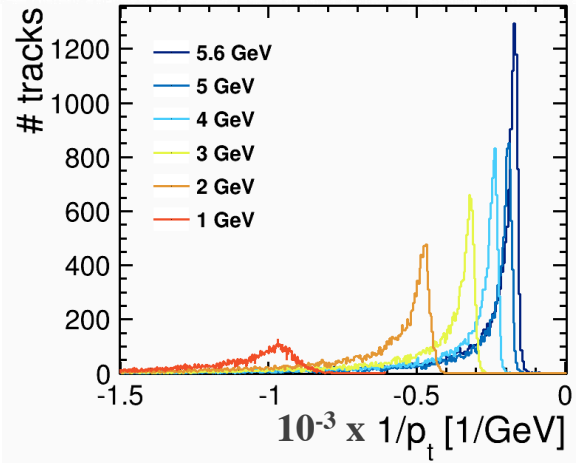




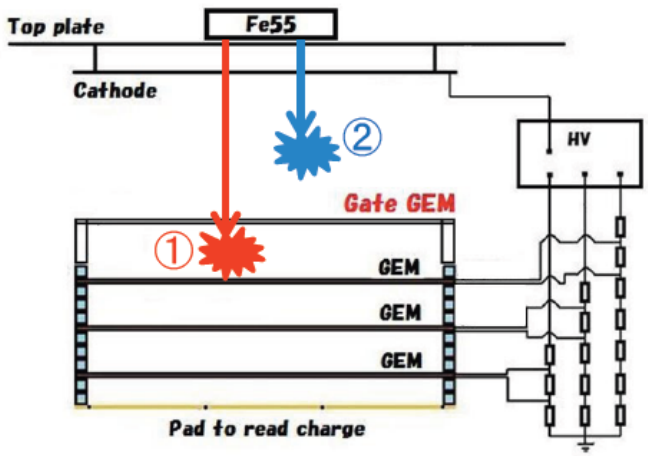
TPC readout

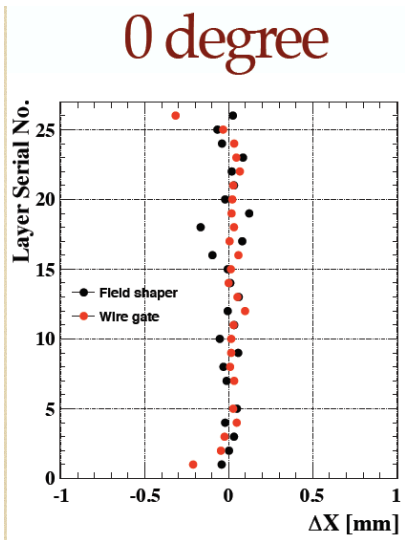
- Two contributions on GEM readout
- Prototypes with triple GEM F. Müller (DESY)
  - Detailed tested in beam
  - Distortions $\mathcal{O}$(0.5 mm) characterized at module edges





- Prototype of ion gate J. Tian (KEK)
  - First distortion correction observed
    - Reproduced by simulation
  - Stability study started





Highlights (not summary)

- **Vertex technologies : very active**
  - Adaptation potential
  - Might propose solution for silicon tracker
  - Convergence with LHC

- **Silicon tracker**
  - New real 2D microstrip solution coming

- **Integration**
  - More and more detailed / complete
  - Real-size models fabricated: feasibility / performances will be assessed soon

- **TPC**
  - GEM solution tackling the distortion difficulty
  - Micromegas contribution cancelled
    (for medical reason, best wishes to Alain Bellerive)