Electronics for FCAL Detectors

On behalf of the FCAL collaboration

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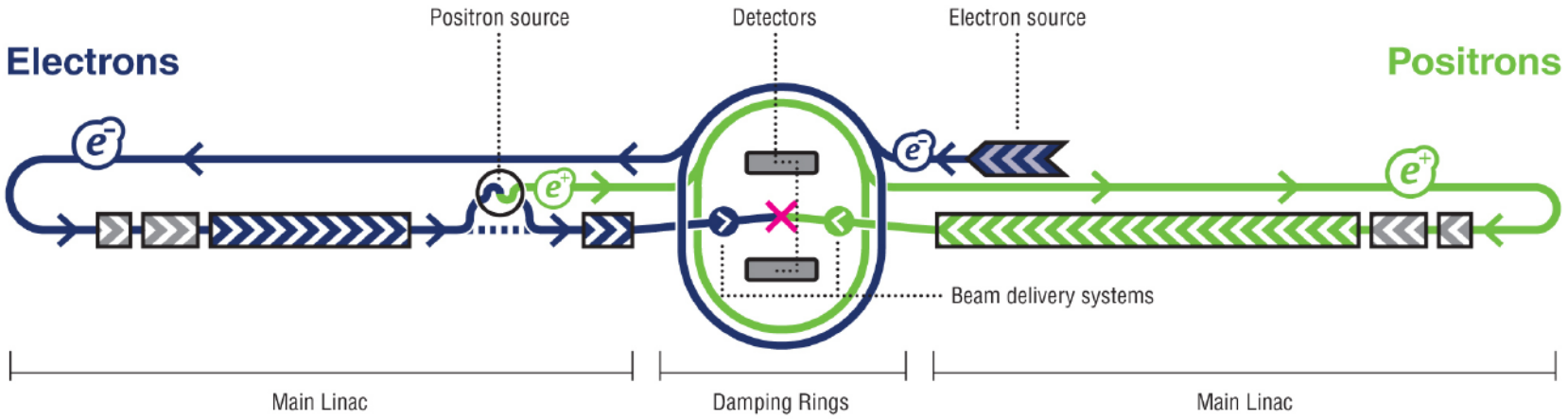
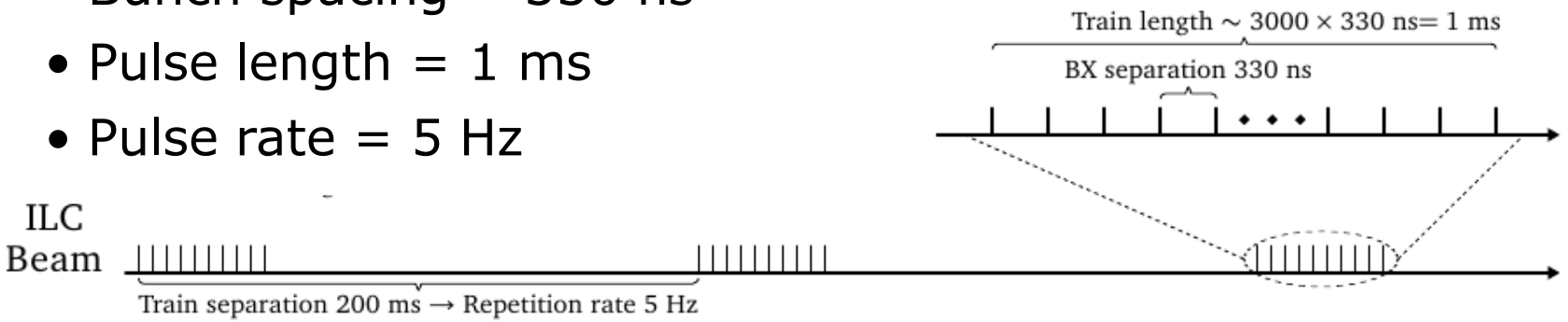
LCWS 2014

October 6-10, Belgrade, Serbia

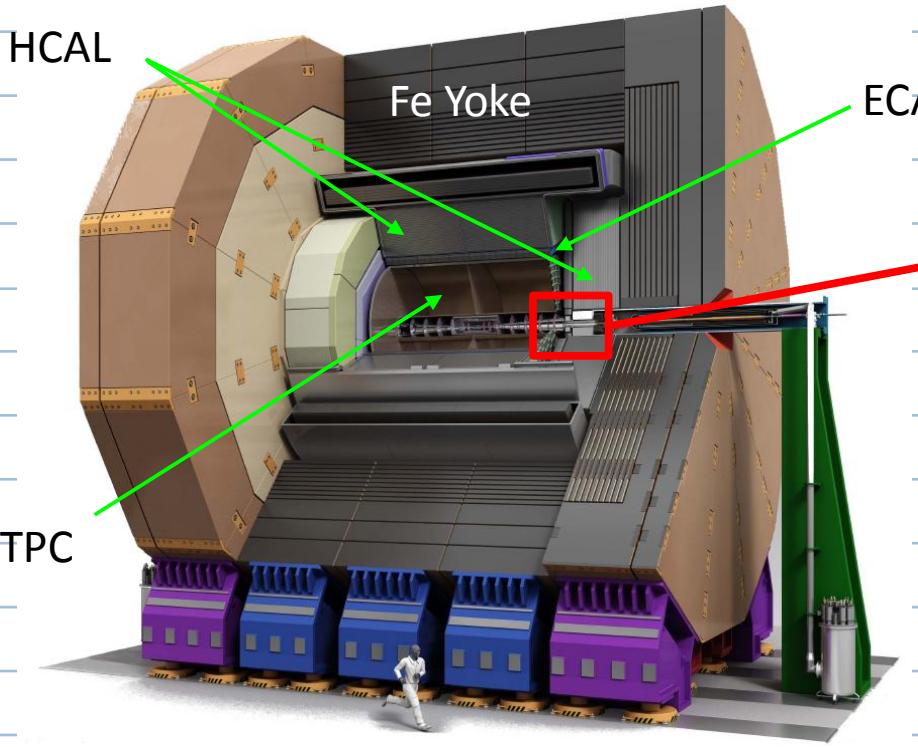
The ILC: Layout and beam structure

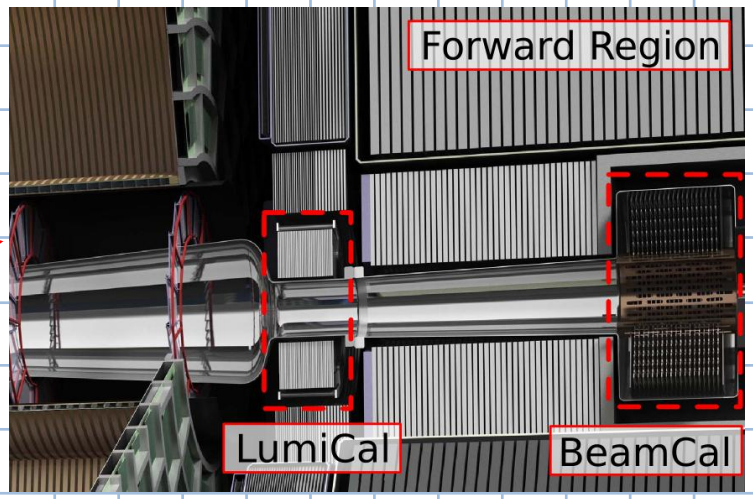


- Center-of-mass energy = 500 GeV
- Peak luminosity = 2 x 10^{34} $cm^{-2}s^{-1}$, particles per bunch = 2 x 10^{10}
- Bunch spacing = 330 ns
- Pulse length = 1 ms
- Pulse rate = 5 Hz



ILC detector



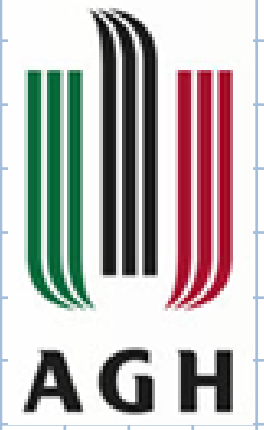


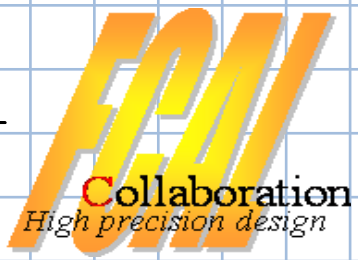
- Beam monitoring:
  - LumiCal – luminosity calorimeter
  - BeamCal – beam monitor

- Particle detectors:
  - Time Projection Chamber (TPC) – tracking
  - Electromagnetic/Hadronic Calorimetes (E/HCAL) – calorimetry
  - Fe Yoke – muon system

Talk Outline

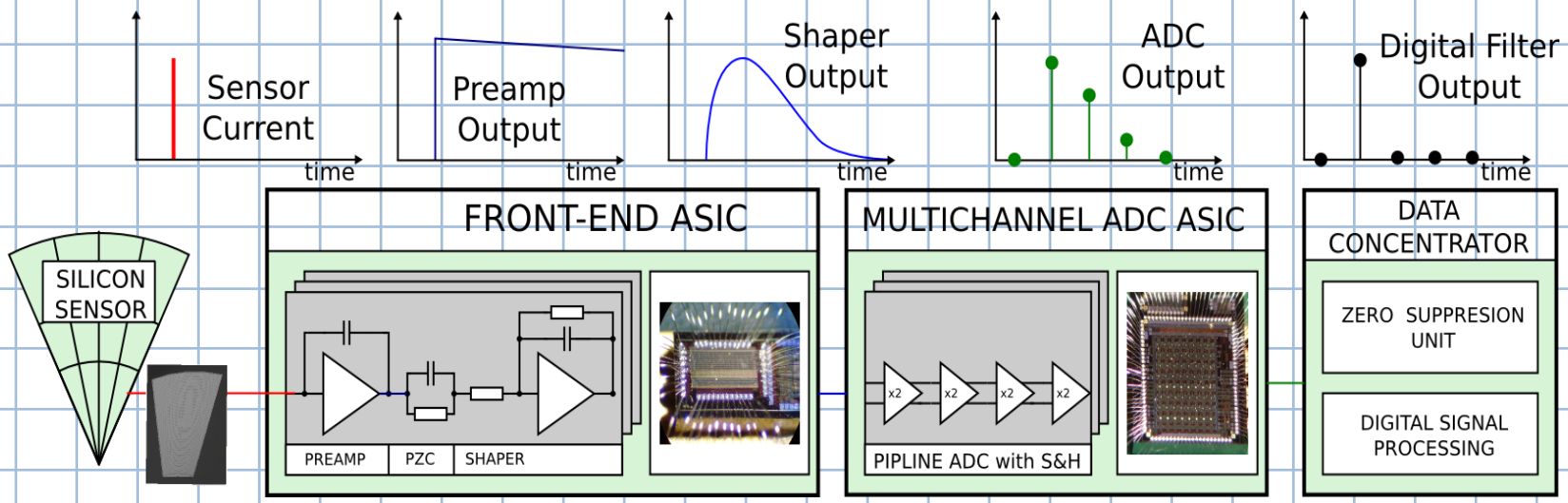
- Electronics for LumiCal
- Electronics for BeamCal





ELECTRONICS FOR LUMICAL

LumiCal Readout Chain



- **Existing LumiCal detector readout comprises:**
- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

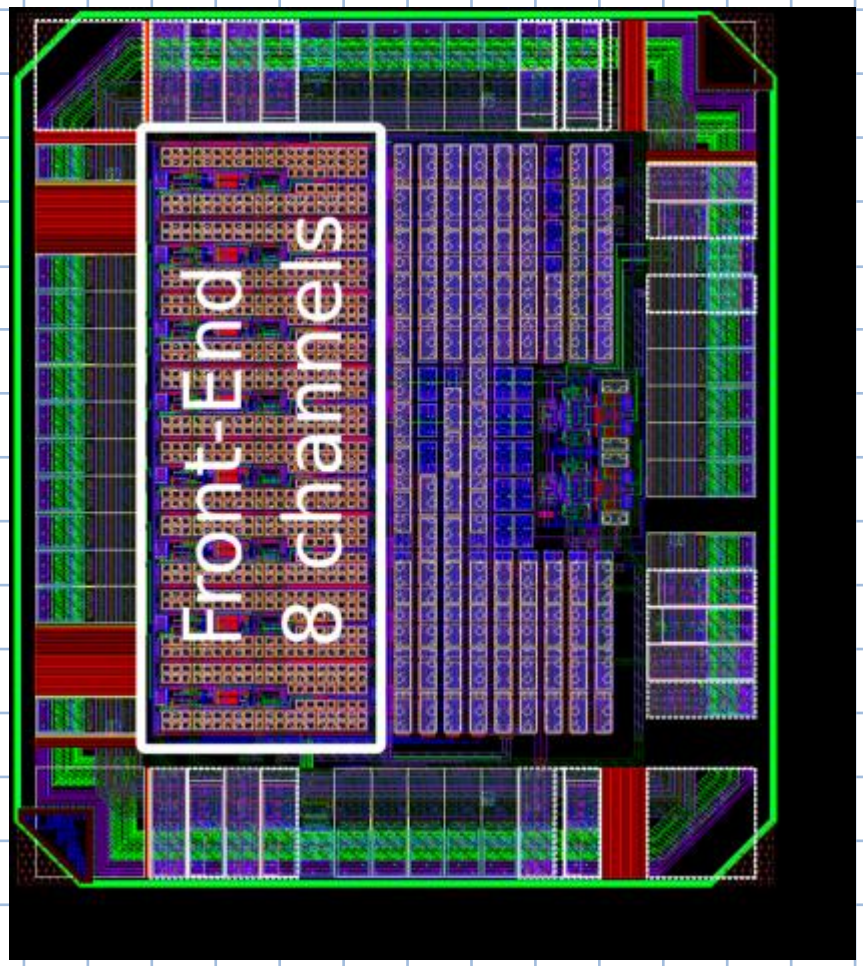
New developments for LumiCal detector readout:

- Prototype front-end ASIC in CMOS 130 nm under development... (presented at TWEPP2014)
- Prototype SAR ADC ASIC in CMOS 130 nm - fabricated and working well, already presented at TWEPP2013

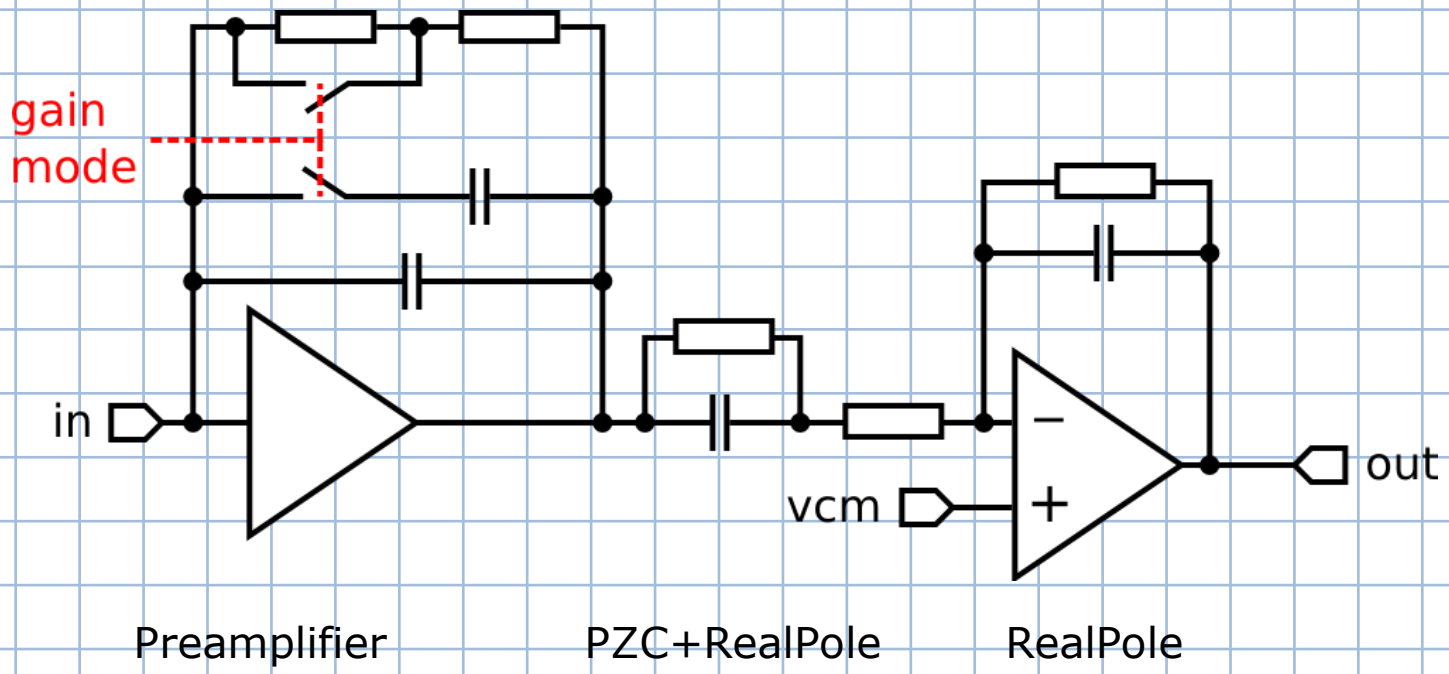
New 8-channel front-end in CMOS 130 nm

CMOS 130 nm technology

- 8 channels
- Detector capacitance Cdet ≈ 5 ÷ 50pF
- CR-RC shaping with peaking time Tpeak ≈ 50 ns
- Variable gain:
- calibration mode - MIP sensitivity
- physics mode - input charge up to ~6 pC
- Power pulsing
- Peak power consumption ~1.5 mW/channel
- Pitch ~140 um
- Noise: ENC ~ 1000e– @10pF
- Crosstalk < 1%



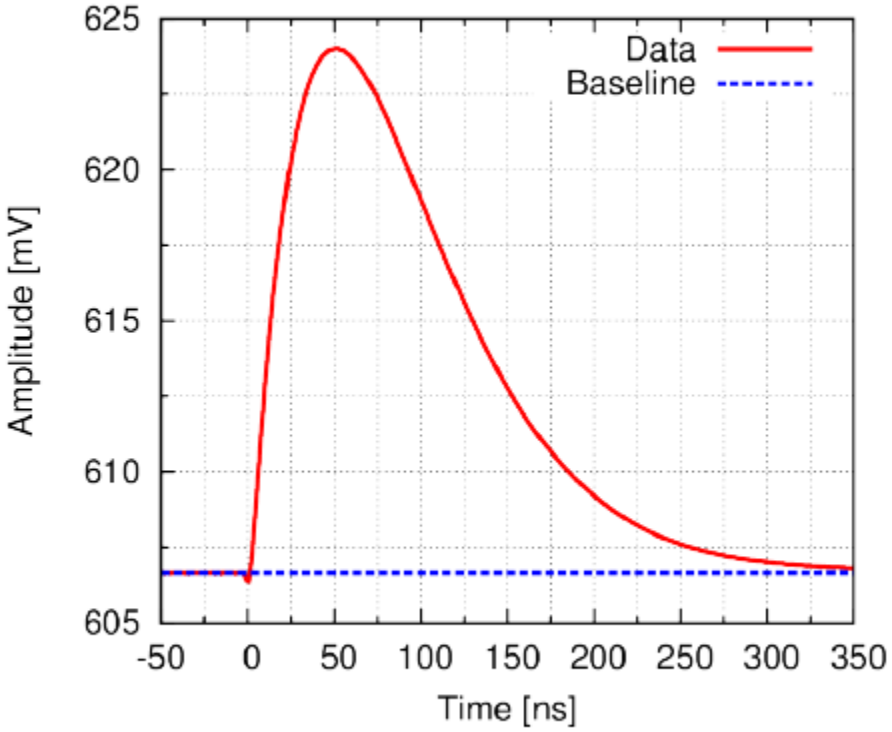
Analog front-end Architecture



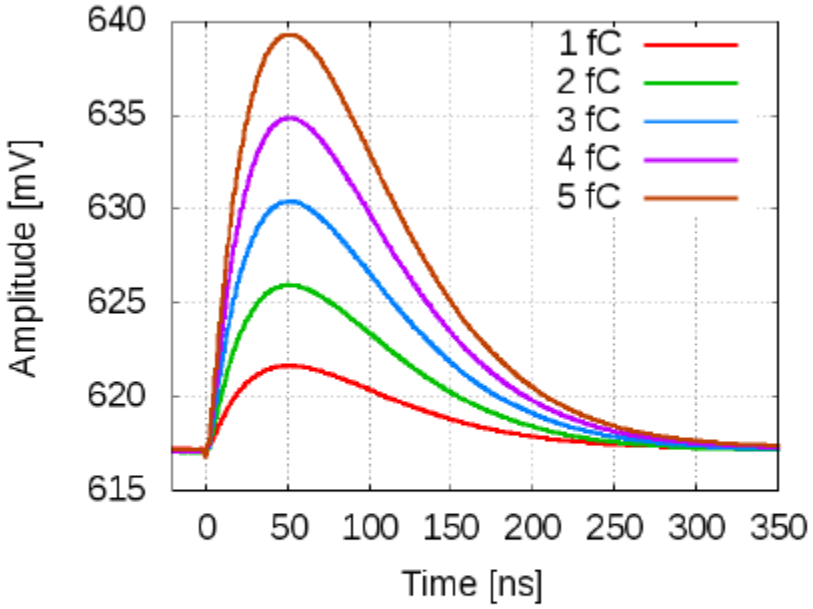
- Two gain modes (calibration and physics) applied by switching R,C components in preamplifier feedback circuit
- Simple CR-RC pulse shaping chosen to simplify the deconvolution procedure in further Digital Signal Processing (DSP)

Analog Front-End measurements
Pulse response in high gain mode

Example pulse response
C_{det}=10 pF, Q_{in}=4fC



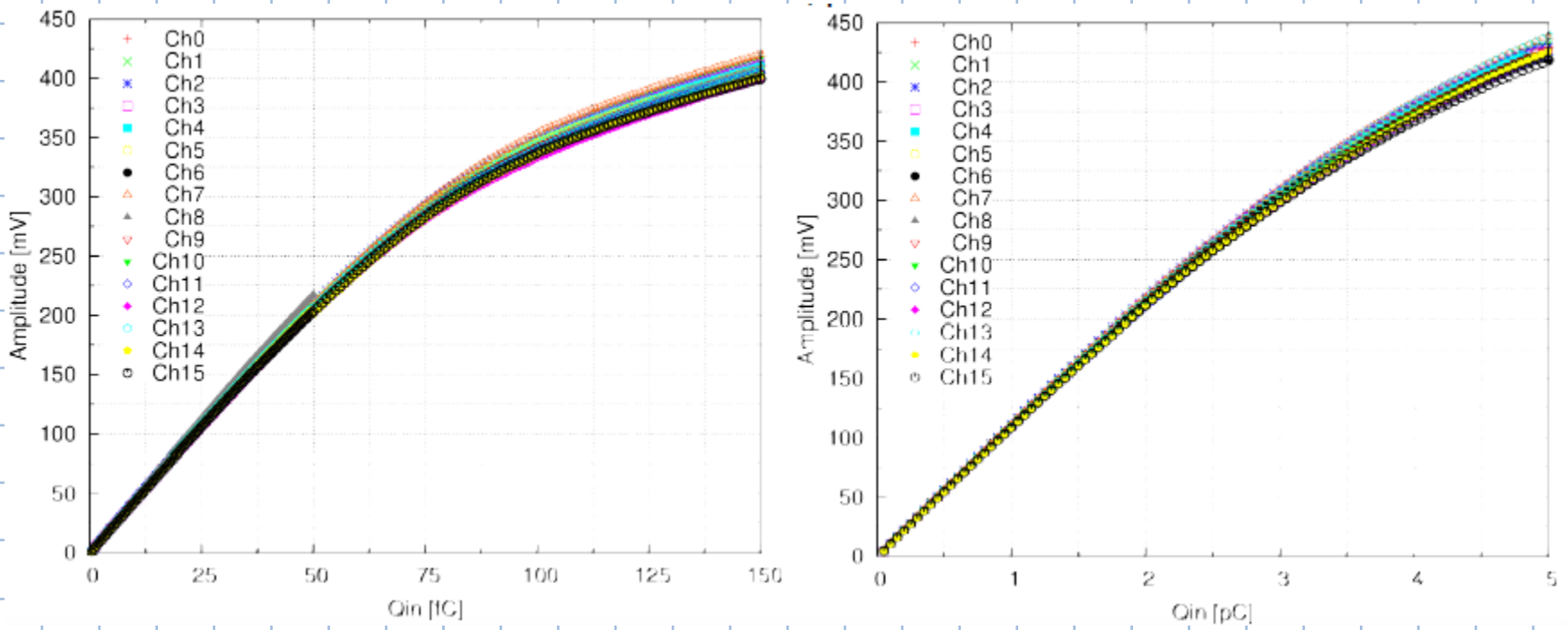
Pulses for different Q_{in}



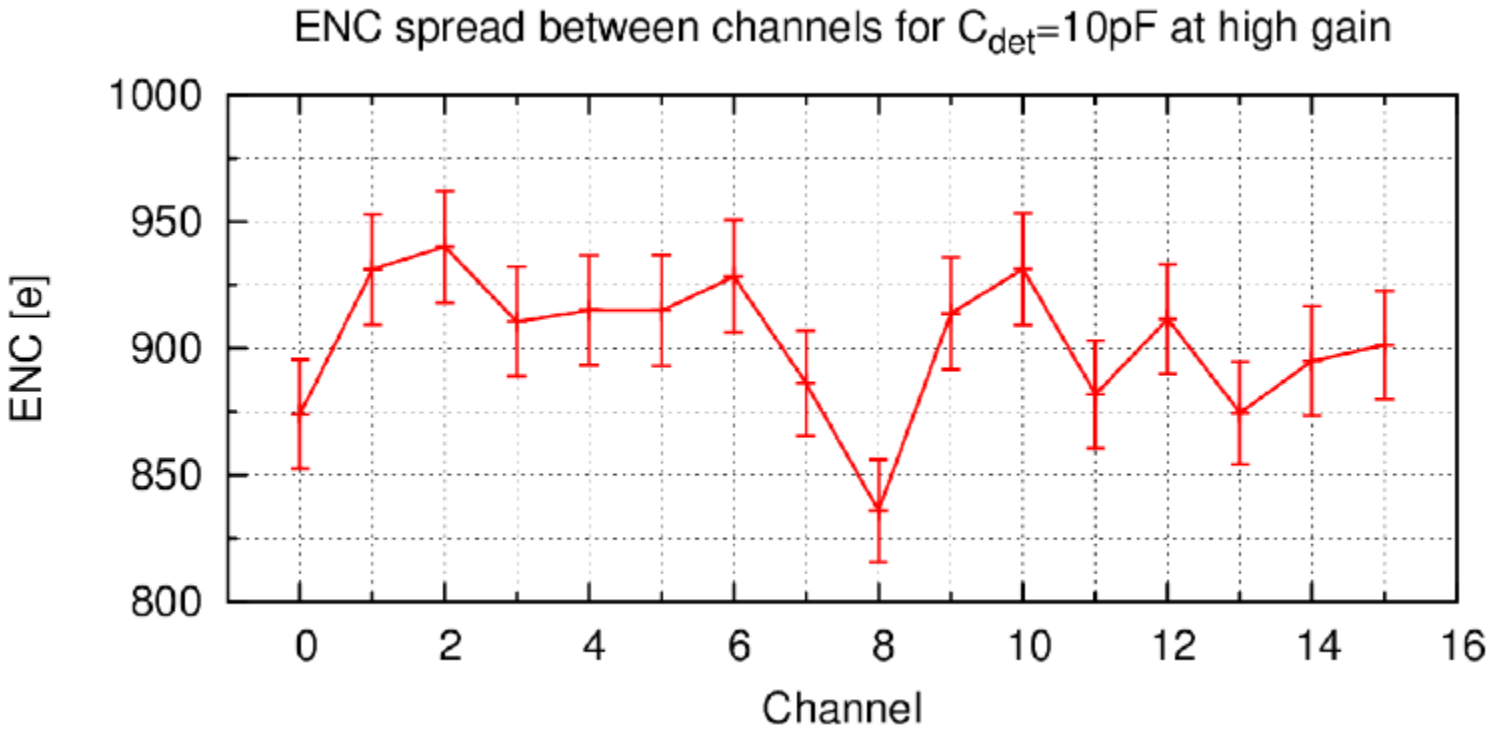
Measured shapes agree with simulations

Analog Front-End measurements: Linearity

- Measurements reasults – with agreement with simulations
  - High gain – 4.2 mV/fC (4.6 mV/fC from simulations) –
    - varies between 4.03 to 4.37 mV/fC
  - Low gain – 105 mV/pC (113 mV/pC from simulations)
    - varies between 101.7 to 106.4 mV/pC



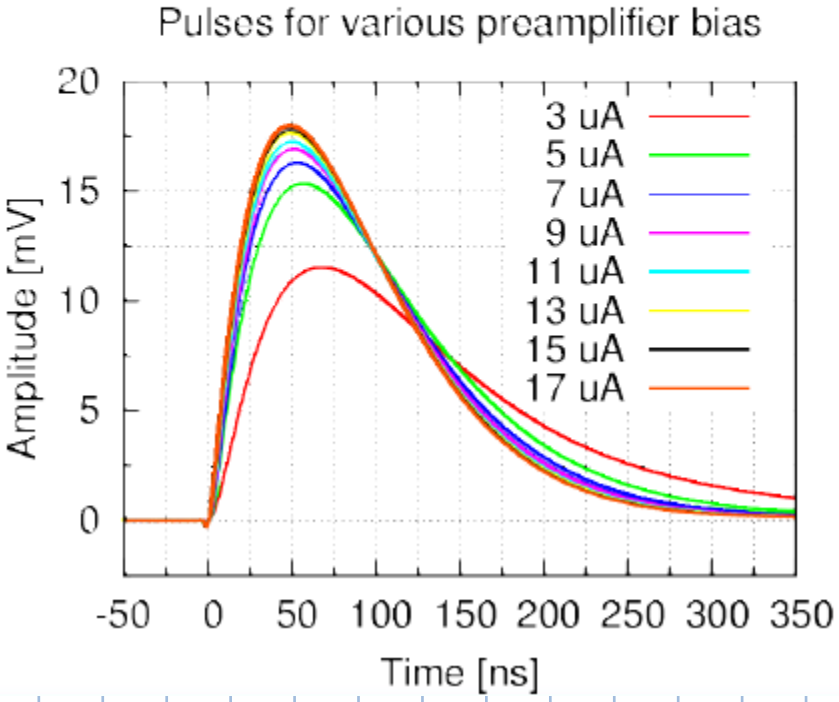
Analog Front-End measurements: Noise performance

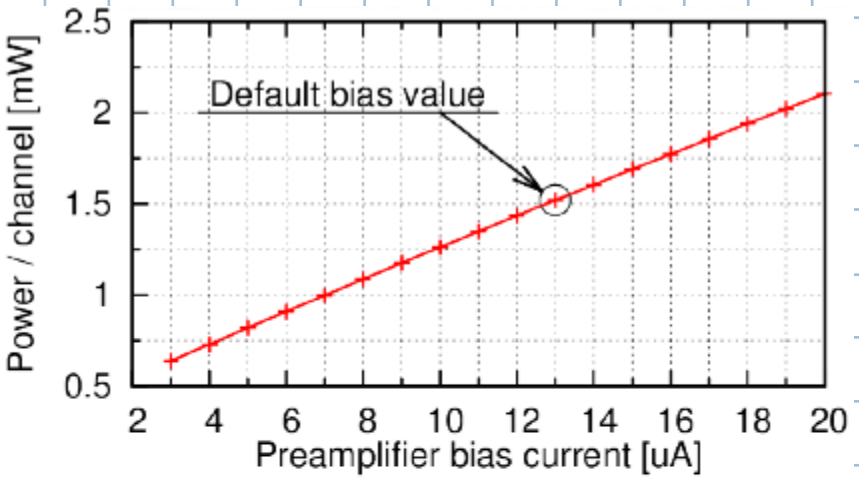


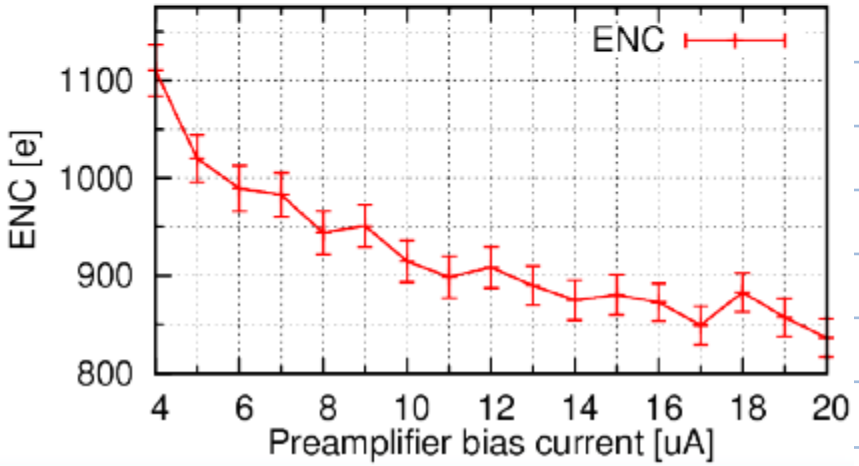
- Noise is uniform between the channels (two ASICs tested – channels 0-7 from first ASIC and 8-15 from the second)
- **ENC** (Equivalent Noise Charge) is **below 950** electrons giving **SNR** (Signal to Noise Ratio) in high gain mode **above 25** for **1 MIP** input charge

Analog Front-End measurements: Power consumption vs performance, Preamplifier bias current in high gain

- Power consumption at typical biasing 1.5 mW / channel
- Power consumption may be decreased without significant decrease of performance







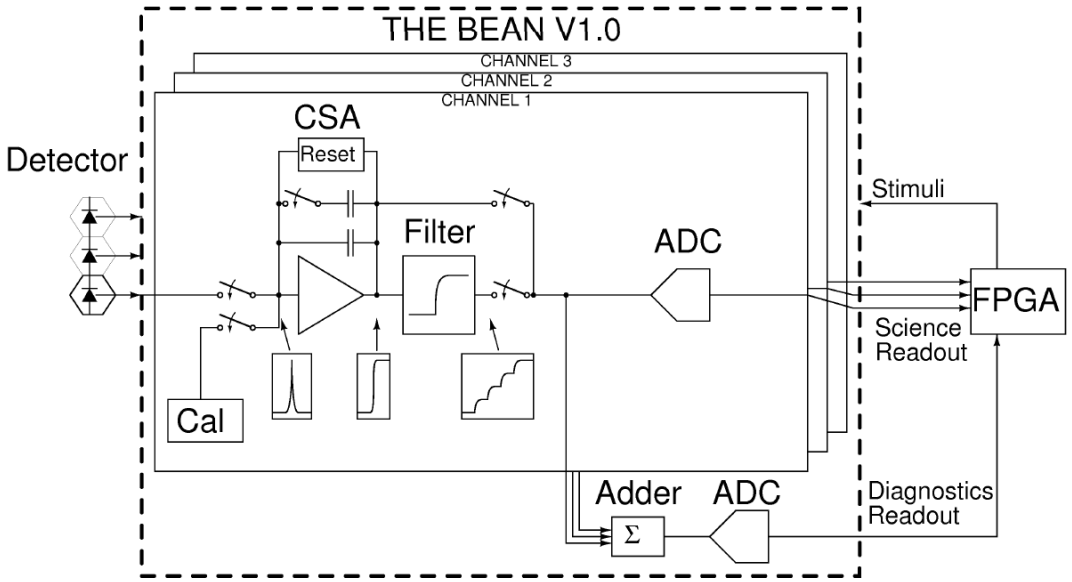
Analog Front-End measurements: Summary

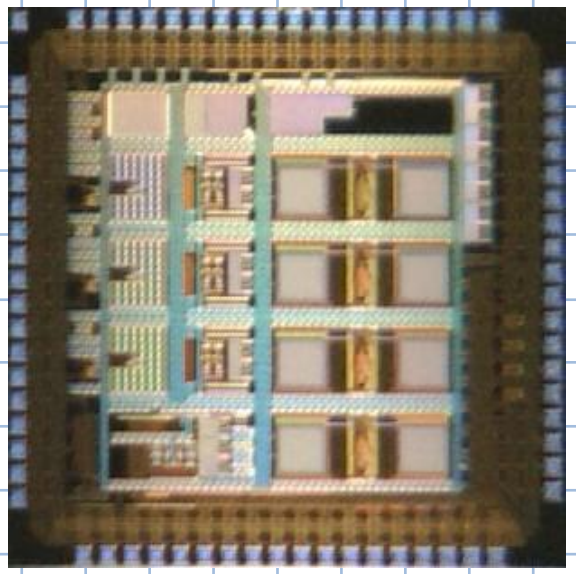
- Measurements results agree with simulations and specifications
  - Pulse shape and peaking time (50ns) as excepted
  - Gains in both modes differs within 10% from simulated
  - Baseline spread below 25 mV
  - Noise ENC at 10 pF below 1000 e-
  - Crosstalk measurements:
    - High gain – 0.64%
    - Low gain – 0.80%
  - Power consumption ~1.5 mW/channel – can be reduced by lowering bias currents
  - All parameters uniform between channels (two ASICs measured)

- Detector capacitance measurements needs to be finished...

ELECTRONICS FOR BEAMCAL

The Bean: 3-channel readout chain in 180nm (2010)

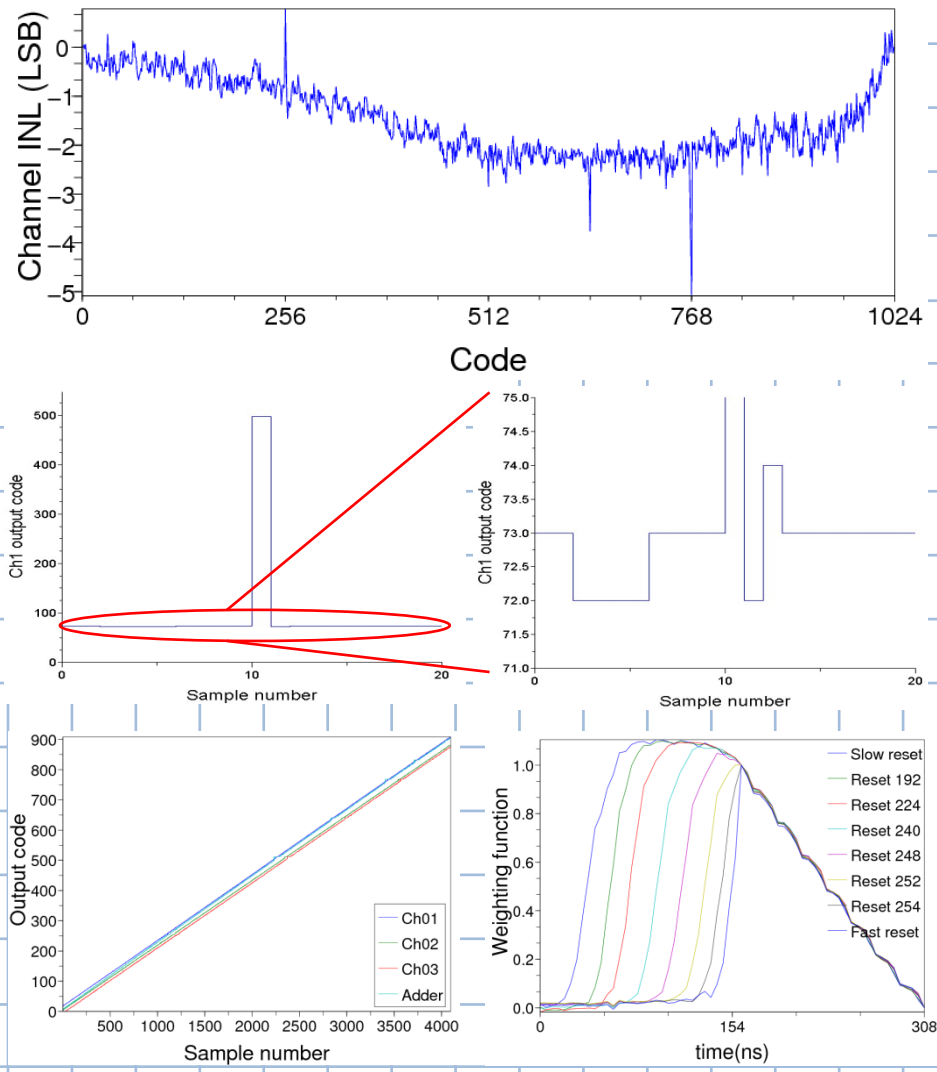




- 72 pads, 2.4mm x 2.4mm (including pads)
- 7306 nodes, 35789 circuit elements
- 360μm channel pitch (including power bus)
- 3 charge amplifiers, 4 x 10-bit, fully diff. SAR ADCs, 1 SC adder, 3 SC filters, etc.

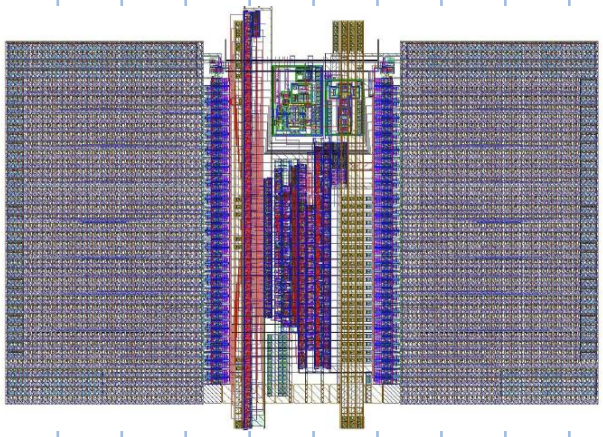
The Bean results summary (2010)

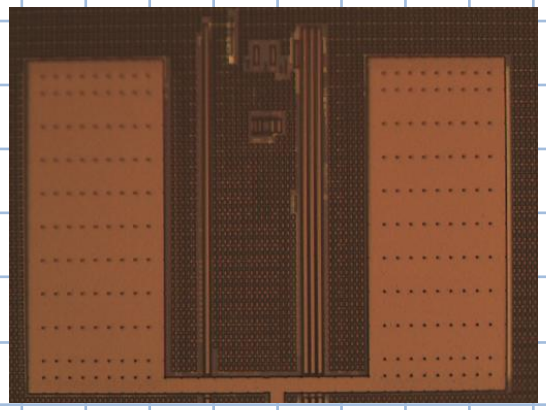
- The chip meets following specs:
  - Functionality
    - Dual gain, physics and calibration modes
    - Fast feedback
  - Input rate
  - Impulse recovery
  - Linearity
  - Noise in Science mode
- Useful as baseline design

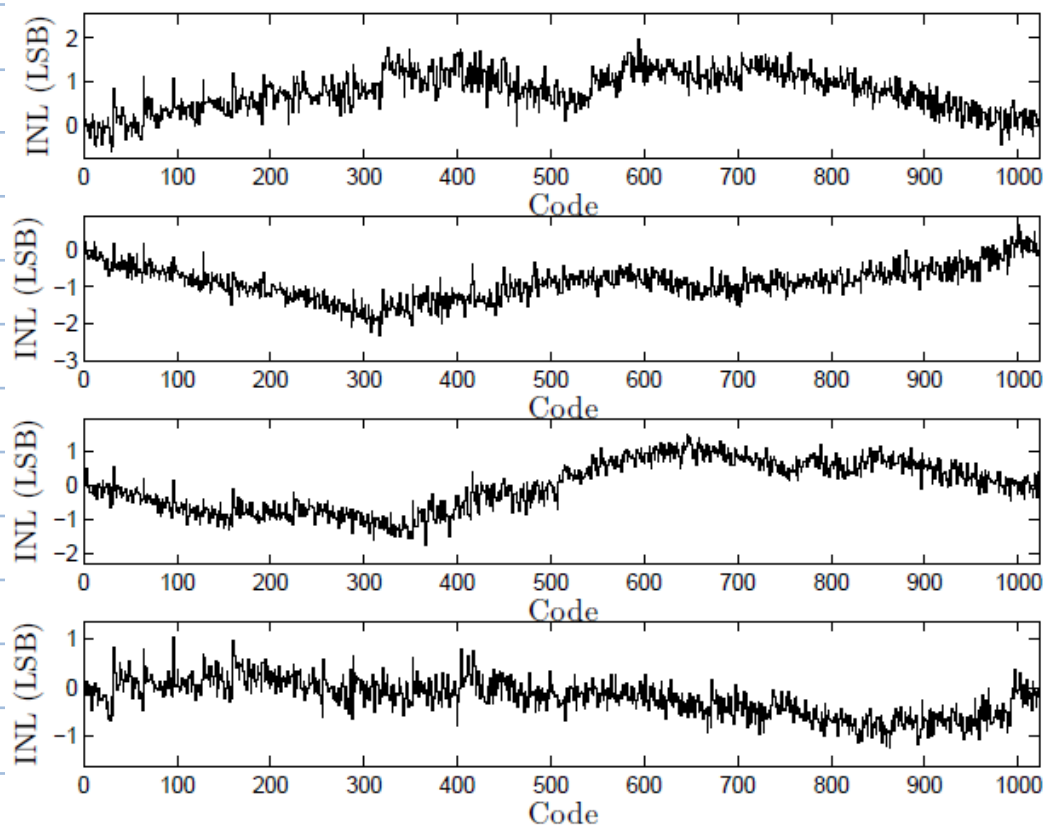


ADC linearity compensation (2012-2013)

ADC uses systematic process mismatch to correct nonlinearity

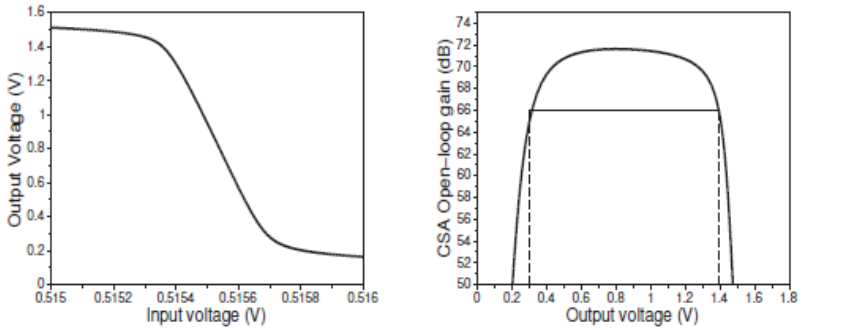






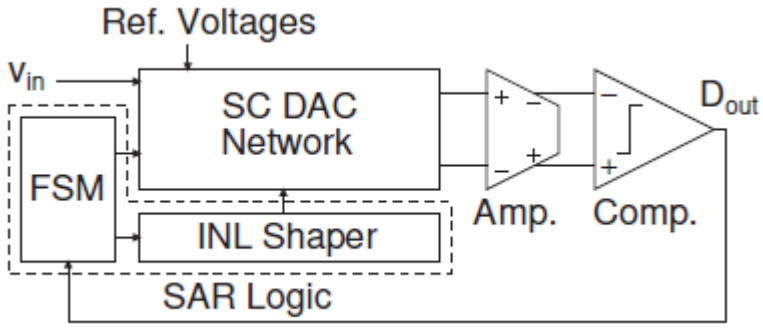
Linearity compensation results

The Bean CSA static transfer char.

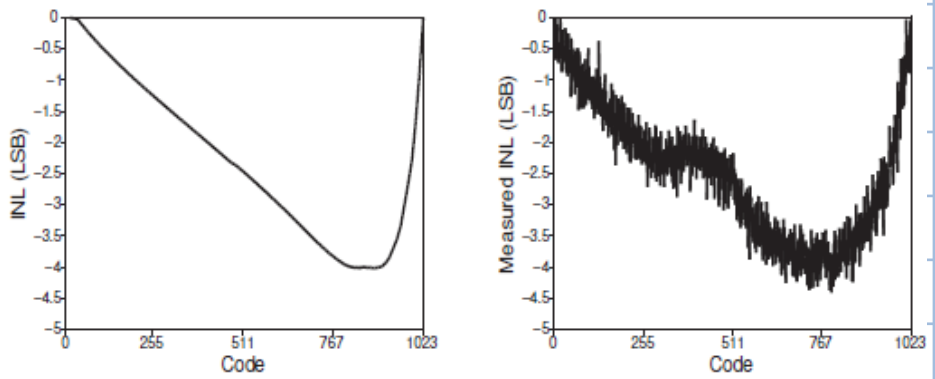


(a) Output voltage vs. input voltage. (b) Open-loop gain vs. output voltage.

Linearity compensation block diagram

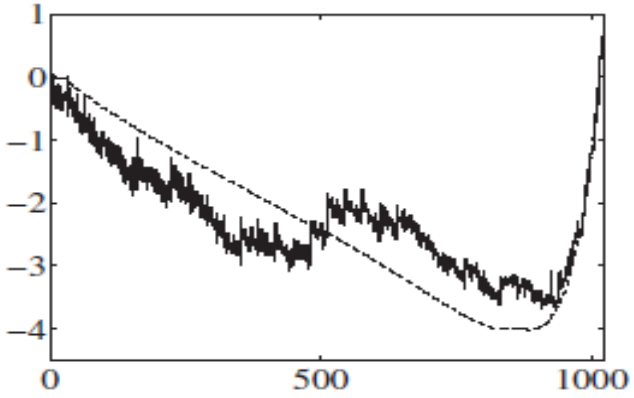


CSA INL (simulated and measured)



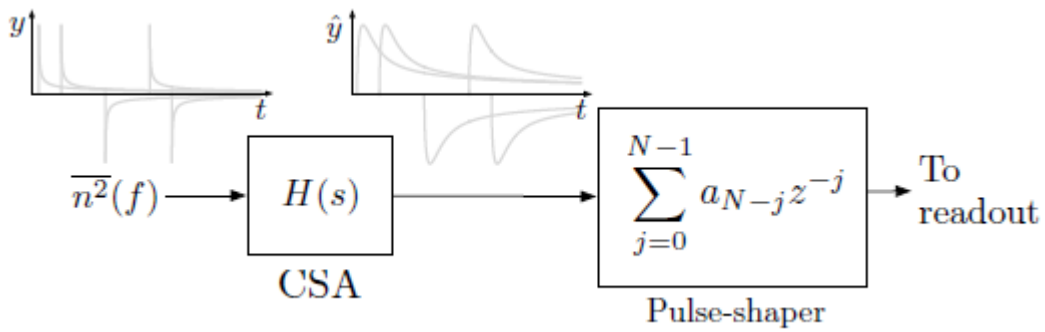
(a) Simulated results. (b) Experimental results.

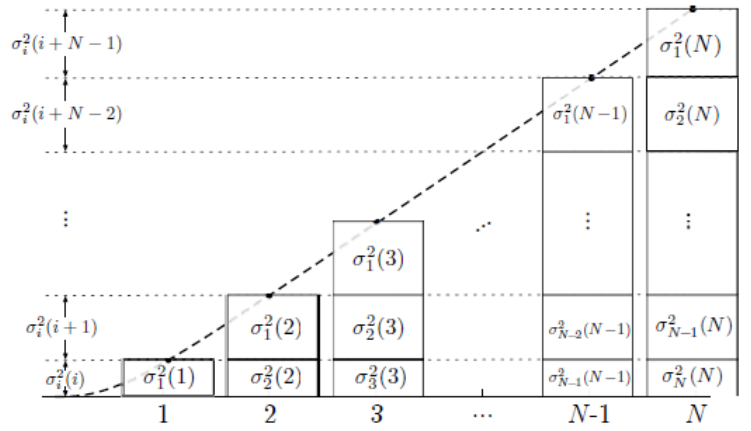
Example – INL with compensation

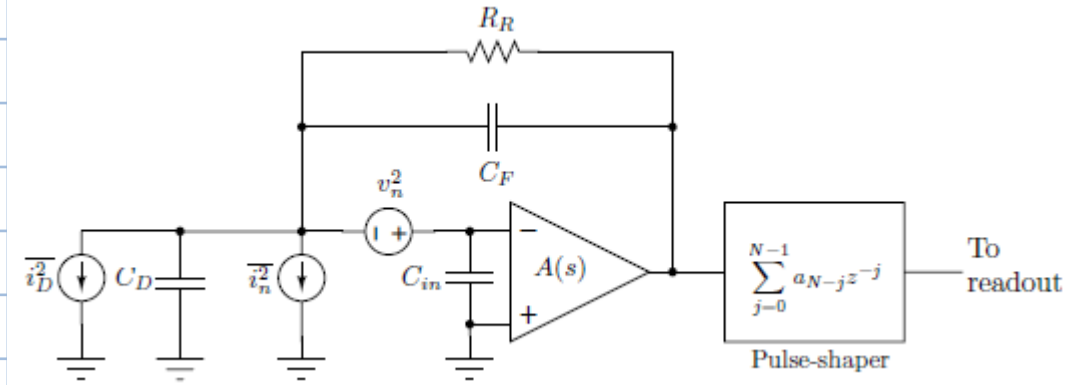


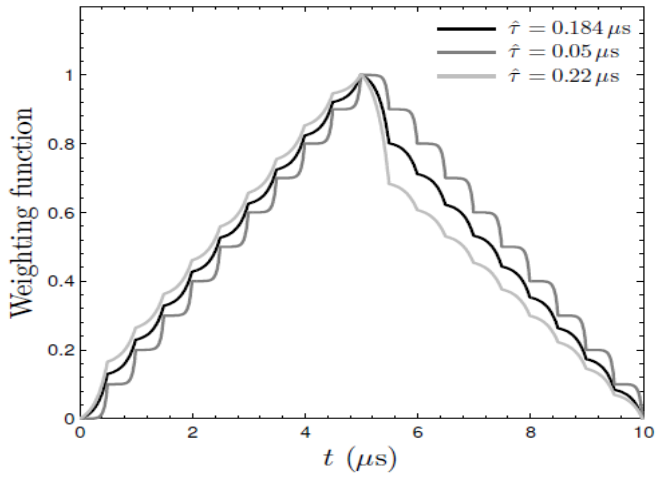
[Alvarez et al, TNS 2014 (submitted)

Arbitrary weighting function synthesis



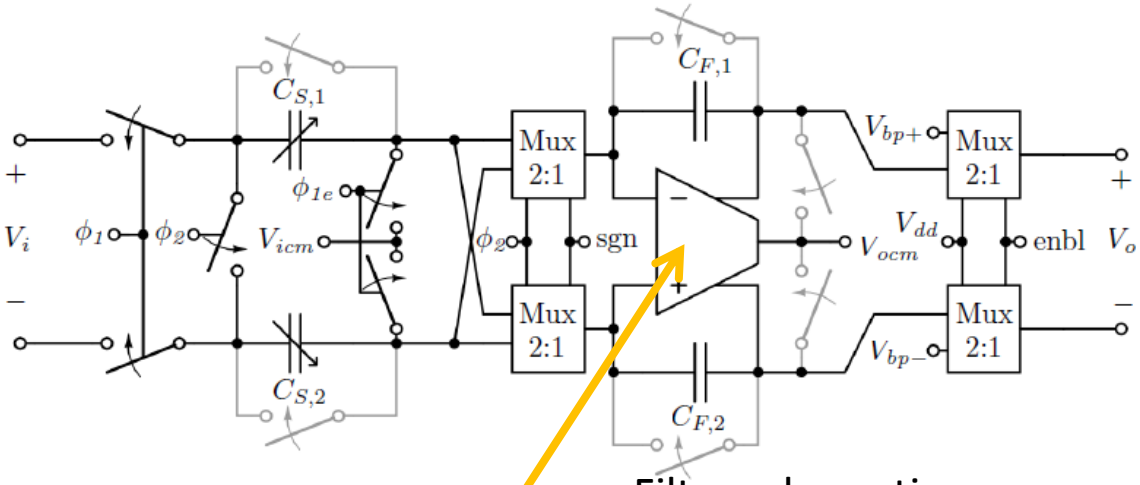




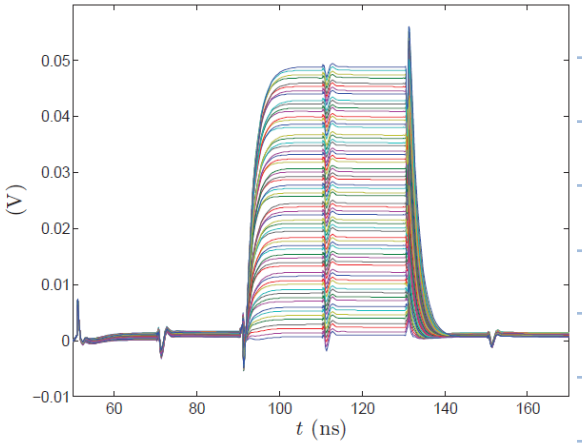


[Avila et al, TNS 2013]

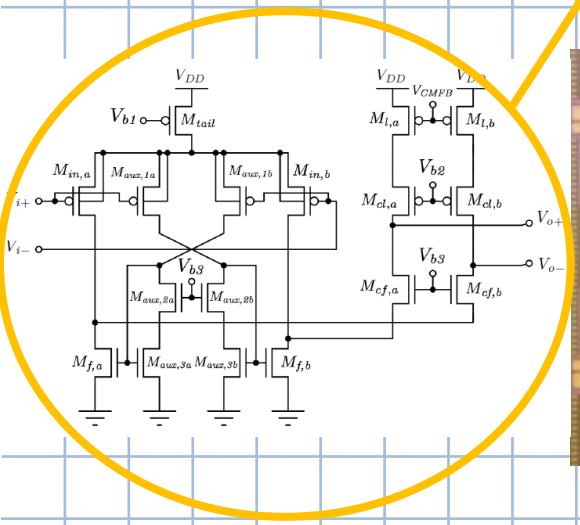
Chip design and fabrication (2013-2014)

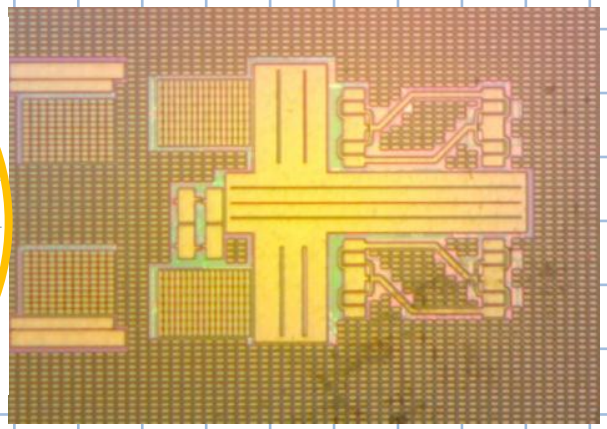


Filter schematics

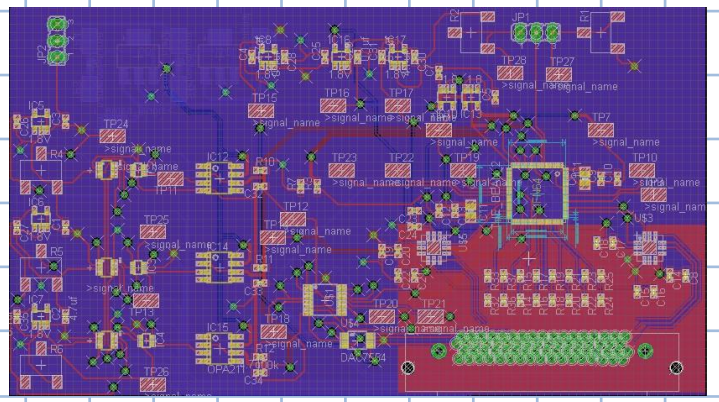


Transient simulations





Chip micrography



Board design

Intentionally-nonlinear ADC study

- The energy resolution of a sampling calorimeter can be described as

$$\frac{\delta E}{E} = \frac{A}{\sqrt{E}}$$

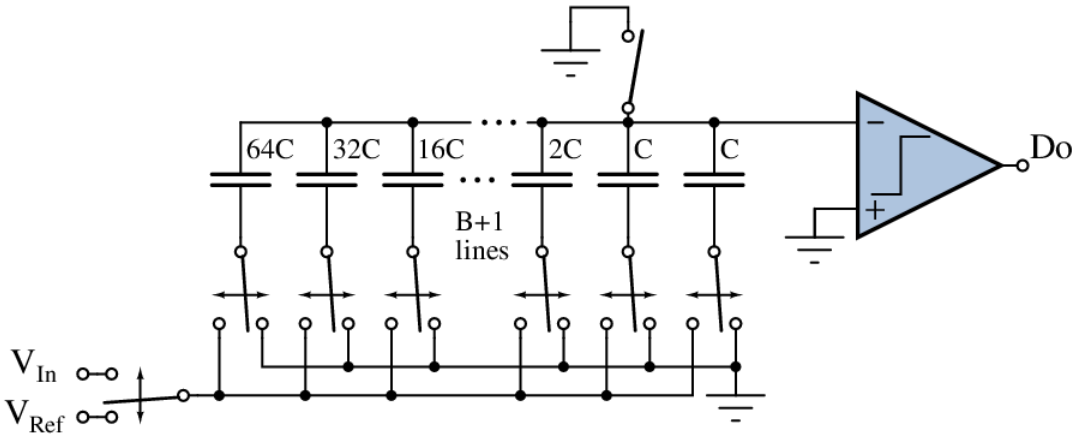
- Required resolution of electronics is a function of the shower energy
  - The bit size changes along the full scale range
  - Idea: to adjust the ADC resolution according to input
    - Otherwise, dynamic range specification is hard to meet

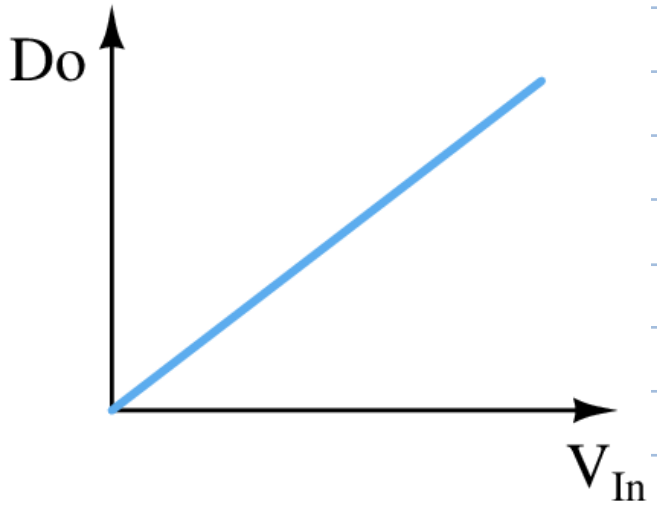
Example: ADC Dynamic range spec

- In BeamCal, the LSB for 1GeV should be 0.2GeV
  - Then, a linear ADC good for up to 1TeV needs 1000/0.2=5000 codes, or **13 bits**
  - However, if the ADC resolution matches the fundamental resolution of a sampling calorimeter, only **8 bits** are required to represent all the information space!
- This does not relax the front-end dynamic range
  - We still want to have a linear CSA
  - This is also required for fast feedback estimations

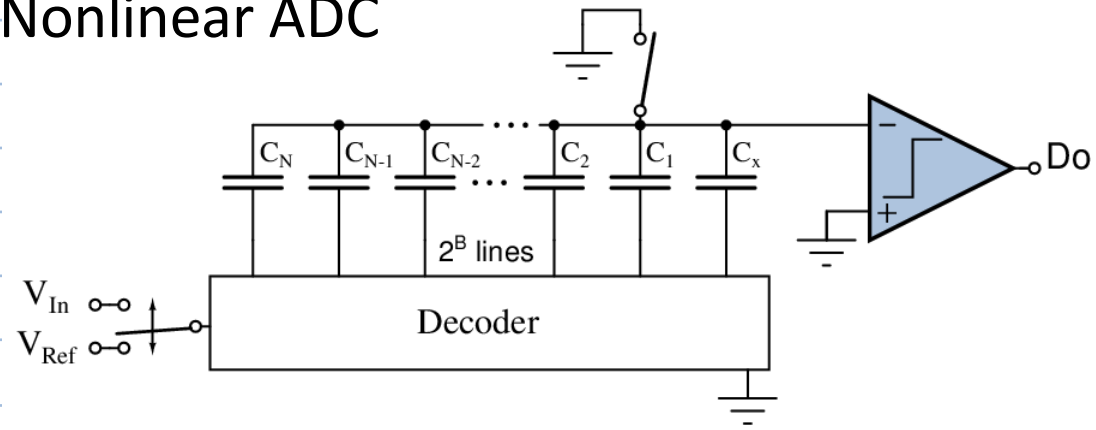
Linear vs. nonlinear ADC design

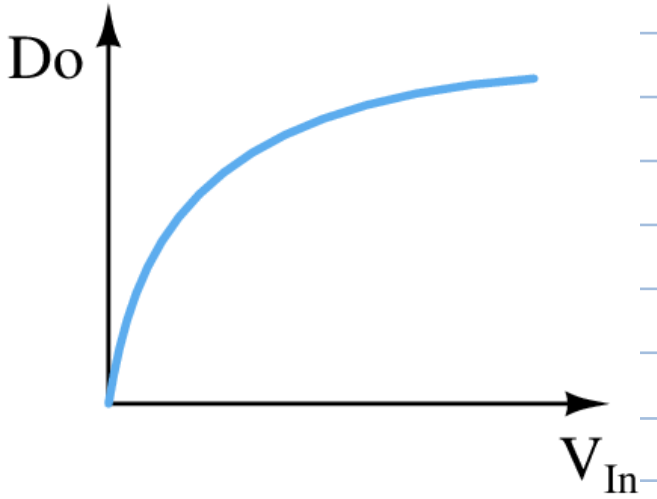
Linear ADC





Nonlinear ADC





To nonlinearize… or not?

SIZE COMPARISON BETWEEN DIFFERENT FULLY-THERMOMETER-CODED SAR ADCS.

	Capacitor Array (C_{tot})	Decoder	Digital Core	Comparator	Amplifier
Standard Linear	$c_u \cdot 2^B$	$\propto 2^B L_{min}$	$\propto B \cdot L_{min}$	$\propto L_{min}$	$\propto L_{min}$
s-section Piecewise	$c_u \cdot 2^B \sum_{i=1}^{s} \alpha_i 2^{\Delta_i}$	$\propto 2^B L_{min}$	$\propto B \cdot L_{min}$	$\propto L_{min}$	$\propto L_{min}$
Fully Nonlinear	$c_u \cdot \sum_{i=1}^{N_{nl}} k_i$	$\propto 2^B L_{min}$	$\propto B \cdot L_{min}$	$\propto L_{min}$	$\propto L_{min}$

- Tradeoff between capacitor array size and decoder size
- But 8 bits instead of 13 bits of resolution!
- Still working on this…

Electronics for FCAL: Summary

- **AGH and PUC are designing electronics for FCAL**
  - AGH: LumiCal, current design also works for BeamCal
  - PUC: BeamCal, now converging through non-standard design ideas
- **LumiCal**
  - Readout IC in AMS0.35 which we still want to use for multiplane tests
  - 8-channel front-end in CMOS 130 nm, good for test-beam purpose and FCAL studies
  - Successfully designed and tested a 10-bit SAR ADC in CMOS 130nm
  - New 8 channel 10-bit SAR ADC in CMOS 130nm waiting for tests (next 2 months)
- **BeamCal**
  - 3-channel Readout chain in 180nm (2010), tested
  - ADC linearity compensation (2012 – 2013)
  - Arbitrary weighting function synthesis (2013 – 2014)
  - Intentionally nonlinear ADC (ongoing work)

Electronics for FCAL: Future plans

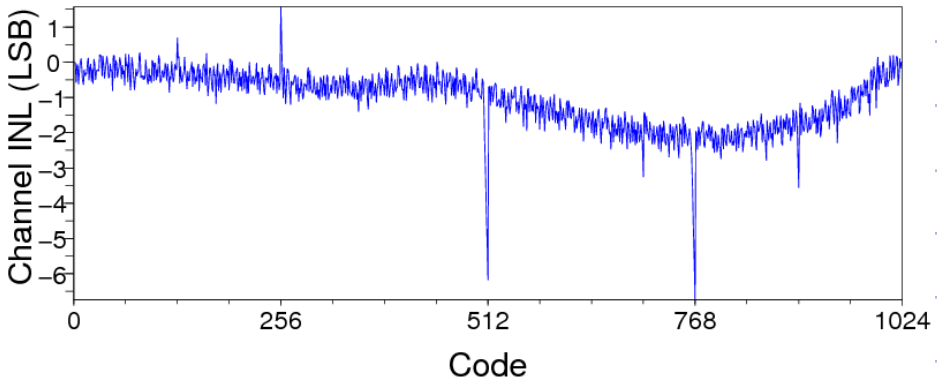
- AGH, 2015: Design and submit complete multichannel ASIC for LumiCal (or two ASICs: FE+ADC) with front-end and ADC in each channel plus various DACs, serializers etc.
- PUC, 2015: Design and test a multichannel FE and ADC IC for BeamCal
  - Synchronous and asynchronous readout
- Joint collaboration:
  - Eventually converge to the same technology and process
  - Share IP/fabrication runs
  - Student/researcher visits

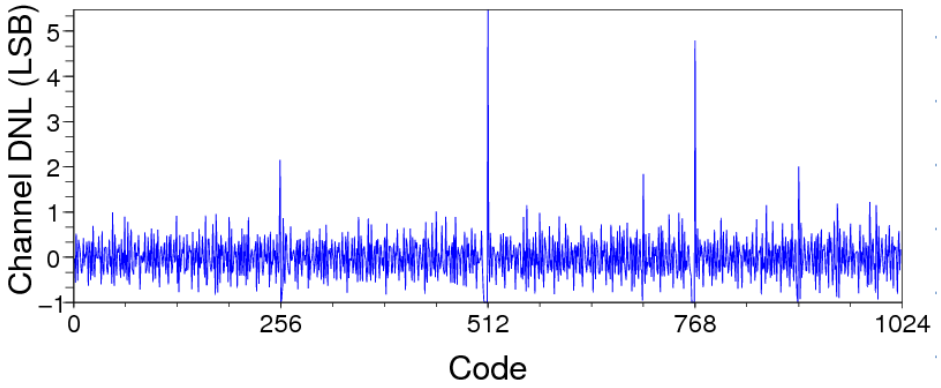
Thank you!

BACKUP MATERIAL

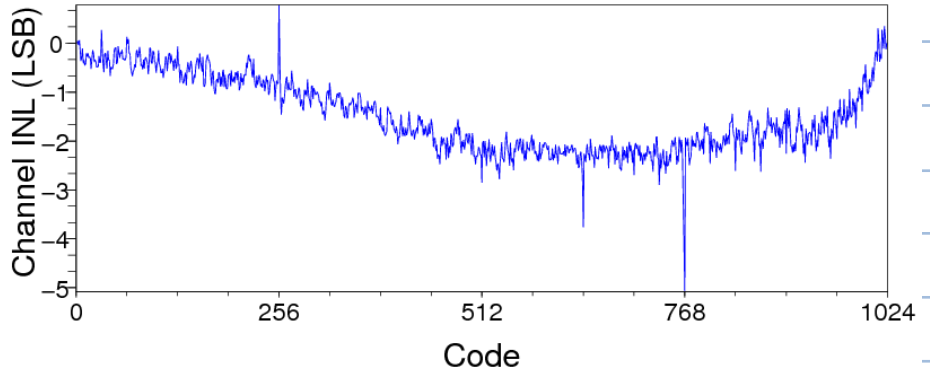
The Bean Linearity Test Results

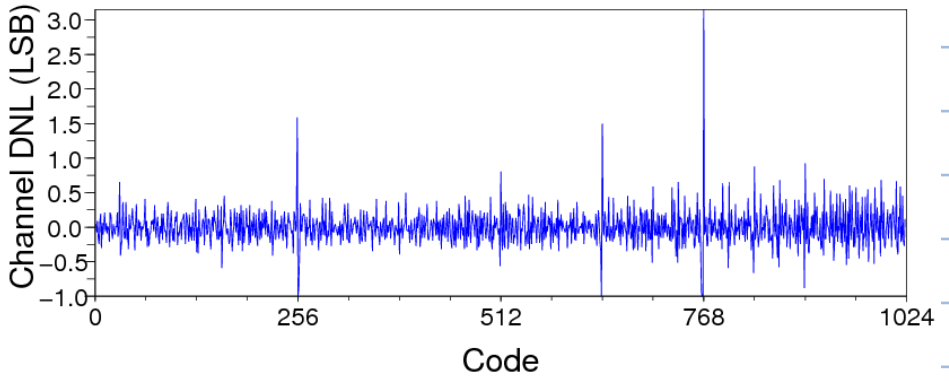
37 pC input (SDT)





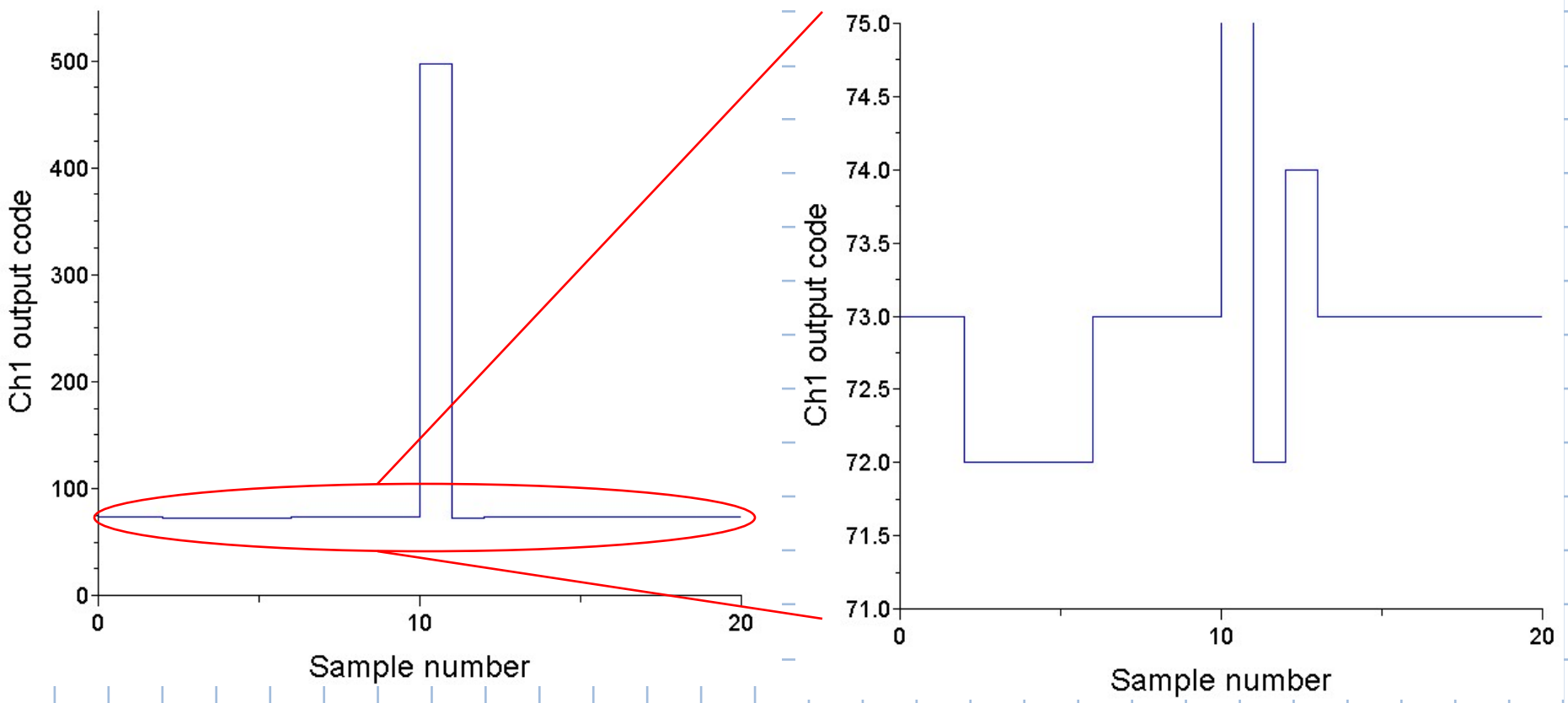
0.74 pC input (DCal)





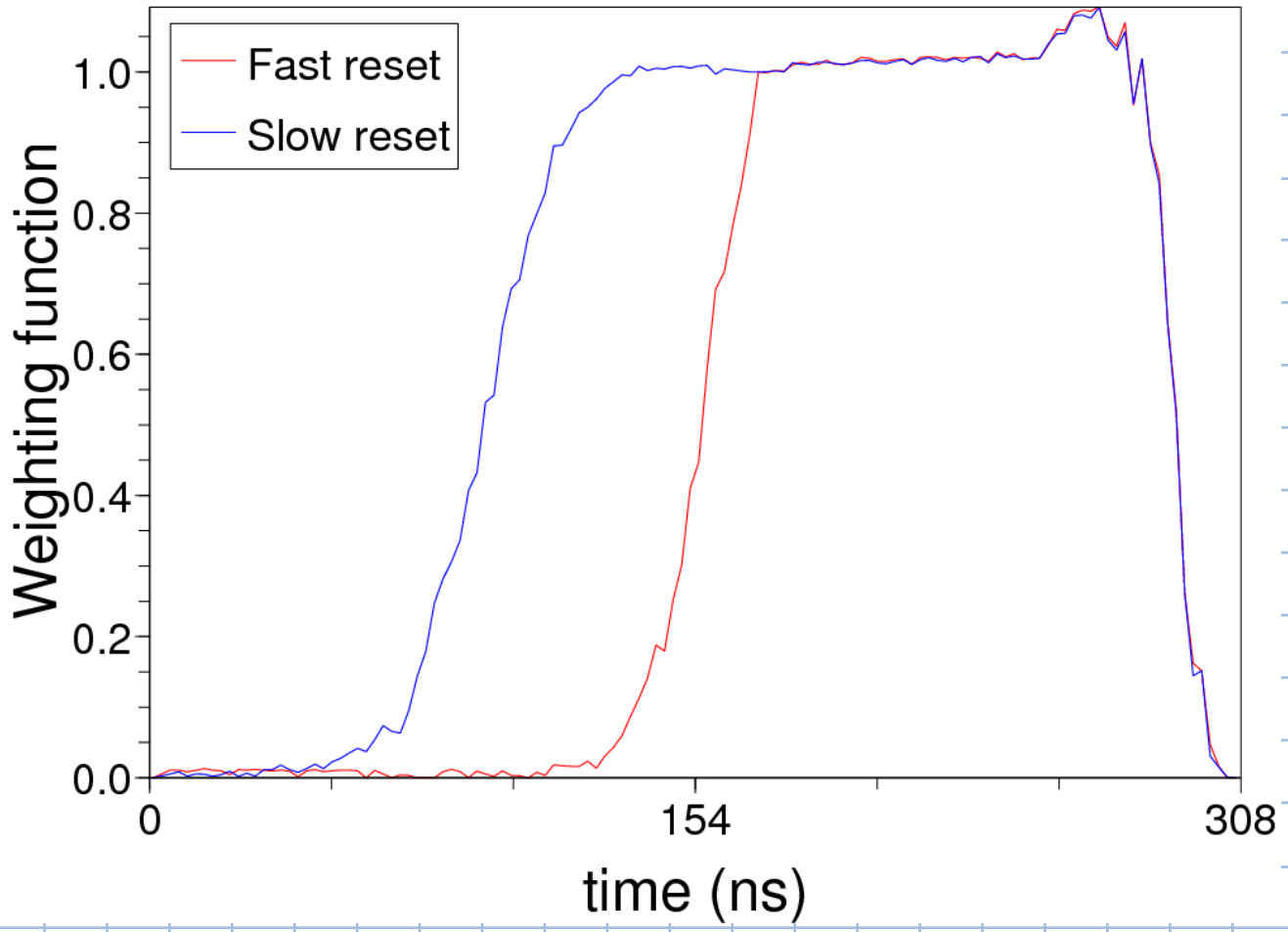
The Bean Bandwidth test results

- Input injected on 10th cycle only
- Digital output recorded, nominal speed



The Bean
Weighting function measurement, SDT

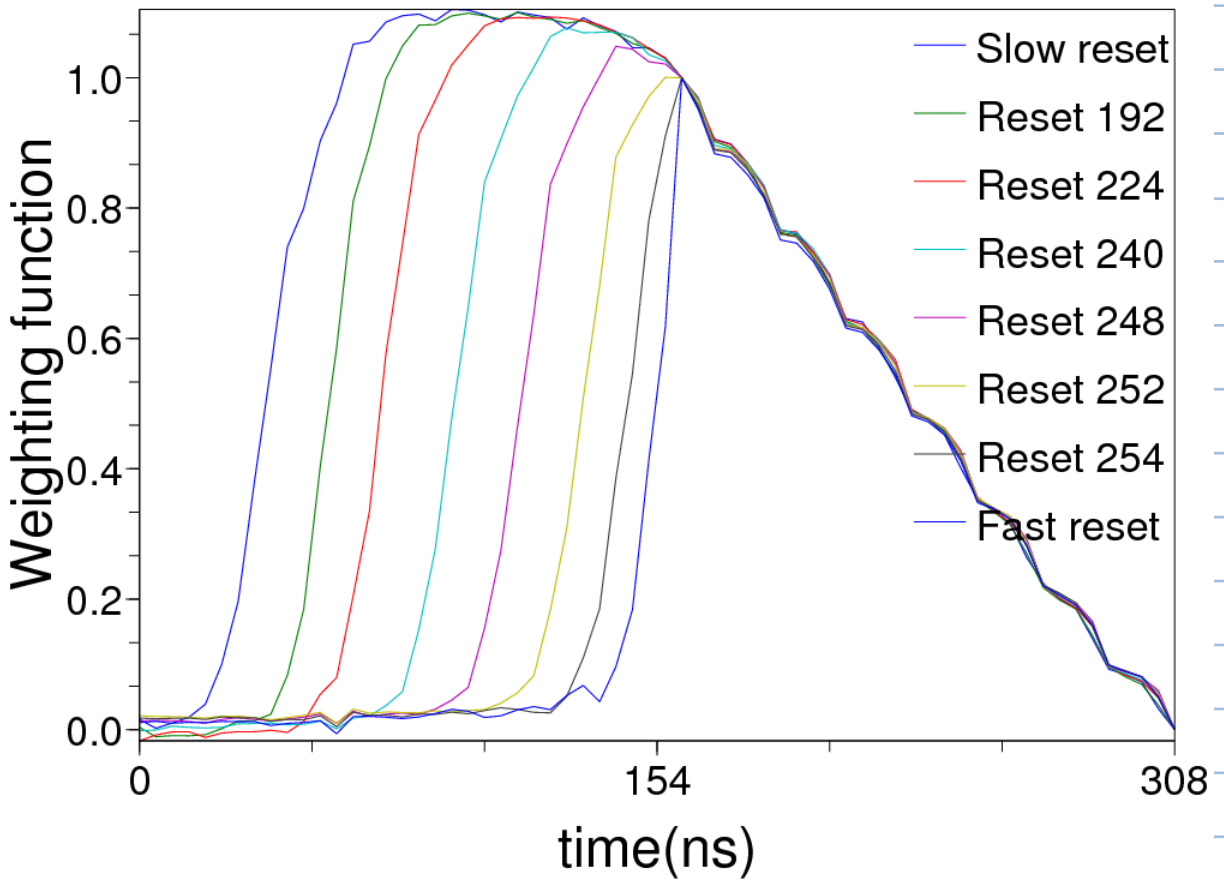
Time resolution: 4.8 ns



The Bean
Weighting function measurement, DCal

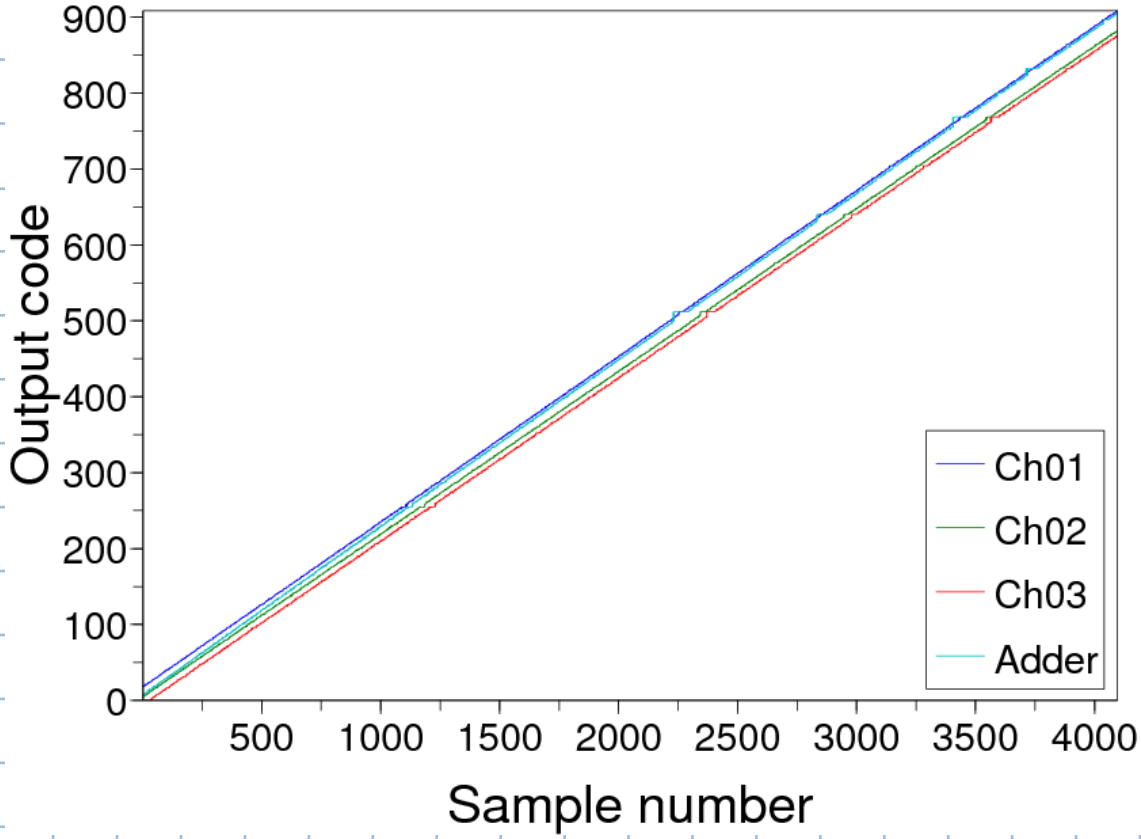
Time resolution: 4.8 ns

Series noise coefficient ranges from $37.6\times10^6\ s^{-1}$ to $59.3\times10^6\ s^{-1}$

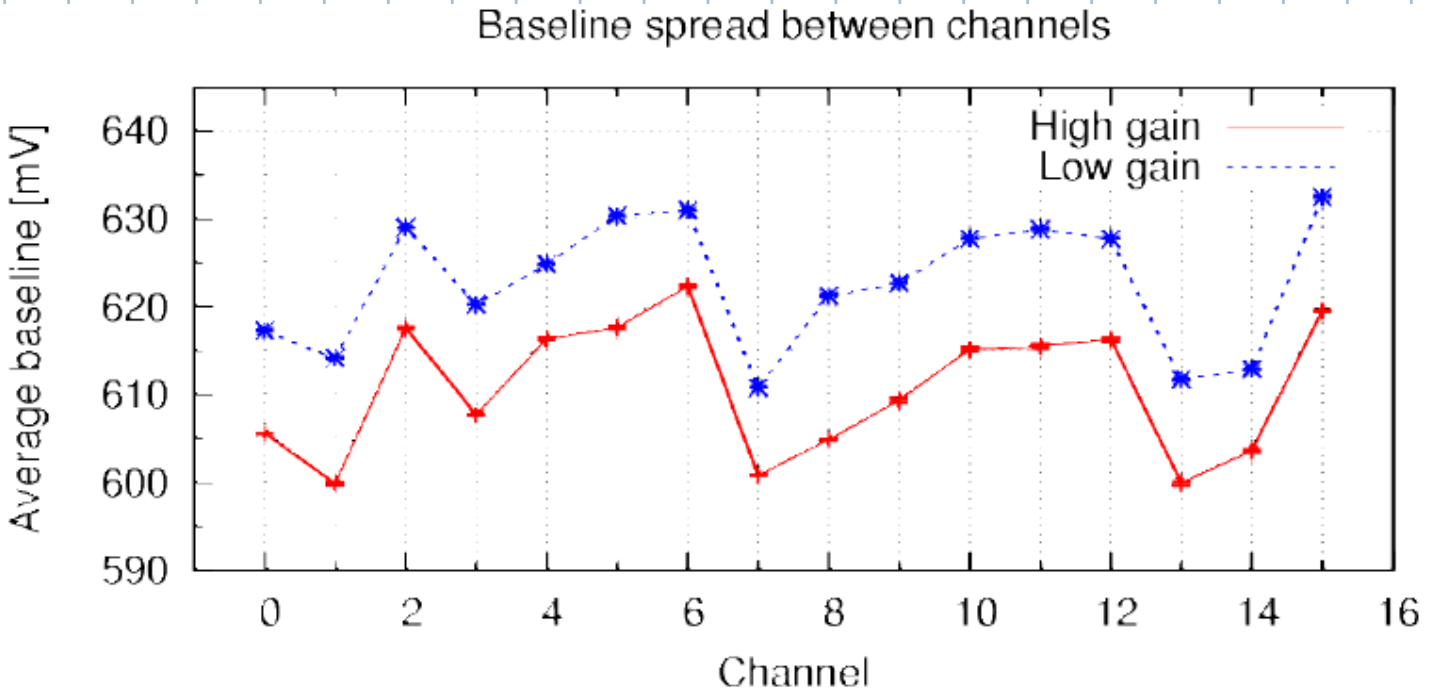


The Bean
Fast feedback adder measurement

- Adder proved full functionality at nominal speed of operation
- Gains from individual channels to Adder range from 0.329 to 0.345

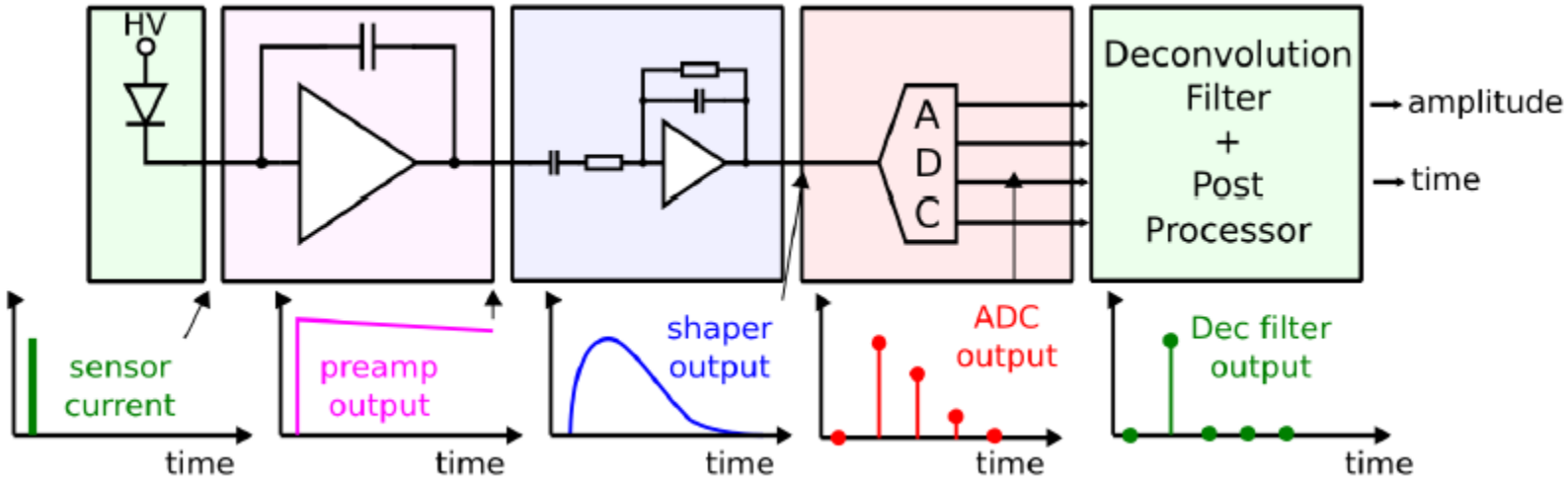


LumiCal Analog Front-End measurements: Baseline spread



- Baseline spread is below 25 mV for both gains - in agreement with shaper opamp offset simulations
- Baseline spread in high gain – 600 mV to 622 mV
- Baseline spread in low gain – 610 mV to 633 mV

LumiCal readout electronics diagram – Deconvolution theory



- Pulse at output of shaper v(t) is convolution of input signal (current from sensor – s(t)) and impulse response of readout chain h(t):

$$v(t)=\int_{-\infty}^{+\infty} h(t-x)\,s(x)\,dx$$

- Using data from continuously running ADC and taking advantage of known pulse shape one can perform invert procedure – **deconvolution** – to get information about event time and amplitude

Deconvolution for CR-RC shaping - Theory

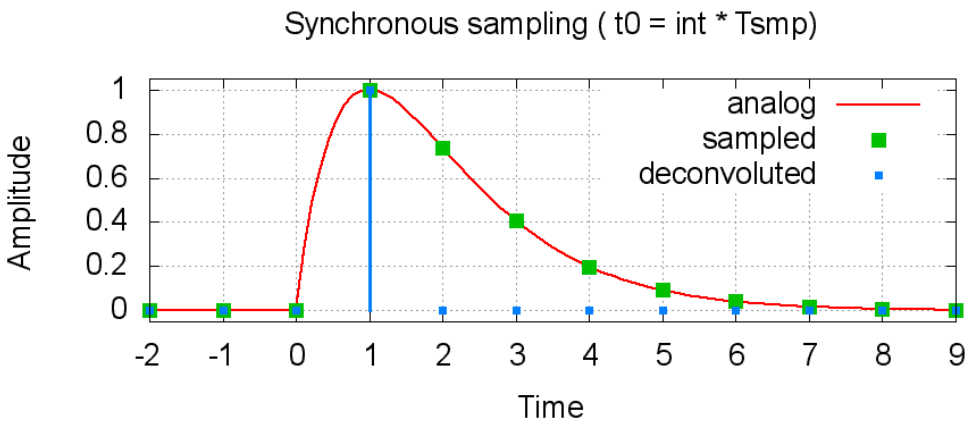
$$d_i = s_i + w_1 s_{i-1} + w_2 s_{i-2}$$

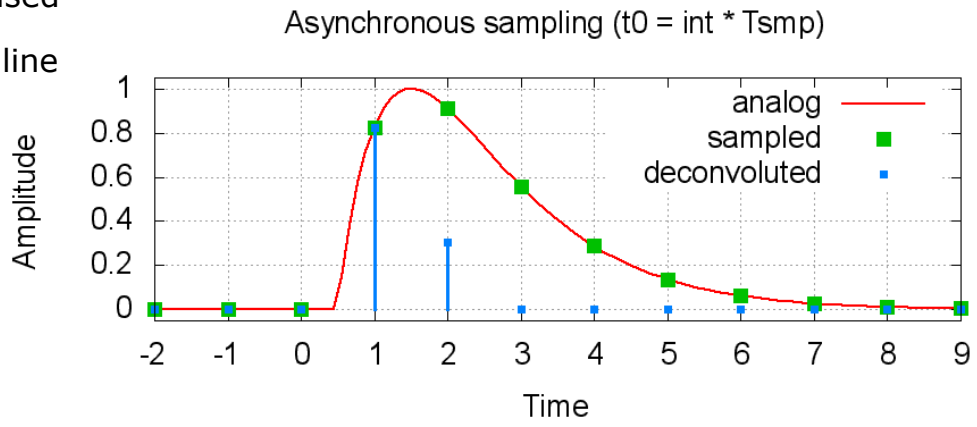
CR-RC, $T_{smp}=T_{peak}=1$, amp =1

- Only two multiplications and three additions (very fast and light !)
- Deconvolution produces non-zero data only when one or two first samples are on baseline,
  and second/third is on pulse
- **Initial time** of pulse is found from ratio of those samples

} Look Up Tables used
Can be done off-line

- **Amplitude** is found from sum of those samples, multiplied by time dependent correction factor
- Deconvolution reduces (infinite number) of CR-RC pulse samples to 1 or 2 non zero samples !





Deconvolution for CR-RC shaping
Real, averaged, FE pulses

- Real pulse (1 MIP) deconvoluted for various phase shift t0 between the Front-End pulse and ADC sampling
- Deconvolution done for different sampling periods (12.5, 25 and 50 ns are presented)
- **Amplitude reconstruction** (top plot) – deconvoluted to real pulse amplitude ratio
  - Error is below 2% except 12.5 ns sampling period
- **Time reconstruction** (bottom plot) – difference between reconstructed and real pulse peak position
  - Constant offset of around 2 ns except 50 ns sampling period
- **S/N after deconvolution still to be measured...**