CPS Performances Expected from a 180 nm CIS Process for the ILD Vertex Detector

M. Winter (on behalf of the PICSEL group of IPHC-Strasbourg)

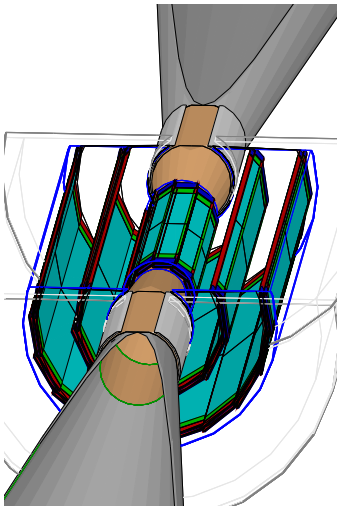
- ALPIDE chip : ALICE/CERN coll.

LCWS14, Beograd, 7 Octobre 2014

Outline

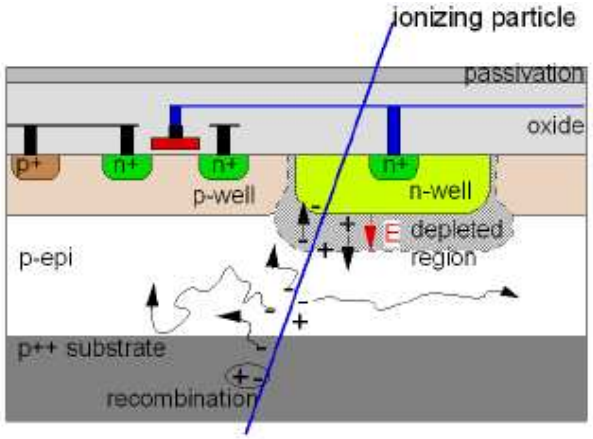
- *VXD concept addressed :* 2-sided ladders with different CPS on L1, L2, L3-6
- *Starting points : STAR-PXL & ALICE-ITS*
- *Extrapolated performances for VXD-L1 & -L2 (mainly)*
- *Summary & Conclusion*

Topics Addressed by the R&D

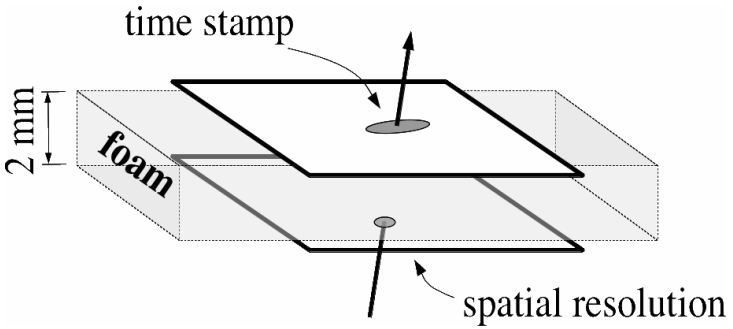


- VERTEX DETECTOR CONCEPT :
  - Cylindrical geometry based on 3 concentric 2-sided layers
  - Layers equipped with 3 different CMOS Pixel Sensors (CPS)

- PIXEL SENSOR DEVELOPMENT:
  - Exploit CPS potential & CMOS technology evolution
  - R&D performed in synergy with other applications
    $\hookrightarrow$ EUDET-BT, STAR, ALICE, CBM, ...
  - CPS $\equiv$ unique technology being simultaneously
    granular, thin, integrating full FEE, industrial & cheap
  - Address trade-off between spatial resolution & read-out speed



- DOUBLE-SIDED LADDER DEVELOPMENT:
  - Develop concept of 2-sided ladder using 50 μm thin CPS
  - Develop concept of mini-vectors providing
    high spatial resolution & time stamping
  - Address the issue of high precision alignment
    & power cycling in high magnetic field



CMOS Pixel Sensors (CPS): A Long Term R&D

- ***Initial objective: ILC, with staged performances***
  - *CPS applied to other experiments with intermediate requirements*

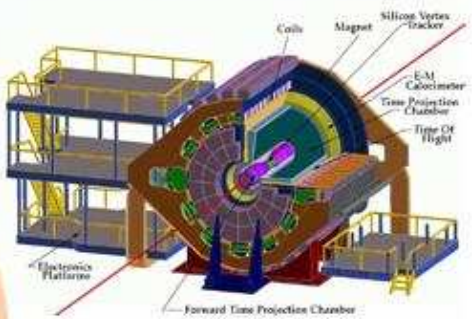
EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadron physics)
CLIC (Particle physics)
BESIII (Particle physics)
...

EUDET 2006/2010

Beam Telescope

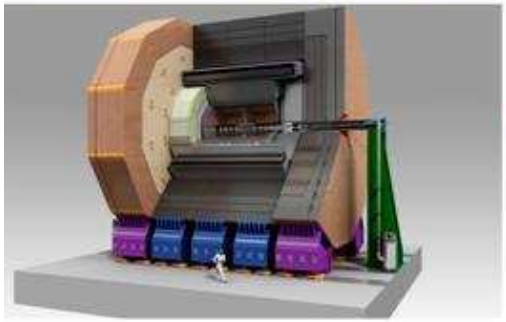
STAR 2013

Solenoidal Tracker at RHIC



ILC >2020

International Linear Collider

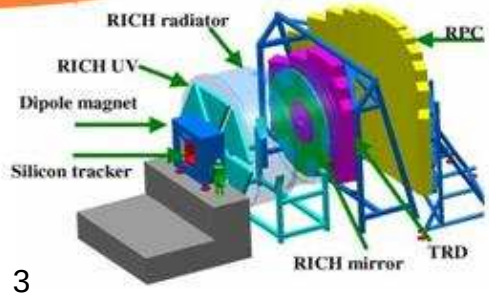


ALICE 2018

A Large Ion Collider Experiment

CBM >2018

Compressed Baryonic Matter

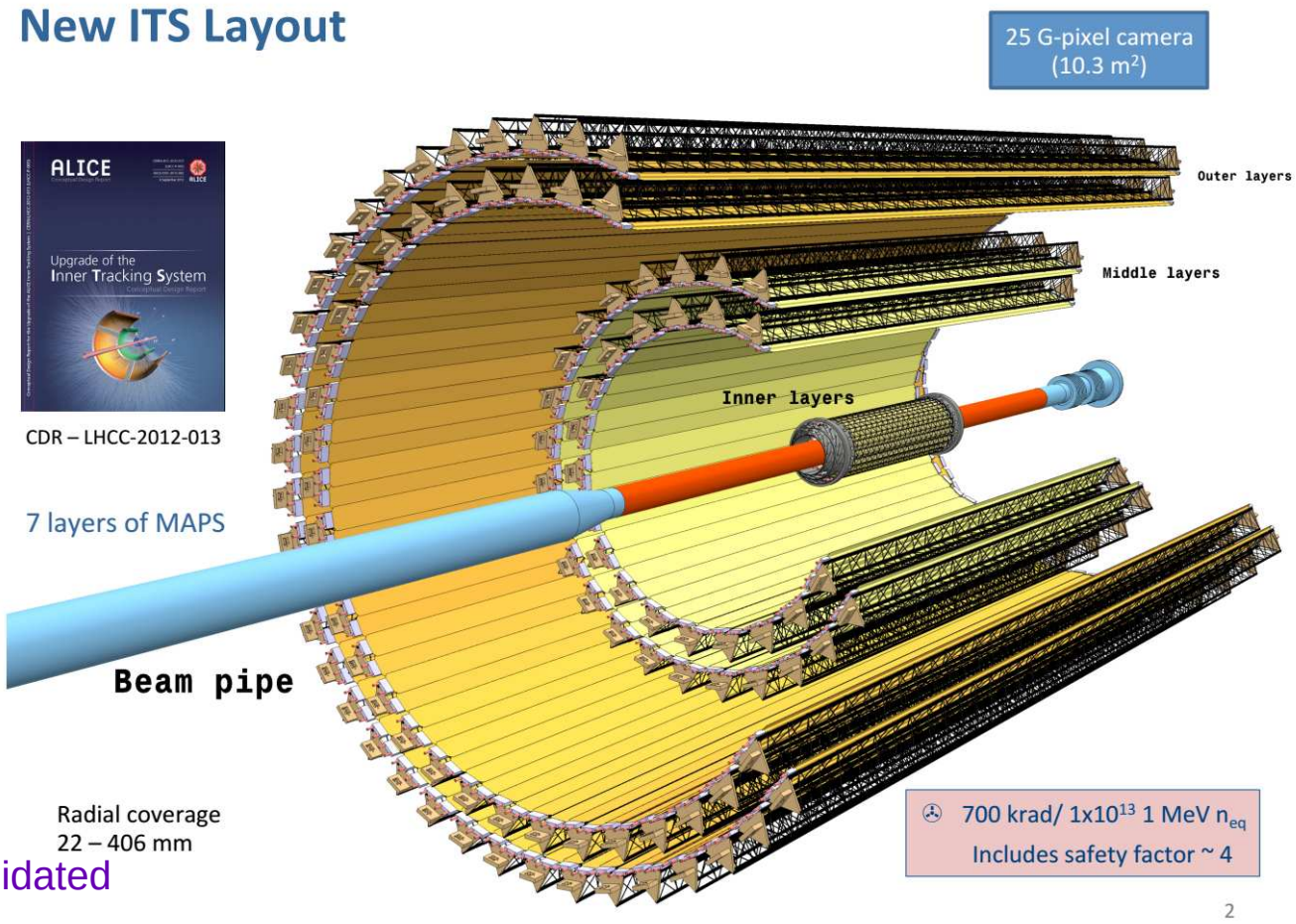


State-of-the-Art : STAR-PXL

Validation of CPS for HEP (25/09/14 : DoE final approval, based on vertexing performance assessment)

Next Progress Driver : ALICE-ITS Upgrade

- Vx Det. (3 layers) + Tracker (4 layers, 10 m^2) : 5 μm, 20-30 μs, 700 kRad & 10^{13} n_{eq}/cm^2 at 30°C
- 3 alternative & complementary sensors being developped (CERN main partner):
  - Conservative: **MISTRAL** (end-of-col. discri.)
    $\hookrightarrow \gtrsim 30\ \mu s, < 200$ mW/cm^2
  - Fast option: **ASTRAL** (in-pixel discri.)
    $\hookrightarrow \gtrsim 15\ \mu s$, 85 mW/cm^2
  - Ambitious: **ALPIDE** (token ring archi.)
    $\hookrightarrow \lesssim 5\ \mu s, \lesssim 50$ mW/cm^2

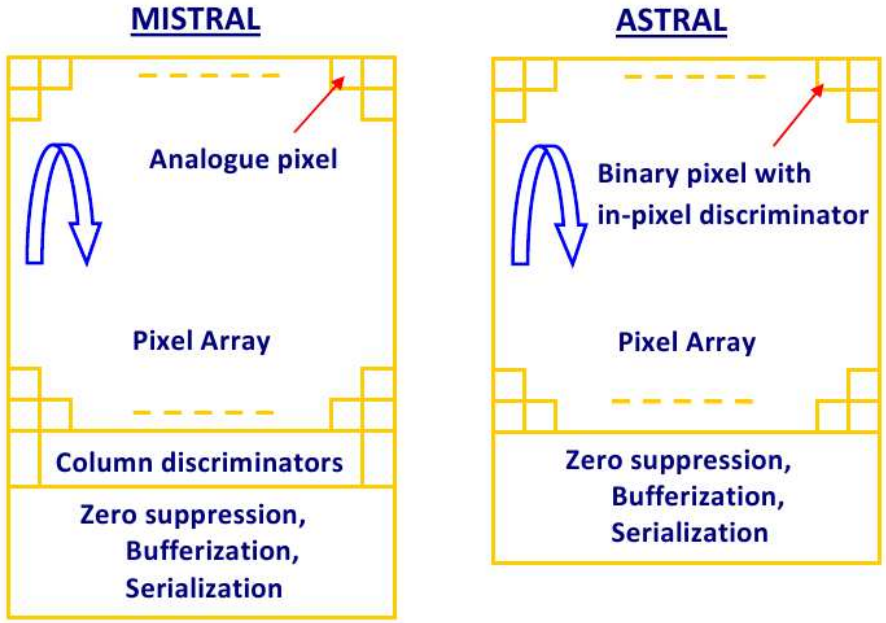


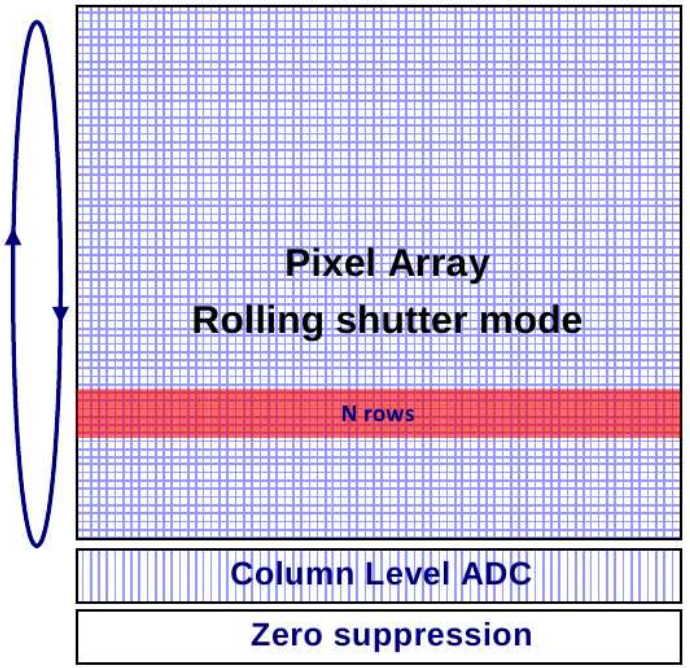
- Status :
  - MISTRAL : real scale proto. operational
    $\hookrightarrow$ (5 μm, 40 μs)
  - ASTRAL : in-pixel discriminator prototype validated
    $\hookrightarrow$ (5 μm, 20 μs)
  - ALPIDE (CERN based development) : full scale prototype functional $\mapsto$ (5-6 μm, 4-5 μs)

✳ read-out time is for 1.3/1.4 cm long columns $\simeq$ 2-2.5 $\times$ VXD-L1 column length (for same pixels)

Synchronous Read-Out Architecture : Rolling Shutter Mode

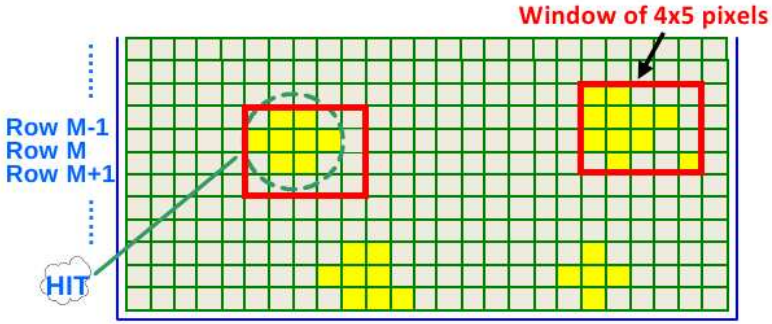
- *Design addresses 3 issues:*
  - *Increasing S/N at pixel-level*
  - *A to D Conversion: at column-level (MISTRAL)*
    at pixel-level (ASTRAL)
  - *Zero suppression (SUZE) at chip edge level*





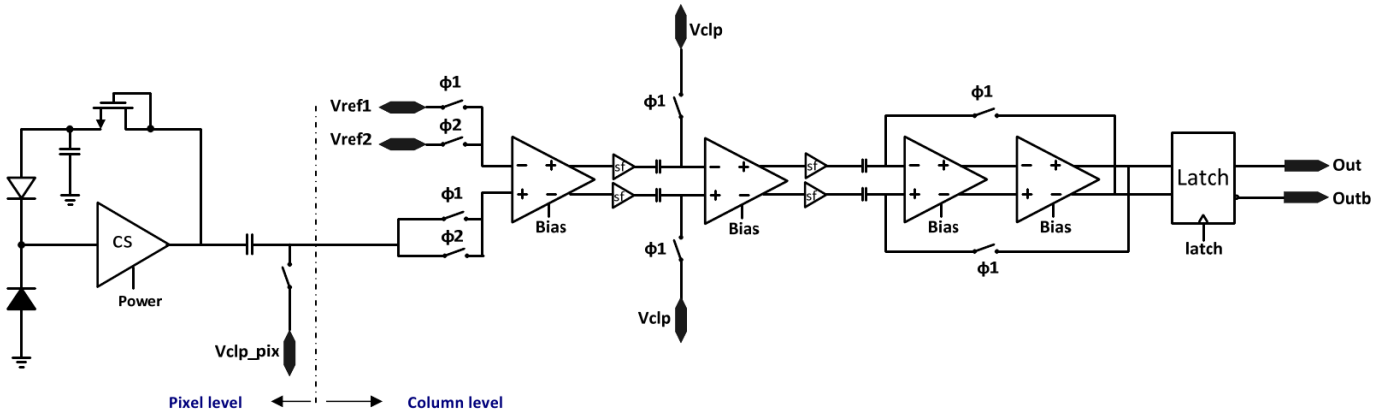
- *Power vs speed:*
  - *Power: only the selected rows (N=1, 2, …) to be read out*
  - *Speed: N rows of pixels are read out in //*
    - *Integration time = frame readout time*

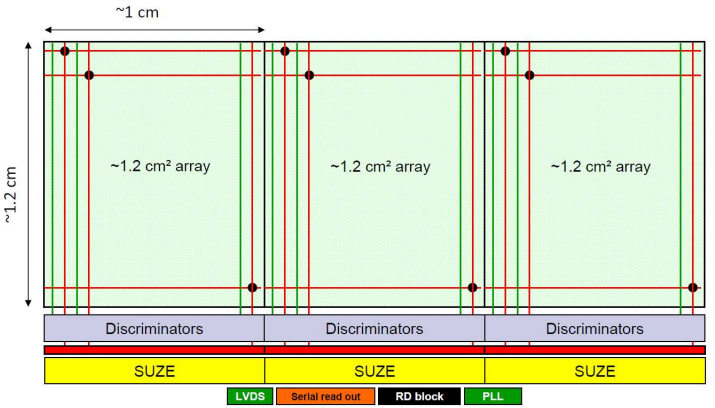
$$t_{\text{int}} = \frac{(\text{Row readout time}) \times (\text{No. of Rows})}{N}$$



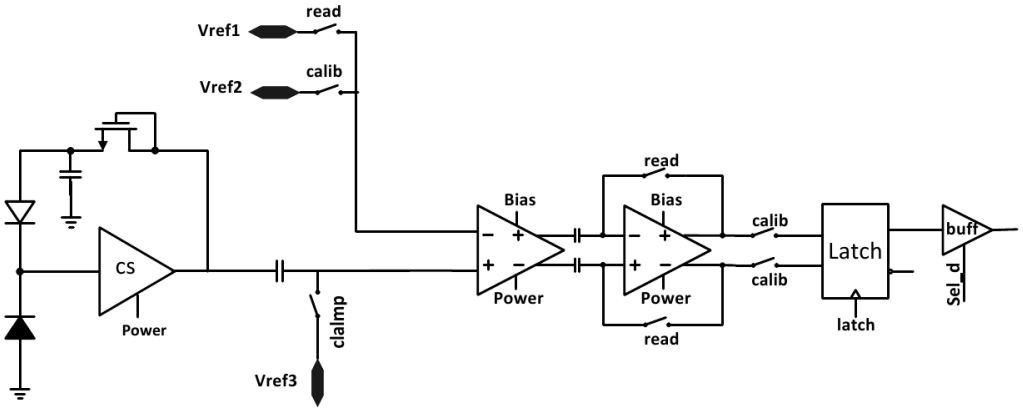
MISTRAL & ASTRAL : Schematics & Layouts

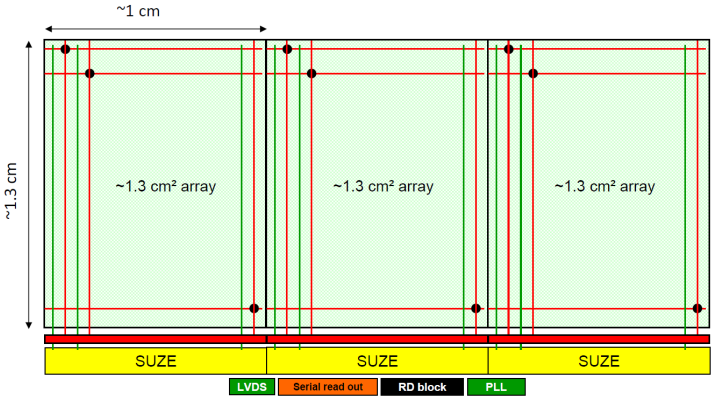
- **MISTRAL :** rolling shutter with 2-row read-out **& end-of column discriminators**





- **ASTRAL :** rolling shutter with 2-row read-out (≡ MISTRAL) **& in-pixel discriminators**



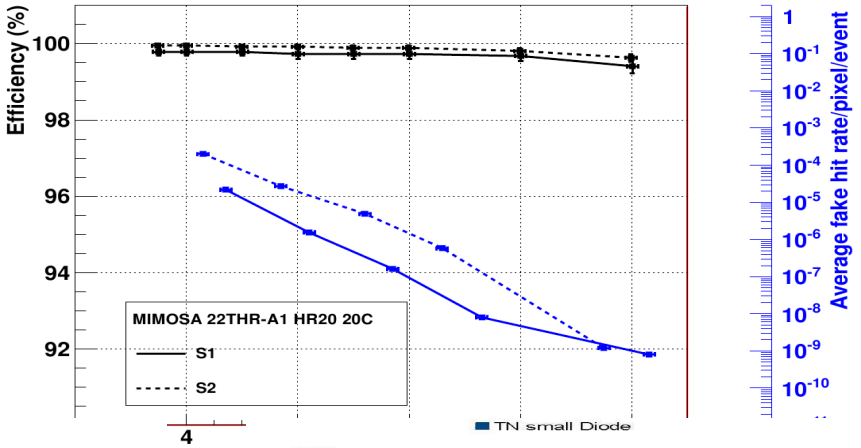


- **1st Full Scale Building Blocks (FSBB) fab. in Spring ’14 ⟼ FSBB-M0 lab tests ± completed**

MISTRAL Architecture Validation

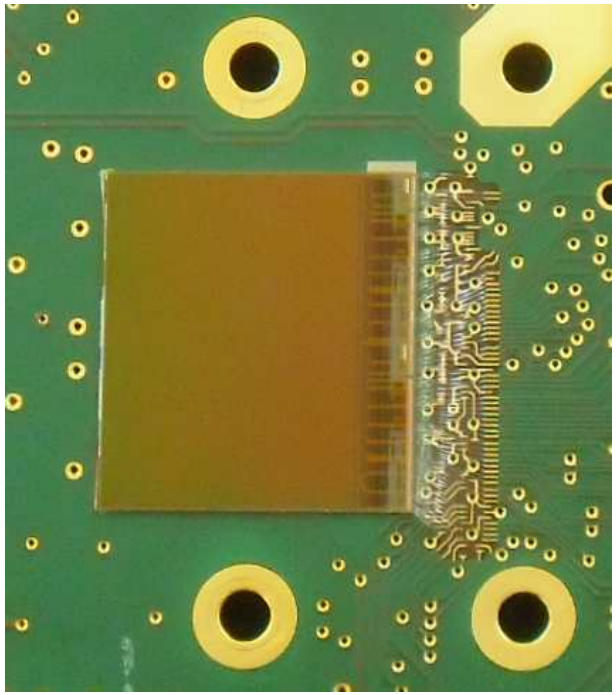
- **1st step : Separate validation of each element composing signal sensing & processing chain :**
  - Pixel array with 1-row read-out (1 discri./column)
  - Pixel array with 2-row read-out (2 discri./column)
  - Zero suppression circuitry with output buffers

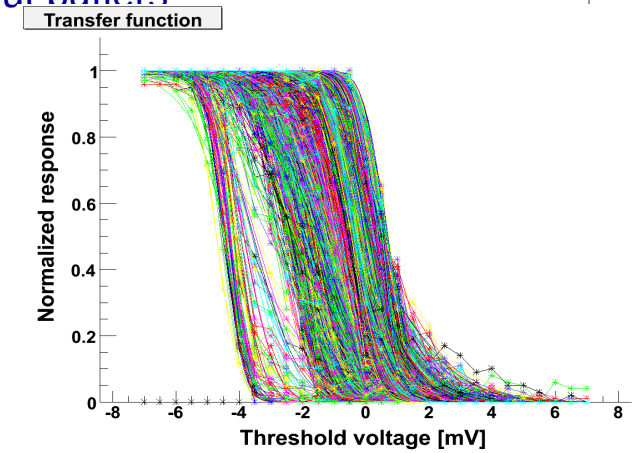
⟼

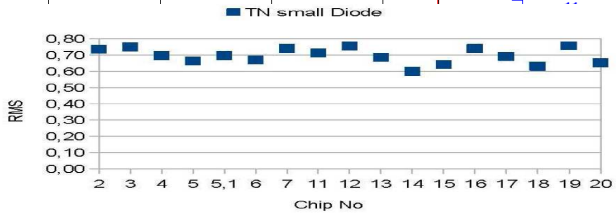


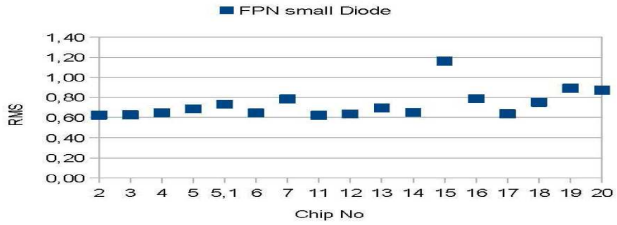
- **2nd step : FSBB-M**

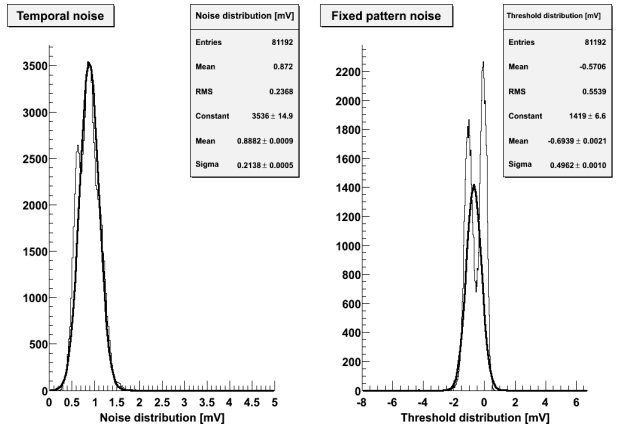
  ≅ **1/3 of MISTRAL :**









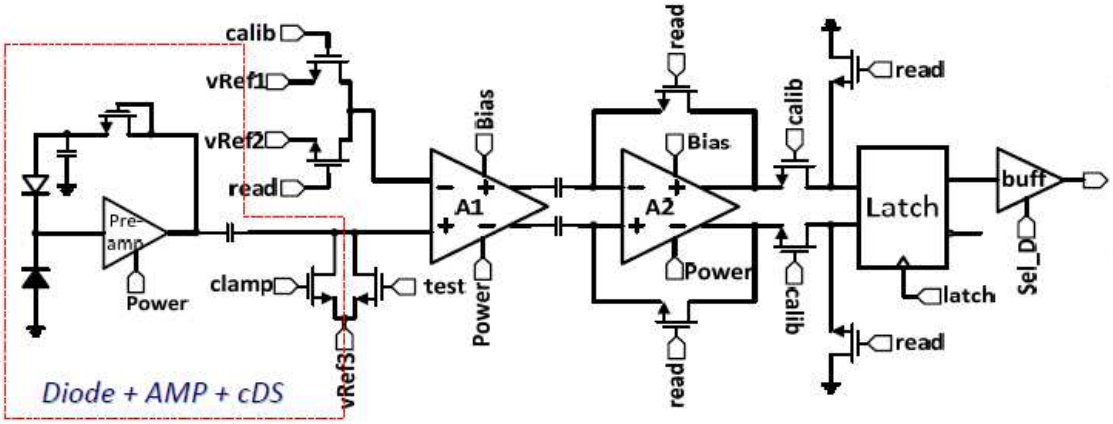


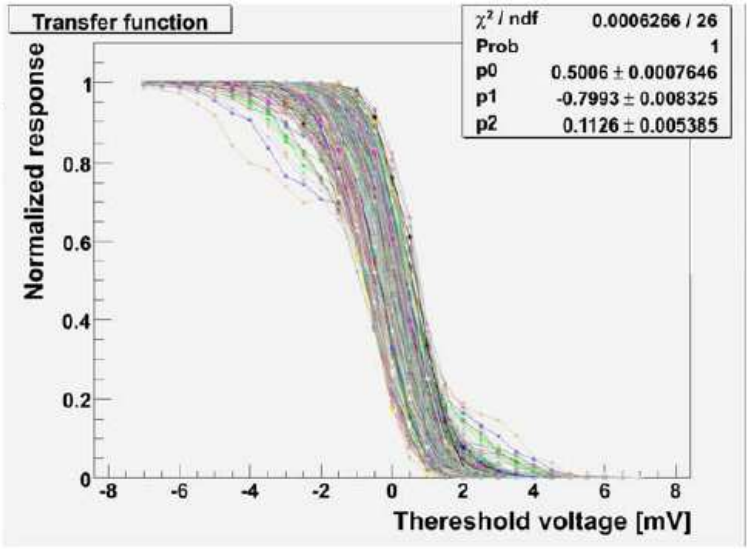
TN ≃ 0.87 mV FPN ≃ 0.55 mV

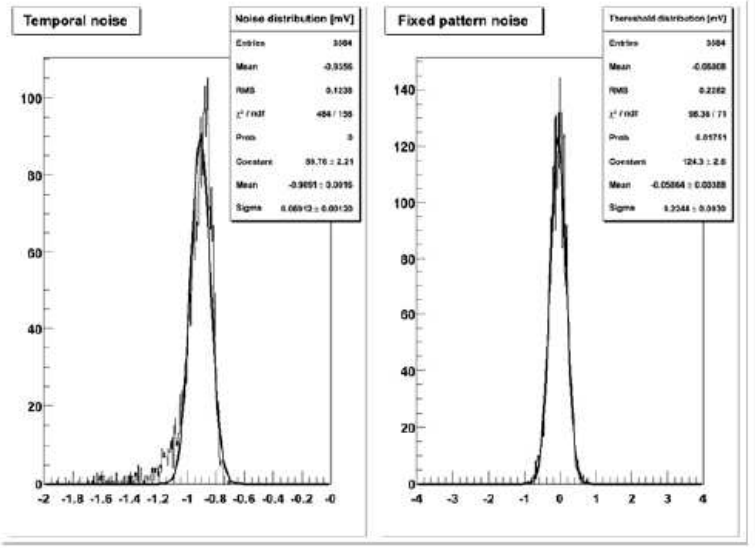
(total noise ≃ 15-20 e⁻ ENC)

threshold		fake rate
4 mV	11870	1.4 10e-5
5 mV	3584	4.35 10e-6
6 mV	1092	1.32 10e-6
7 mV	406	4.96 10e-7
8 mV	236	2.86 10e-7

Synchronous Read-Out Architecture : In-Pixel Discrimination



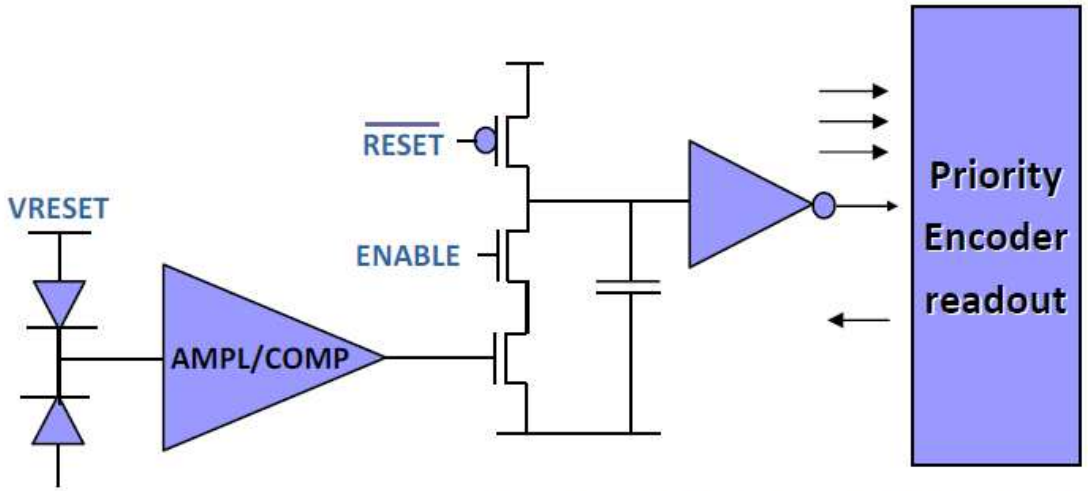




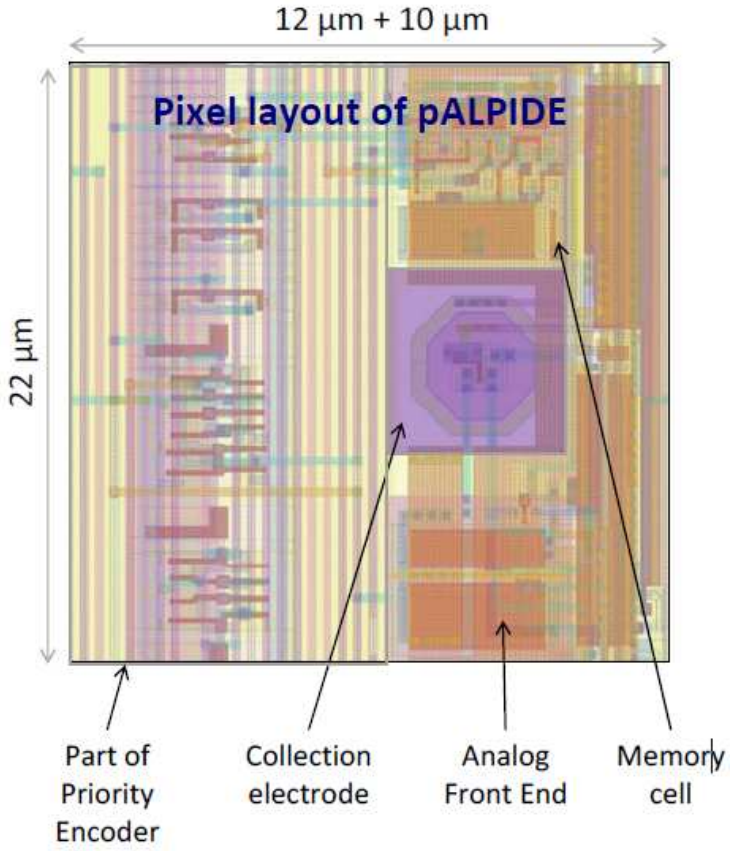
- *To provide adequate performance within small pixel*
  - *Structure selection: speed & power & offset mitigation vs area*
    - *Differential structure: preferable in mixed signal design*
    - *Two auto-zero amplifying stages + dynamic latch*
      - ✓ *OOS (Out Offset Storage) for the first stage and IOS (Input Offset Storage) for the second*
    - *Gain and power optimized amplifier*
  - *Very careful layout design to mitigate cross coupling effects*
  - *Conversion time: 100 ns; current: ~14 µA/discriminator*
- *Test results of in-pixel discriminator:*
  - *Discriminators alone: TN ~ 0.29 mV, FPN ~ 0.19 mV*
  - *Discriminators + FEE: TN ~ 0.94 mV, FPN ~ 0.23 mV*

Asynchronous Read-Out Architecture : ALPIDE (Alice PIxel DEtector)

- *Design concept similar to hybrid pixel readout architecture thanks to availability of Tower CIS quadruple well process: both N & P MOS can be used in a pixel*
- *Each pixel features a continuously power active:*
  - *Low power consumption analogue front end (Power < 50 nW/pixel) based on a single stage amplifier with shaping / current comparator*
    - *High gain ~100*
    - *Shaping time few µs*
  - *Dynamic Memory Cell, ~80 fF storage capacitor which is discharged by an NMOS controlled by the Front-End*
- *Data driven readout of the pixel matrix, only zero-suppressed data are transferred to the periphery*

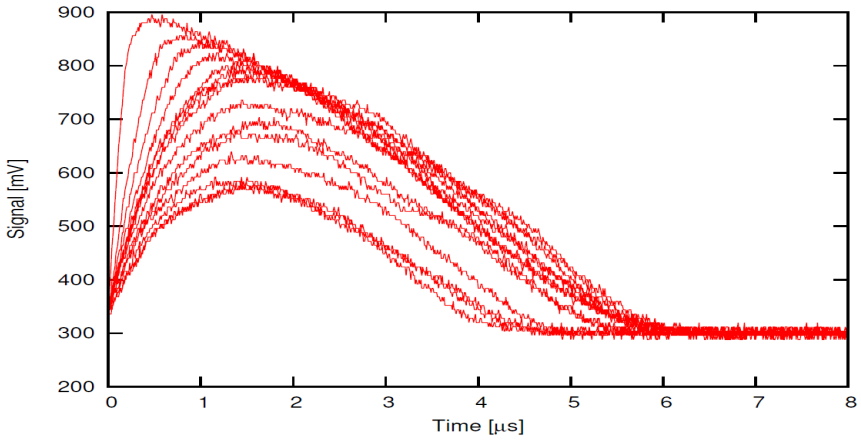


Courtesy of W. Snoeys / TWEPP-2013

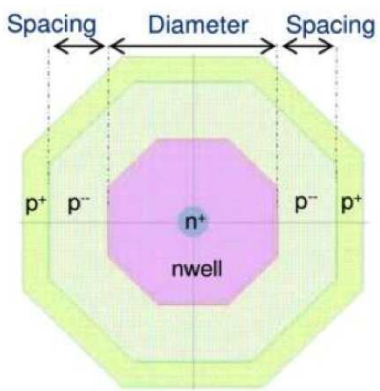


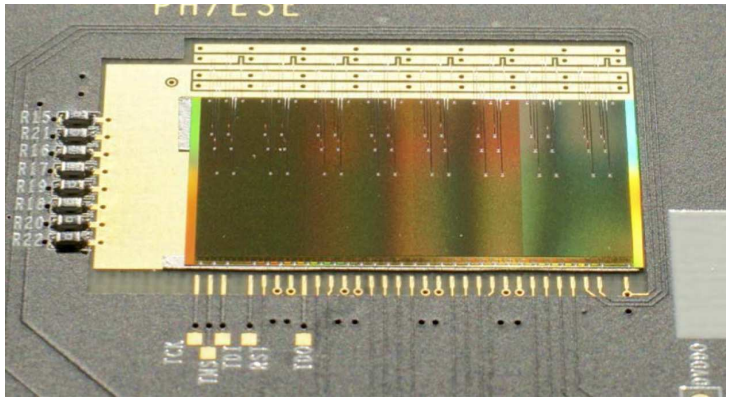
ALPIDE Architecture Validation

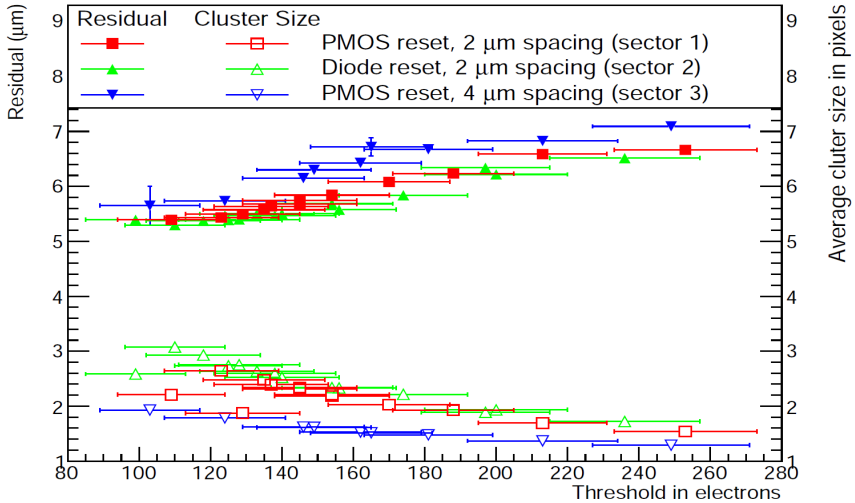
- **1st step : pALPIDE to validate fast pixel read-out**
  - pALPIDE : 64 columns of 512 pixels (22 $\mu m \times 22\ \mu m$)
  - Analog output of one pixel tested with ^{55}Fe source
    ↪ expected time resolution confirmed

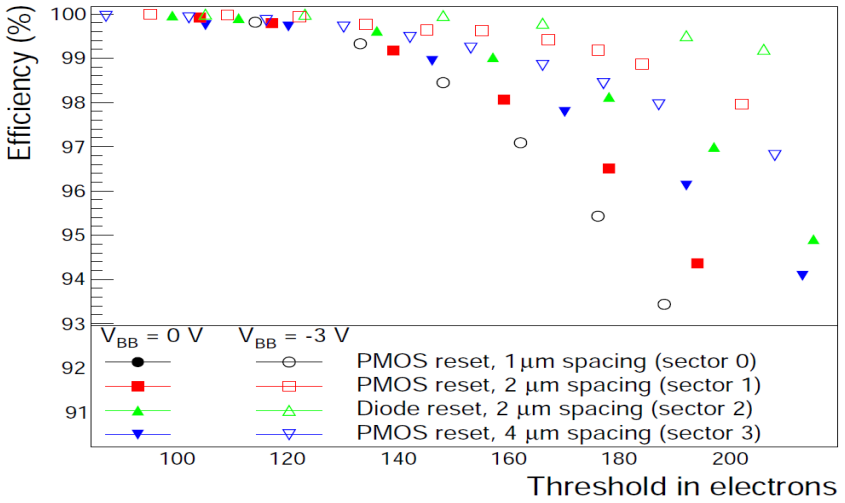


- **2nd step : Full scale ALPIDE**
  - Final sensor dimensions : 15 mm $\times$ 30 mm
  - About 0.5 M pixels of 28 $\mu m \times 28\ \mu m$
  - 4 different sensing node geometries
  - Possibility of reverse biasing the substrate









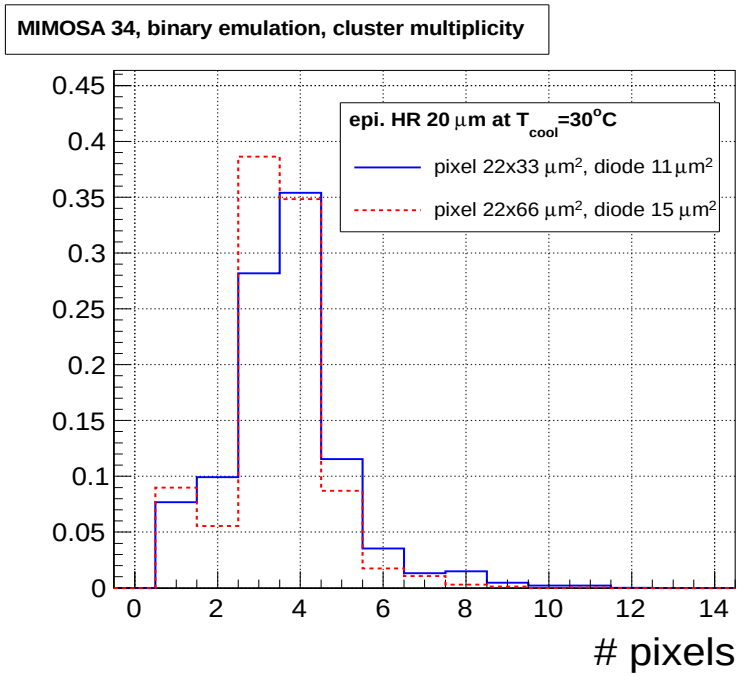
Comments on ILD Vertex Detector Requirements

- **Expected N(hits)/cm^2/BX at 500 GeV & 1 TeV with anti-DID, for each ILD-VXD layer (DBD) :**

Layer	1	2	3	4	5	6
0.5 TeV	6.3±1.8	4.0±1.2	0.25±0.11	0.21±0.09	0.05±0.03	0.04±0.03
1 TeV	11.8±1.0	7.5±0.7	0.43±0.13	0.36±0.11	0.09±0.04	0.08±0.04

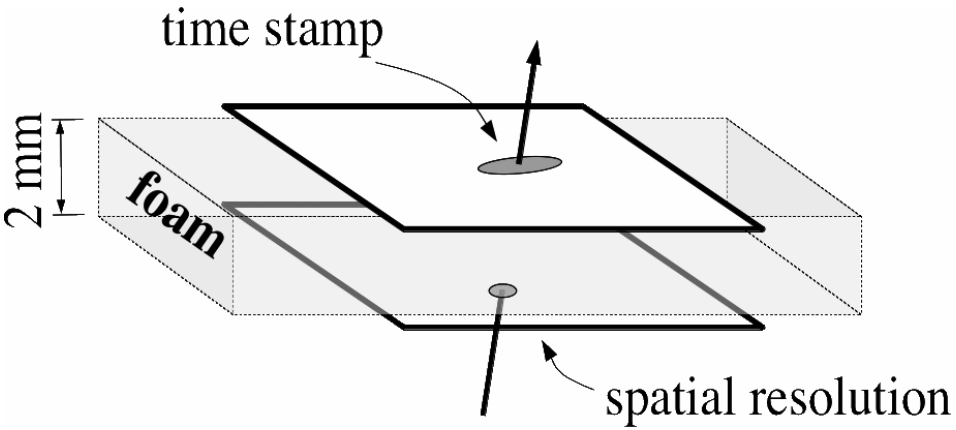
- **Occupancy in L1 and L2 :**
  - L1 : 17 μm ×17 μm pixels (cluster mult. $\simeq$ 5)
    Pixel occ. at 500 GeV $\simeq 10^{-4}$/BX $\Rightarrow$ 10^{-2}/50 μs
  - L2 : 17 μm ×102 μm pixels (cluster mult. $\simeq$ 3)
    Pixel occ. at 500 GeV $\simeq 2\times10^{-4}$/BX $\Rightarrow$ 10^{-3}/2.5 μs
  - 1 TeV : twice higher occupancy
  - Luminosity upgrade : 4 times higher occupancy
  - Large uncertainties (MC stat., anti-DID uncertainty, etc.)

$\Rightarrow$ **Safety margins required on param. governing occupancy**



Upcoming Sensors (Partly) Based on the ALICE Development

- **Spin-off of MISTRAL :**
  - best suited to reach $\lesssim$ 2.8 μm resolution in L1 **BUT** pixels of 17 $\mu m \times$ 17 $\mu m \Rrightarrow$ $\lesssim$ 60 μs r.o. time
  - alternative with 2-row read-out : pixels of 20 $\mu m \times$ 14 $\mu m \Rrightarrow$ $\lesssim$ 40 μs r.o. time
- **Spin-offs of ASTRAL :**
  - L2 : pixels of 17 $\mu m \times$ 102 $\mu m \Rrightarrow$ $\sim$ 7 $\mu m \oplus$ 2.5 μs
  - L1 & L2 : pixels of 22 $\mu m \times$ 33 $\mu m \Rrightarrow$ 5 $\mu m \oplus$ 8 μs
    $\hookrightarrow$ mini-vectors $\cong$ 3.5 $\mu m \oplus$ 4-8 μs
  - L3-L6 : pixels of $\lesssim$ 22 $\mu m \times$ 33 $\mu m \Rrightarrow$ 4-5 $\mu m \oplus$ 30 μs



- **Spin-offs of ALPIDE :**
  - L2 : pixels of 25 $\mu m \times$ 25 $\mu m \Rrightarrow$ 5 $\mu m \oplus <$ 5 μs
  - L2 : pixels of 15 $\mu m \times$ 125 $\mu m \Rrightarrow$ 8 $\mu m \oplus <$ 1 μs reachable ?
- **Spin-offs of MIMOSA-31, MISTRAL & MIMADC :**
  - L3-L6 : pixels of 35 $\mu m \times$ 35 $\mu m \Rrightarrow$ 4 $\mu m \oplus$ 60 μs
  - L1-L2 : pixels of 25 $\mu m \times$ 25 $\mu m \Rrightarrow$ 3 $\mu m \oplus$ 20 μs or 25 $\mu m \times$ 35 $\mu m \Rrightarrow$ 3.5 $\mu m \oplus$ 15 μs ???
- **MIMOSA-33 :** Fine Pixels of 4 $\mu m \times$ 4 μm with delayed (analogue) read-out

SUMMARY

- **CPS are validated for vertex detectors :** STAR-PXL physics run of Spring '14

  $\hookrightarrow$ architectures developed in 0.35 μm CMOS process comply with ILD-DBD requirements

  BUT are far from the real potential of CPS

- **Faster read-out would alleviate vulnerability to unknowns**

  associated to beam related background and track reconstruction performance

  $\hookrightarrow$ main motivation for further R&D, with **single bunch tagging** as ultimate (realistic ?) goal

- **ALICE-ITS $\equiv$ new driving application of CPS, based on a better suited (180 nm) process**
  - MISTRAL $\cong$ MIMOSA-28 with twice faster read-out : validated at real scale
  - ASTRAL $\equiv$ MISTRAL with in-pixel discri. $\Rightarrow$ twice faster : validated at small proto. scale
  - ALPIDE (CERN) : asynchronous read-out (few μs r.o. time) : 1st full scale proto. test results satisfactory

  $\Rightarrow$ $\geq$ **2-4 times faster read-out w.r.t. 0.35 μm techno., with up to 60 % power reduction**

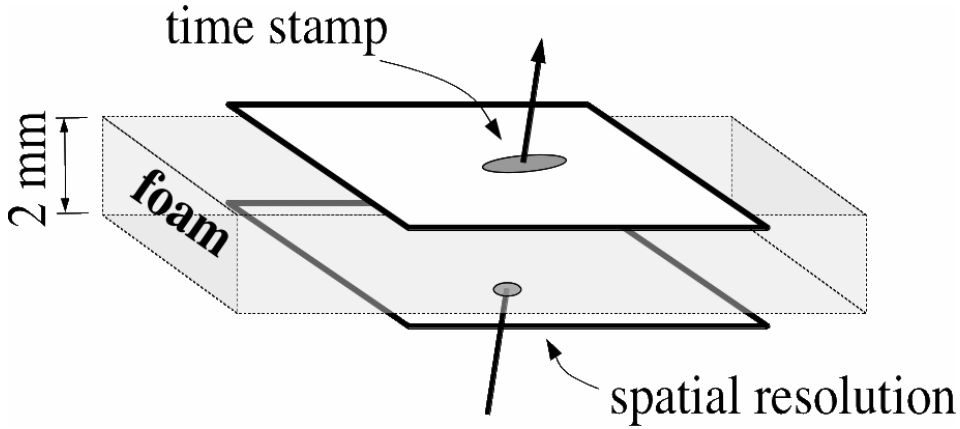
- **Next steps :**
  - finalise ALICE-ITS sensor prototyping in 2015
  - start deriving CPS for VXD in 2016/17 $\mapsto$ baseline $\triangleright$

Layer	σ_{sp}	t_{int}
ILD-VXD/In	$<$ 3/5 μm	30-40/8 μs
ILD-VXD/Out	$\sim$ 3.5/4 μm	80/120 μs

- **Topics not addressed here:** alternative CPS designs, CPS for trackers, PLUME devts, etc.

ILD - VXD Concept Addressed

- **Two types of CMOS Pixel Sensors :**
  - **Inner layers :** Priority to read-out speed & spatial resolution
  - **Outer layers :** Priority to power consumption and good resolution
- **Inner layers : $\sim$ 300 cm^2**
  - L1 : small pixels with end-of-column
    binary charge encoding $\mapsto$ $\lesssim 3\ \mu m$
    - $20\times14\ \mu m^2$ with 2-row read-out : $\lesssim 40\ \mu s$
    - $17\times17\ \mu m^2$ with 1-row read-out : $60\ \mu s$
      $\hookrightarrow$ 2-row read-out : $30\ \mu s$ (tbc)



  - L2 : elongated pixels with in-pixel binary charge encoding $\mapsto$ $\sim 5\ \mu m$
    - $22\times33\ \mu m^2$ with 2-row read-out : $\sim 8\ \mu s$
    - $22\times33\ \mu m^2$ with 4-row (tbc) read-out : $\sim 4\ \mu s$
- **Outer layers : $\sim$ 3000 cm^2**
  - L3-6 : large pixels with end-of-col 3-4 bit ADCs
    - $35\times35\ \mu m^2$ pixels : $\lesssim 4\ \mu m$ & $120\ \mu s$
    - $25\times50\ \mu m^2$ pixels : $\lesssim 4\ \mu m$ & $80\ \mu s$