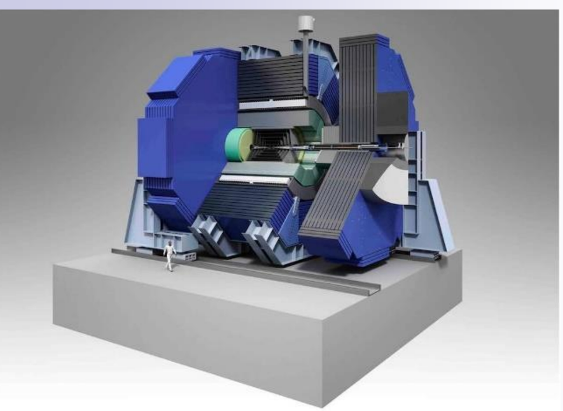
LCWS 2014

Belgrade, Serbia

October 6-10, 2014

The SiD Detector Concept: Status and Plans



Bruce A. Schumm

Santa Cruz Institute for Particle Physics

University of California, Santa Cruz

for the SiD Consortium

Outline

- The SiD organization
- Physics drivers & detector concept
- SiD subsystem status
- Areas of need
- Keeping in touch; next meetings

The SiD Organization

SiD-Ogenesis

Design Concept era: informal association of interested individuals

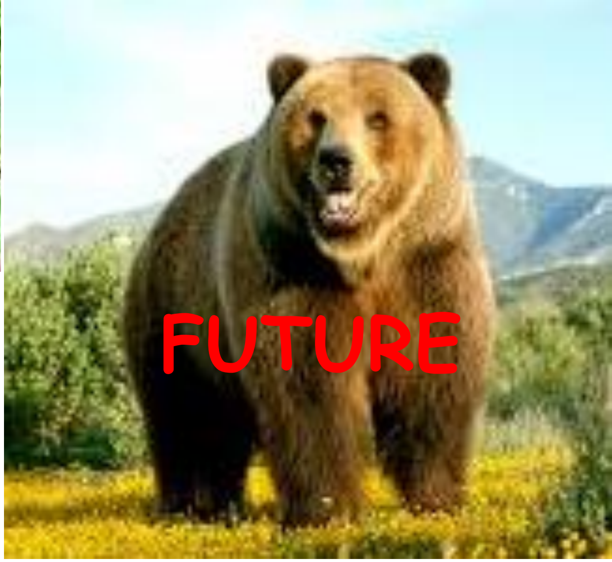
R&D funded by varying means

As of 22-Sept-2014

Inauguration of SiD Consortium

The SiD remains open and non-exclusive

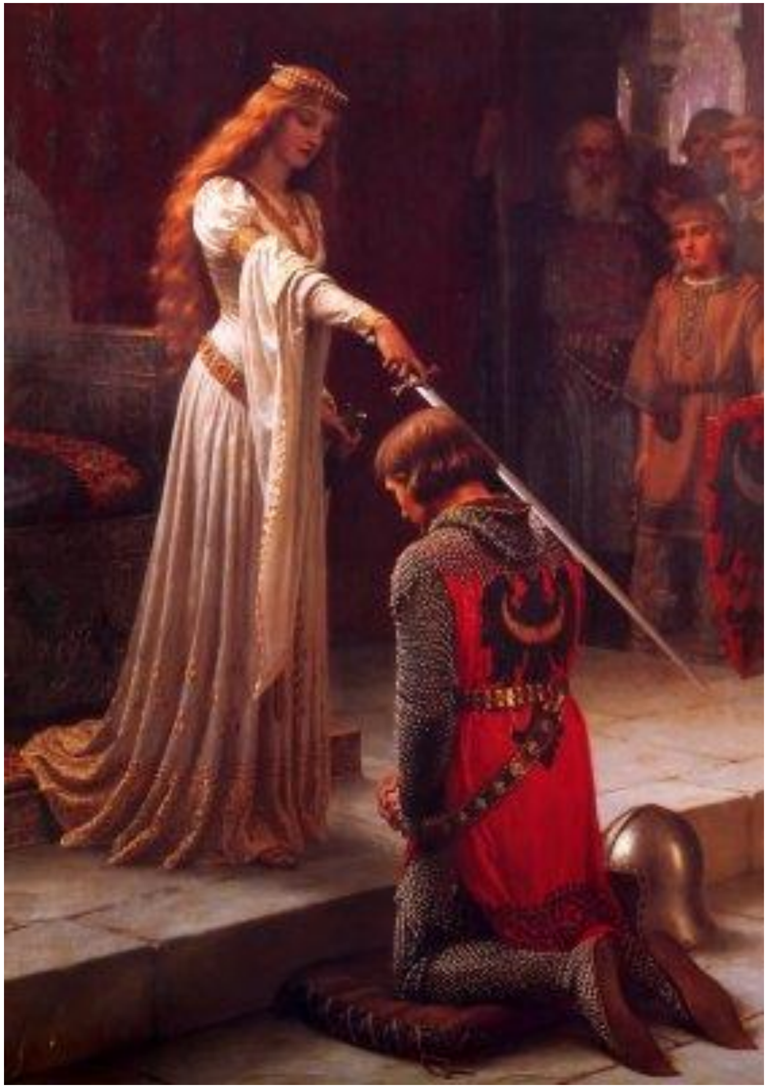
Full Collaboration status awaits formal approval and funding of ILC project



1st SiD Consortium Meeting

The 1st meeting of the nascent SiD Consortium took place by WebEx on 22 September 2014

- Initial bylaws adopted (see consortium website)
- Conscription of Institutional Board Chair
- Philip Burrows (Oxford University)

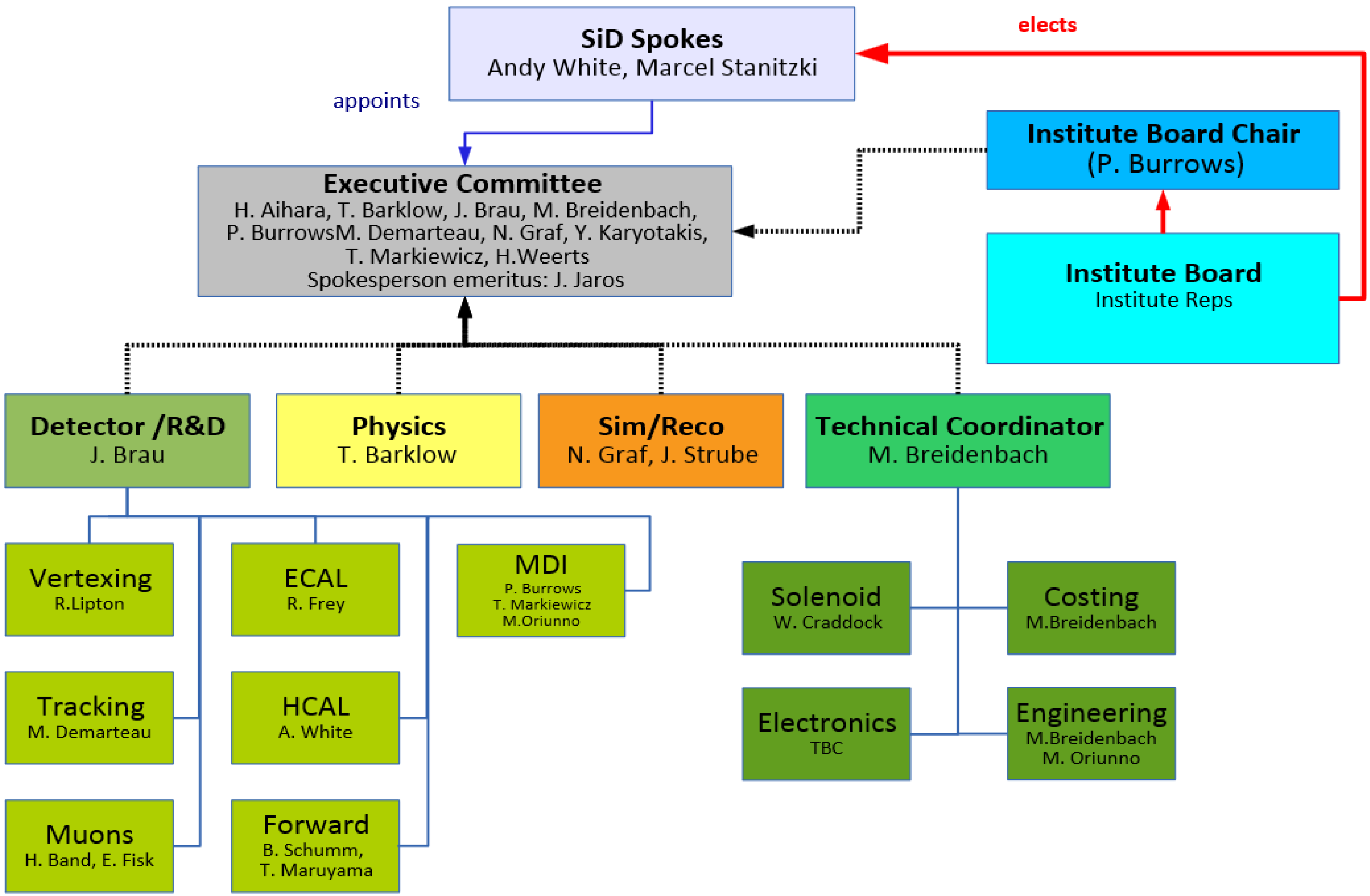


Institutions of the SiD Consortium Board

SiD Consortium currently comprises 21 institutions from all three regions (Asia, Europe, the Americas), most of which attended the inaugural Consortium Board meeting

Argonne National Lab
Bristol University
Cornell University
FNAL
LAPP (Annecy)
Los Alamos National Lab
Manchester University
Open University
Oxford University
Pacific NW National Lab
Queen Mary University
Rutherford Laboratory
SLAC
University of Barcelona
UC Davis
UC Santa Cruz / SCIPP
University of Iowa
University of Oregon
UT Arlington
Tokyo University
Yale University

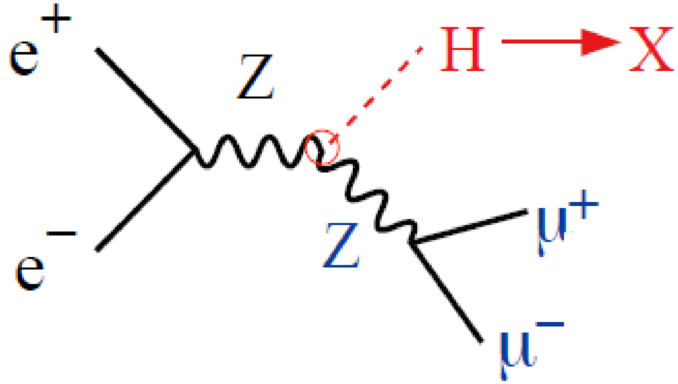
SiD Organigram

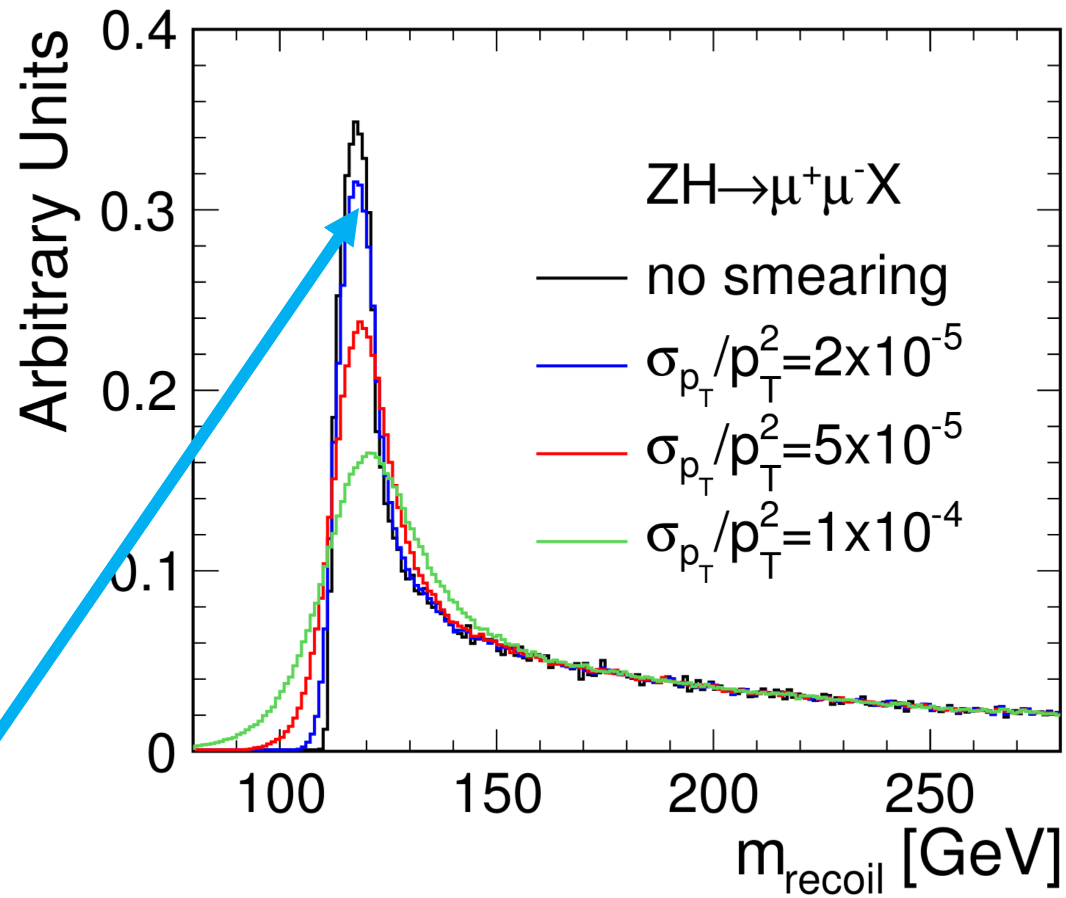


SiD Outreach

- First SiD meeting in Aisa (2-3 September 2014)
- Hosted by Hiro Aihara (U. Tokyo)
- Strong Japanese participation

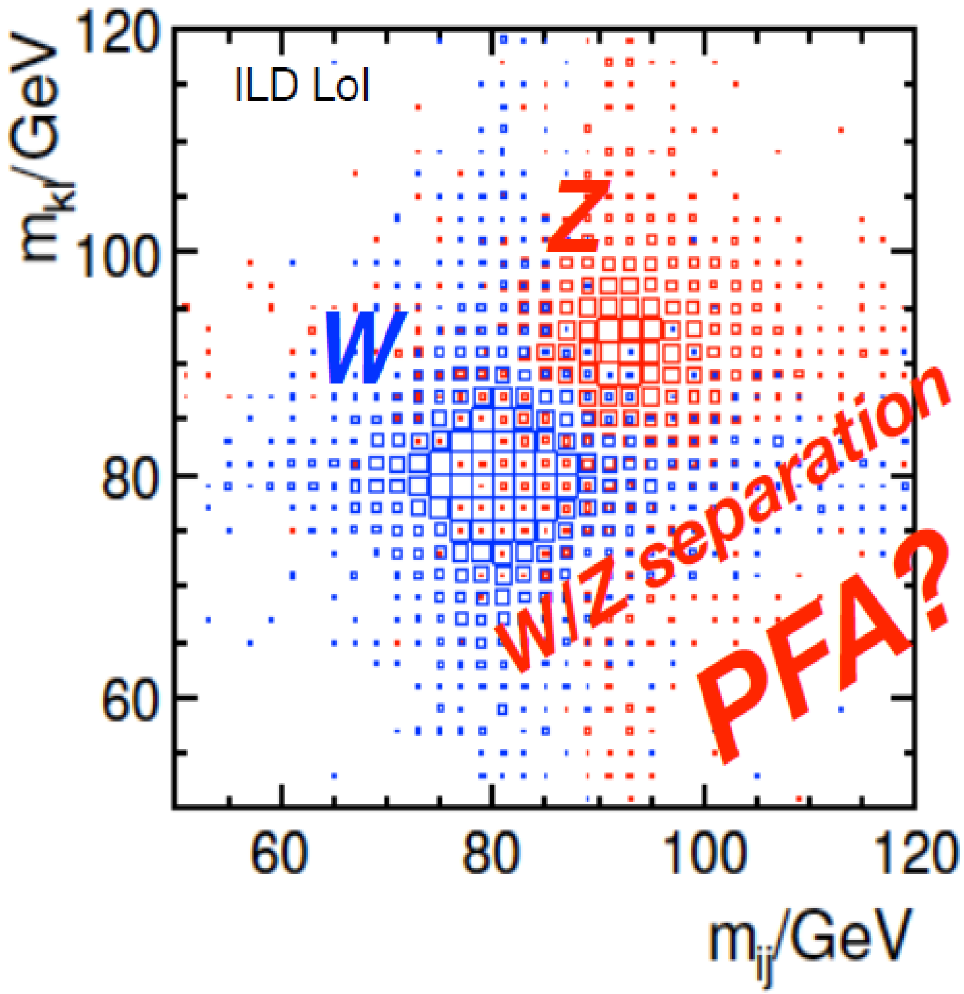
ILC Physics and the SiD Detector Concept



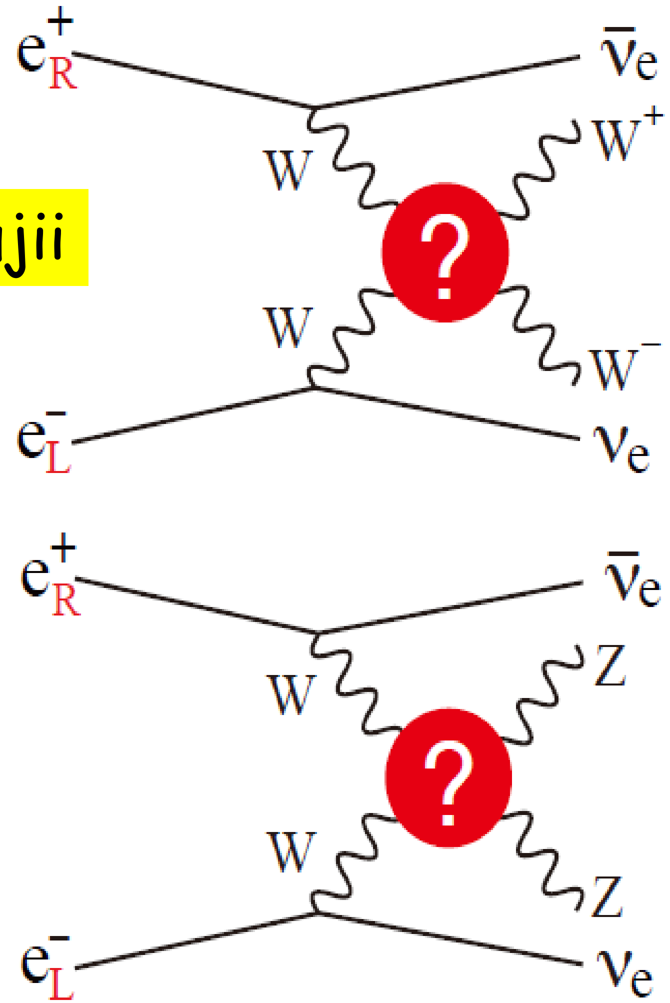


Recoil mass for $\delta p_{\perp}/p_{\perp}^2=2\times10^{-5}$

Physics Drivers II



K. Fujii



Silicon Tracker Primer

For a given track $p_\perp$ and tracker radius R, error on sagitta s determines $p_\perp$ resolution

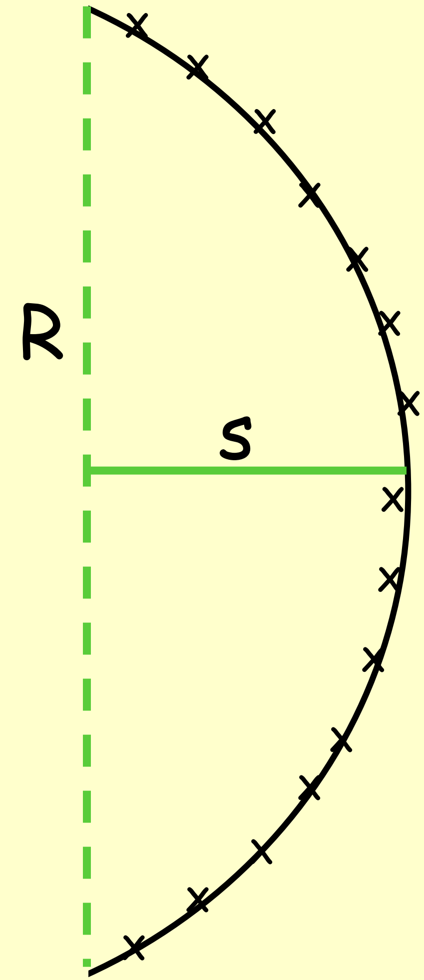


Figure of merit is $\eta = \sigma_{point}/\sqrt{N_{hit}}$.

Gaseous detector: Of order 200 hits at σ_{point}=100 μm ➔ η = 7.1 μm

Solid-state: 5 layers at σ_{point}=5 μm ➔ η = 2.2 μm

Also, Si information very localized, so can better exploit the full radius R.

Solid-state tracking intrinsically more efficient

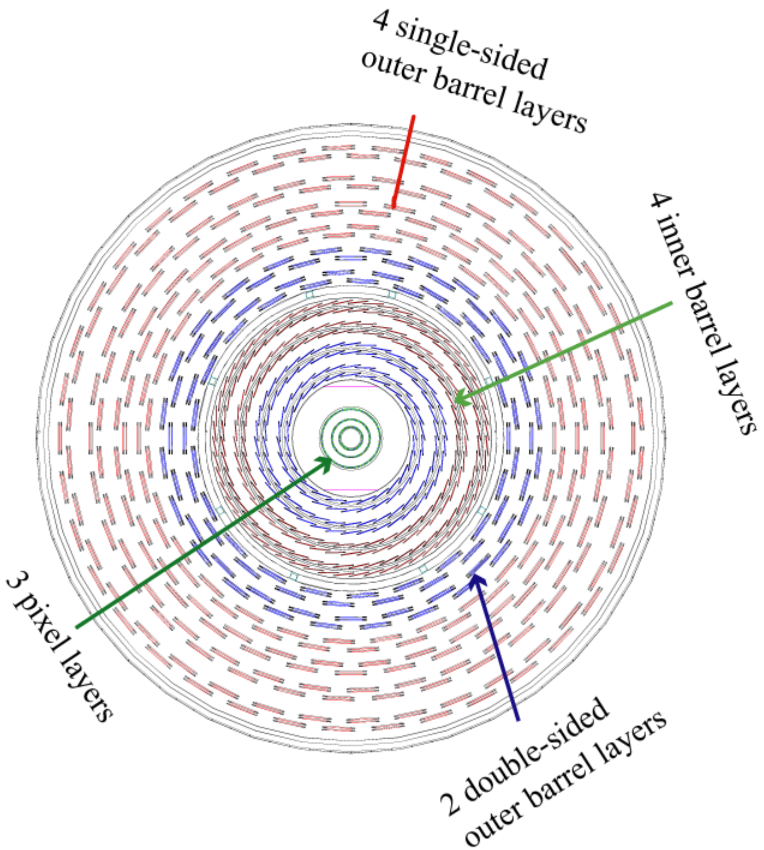
SiD Design Strategy

The SiD Detector design takes advantage of the properties of Si diode sensing to provide a compelling solution for ILC physics

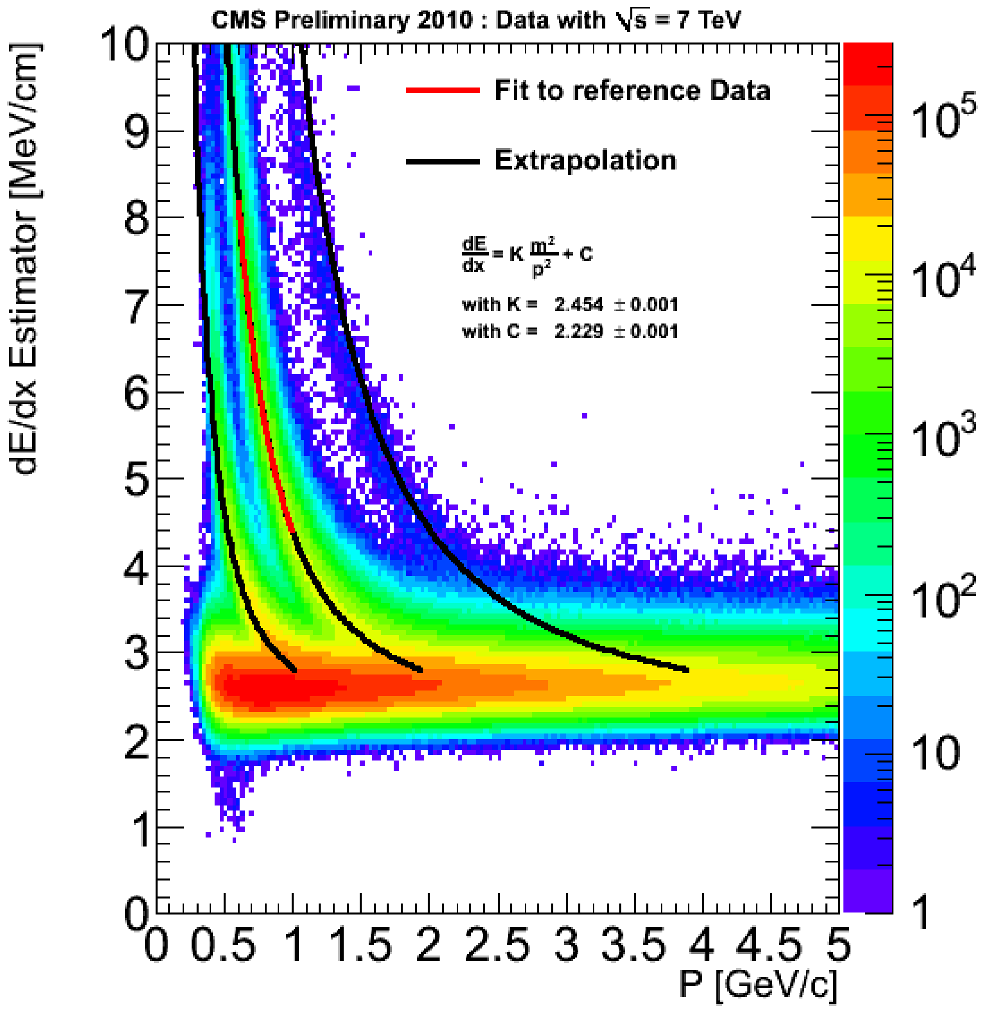
Basic idea: Exploit superior sagitta resolution to reduce tracker radius R, reducing calorimeter volume by $1/R^2$.

Plow savings into precision calorimetry (fine-grained Si/W ECAL) ➔ **Efficient PFA**

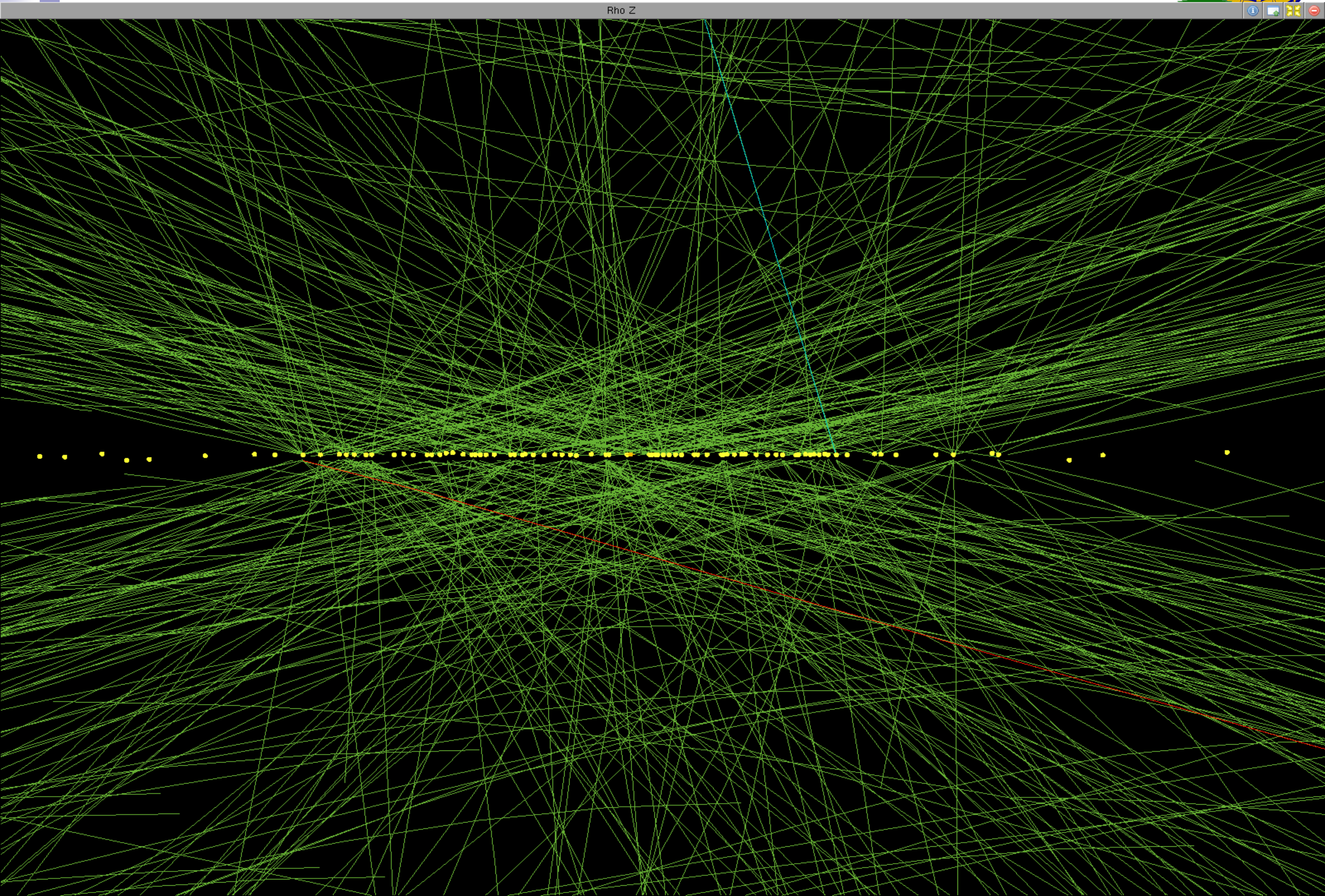
Proof of Principle: The CMS Tracker



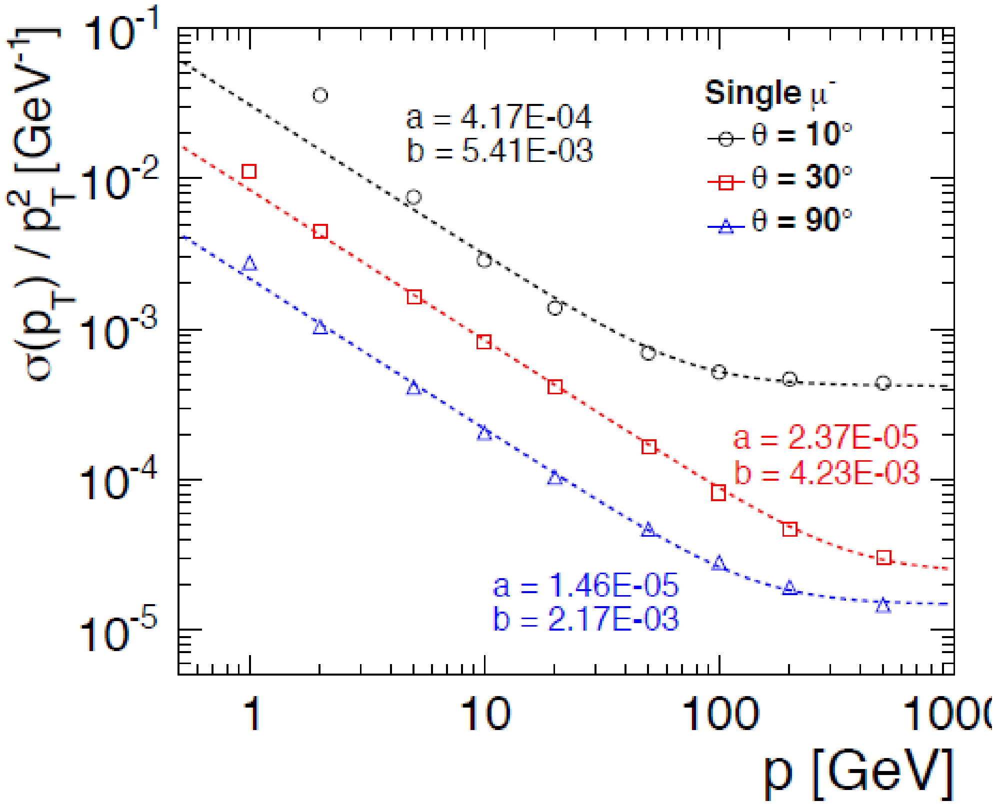
CMS Tracker Layout

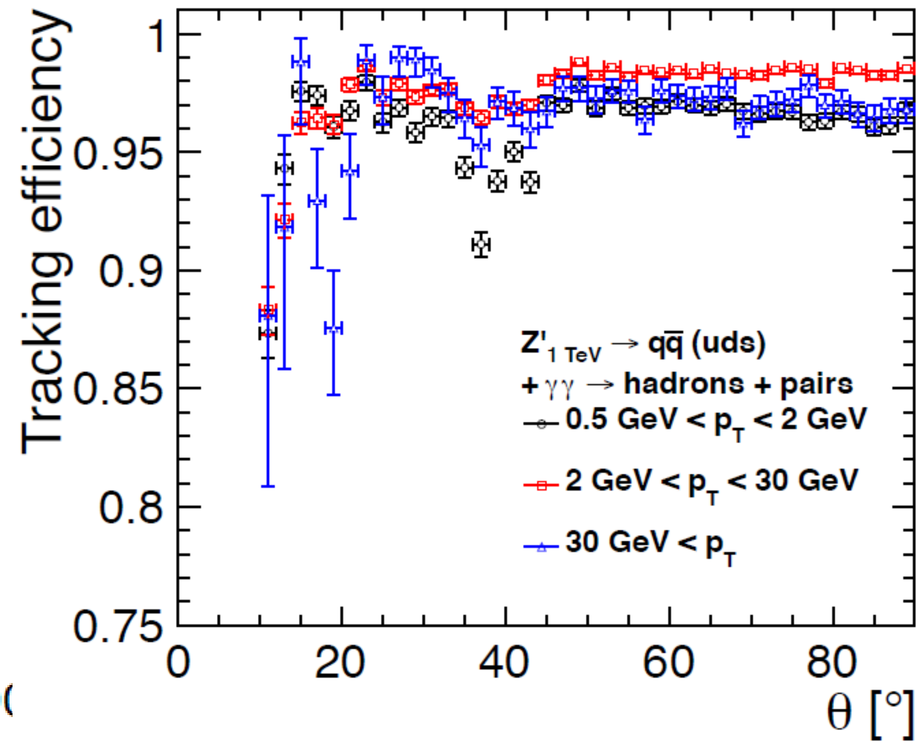


Proof of Principle: CMS Tackles 78 Vertices



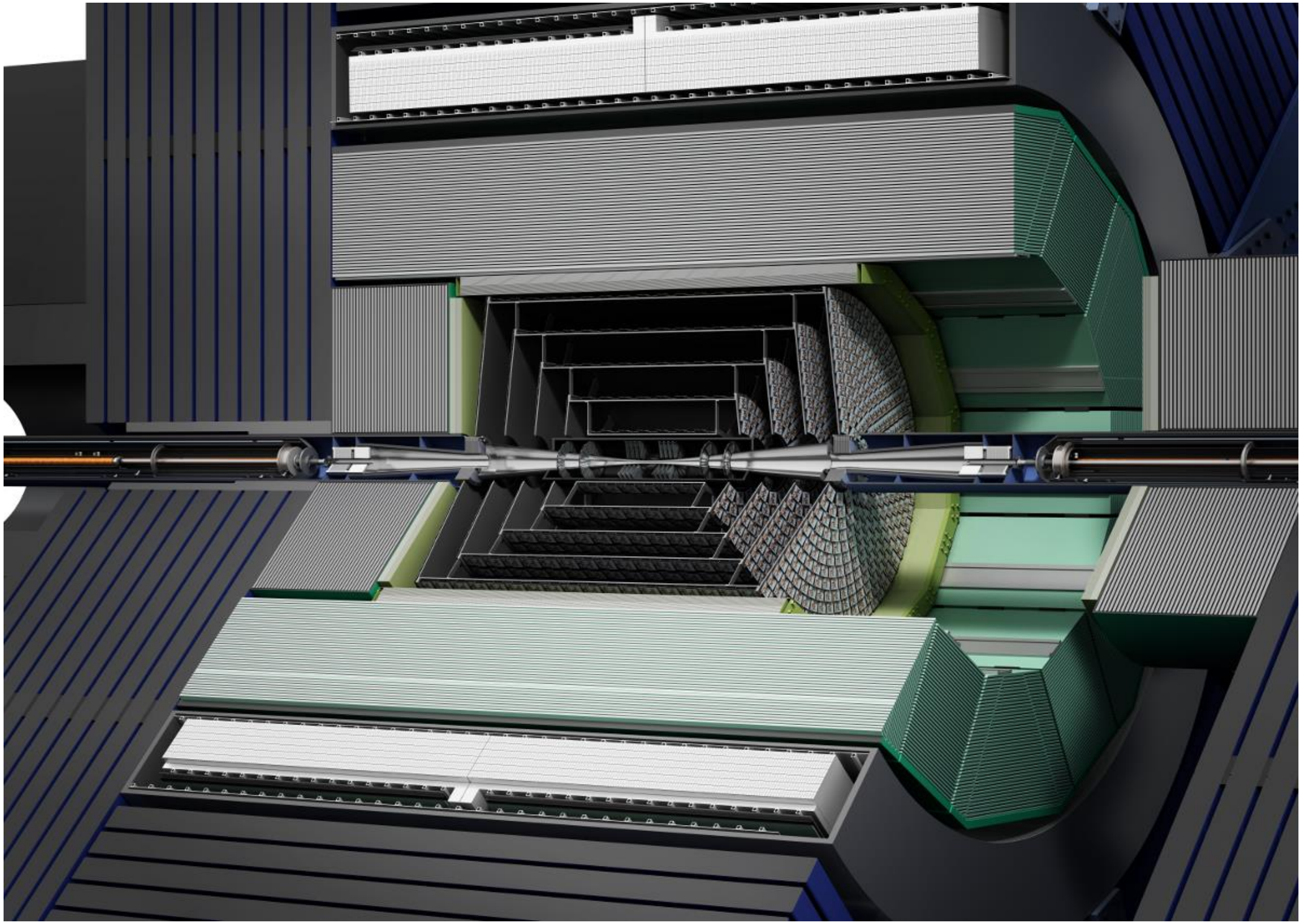
SiD Tracking Simulation





- In challenging environment (1 TeV Z′, including γγ backgrounds)
- Kalman Filter (pattern recognition, fitting) not yet implemented

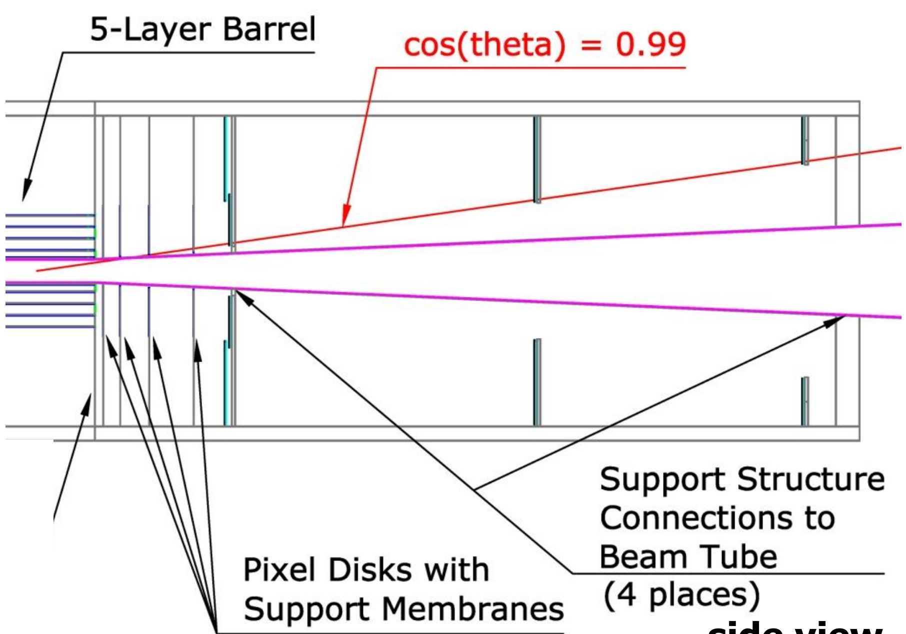
SiD Detector Subsystems



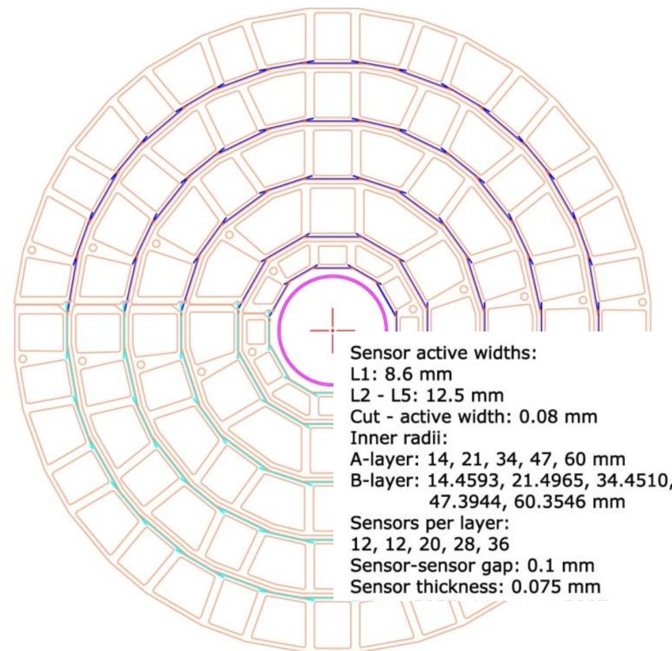
SiD Vertexing

Slide courtesy Marcel Demarteau

- **Baseline vertex detector:**
  - **Central: 5-layer barrel, consisting of two sub-assemblies clam-shelled around beam pipe**
  - **End cap: two 4-plane end disk assemblies and three additional disks per end for extended coverage**
- **All elements are supported indirectly from the beam tube via double-walled, carbon fiber laminate half-cylinder**
- **Material budget 0.1% X_0 per layer, with 20x20 μm^2 pixel size barrel and end; 50x50 μm^2 forward**



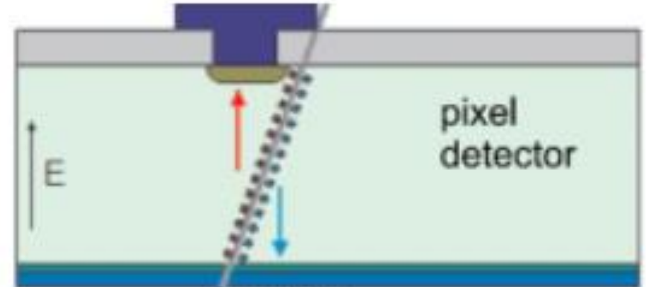
side view



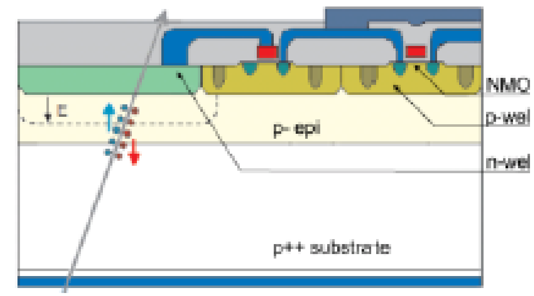
end view

A number of sensor technologies being explored…

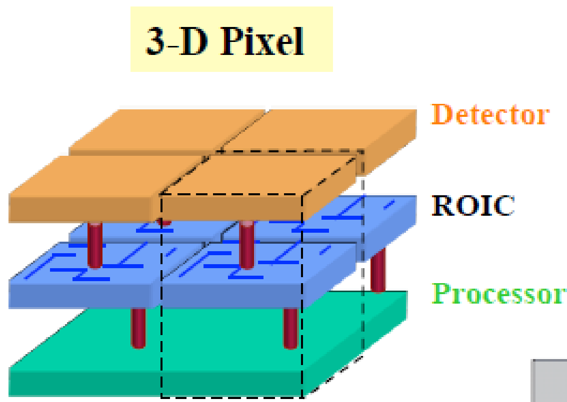
- Si diode pixels ("standard" technology)



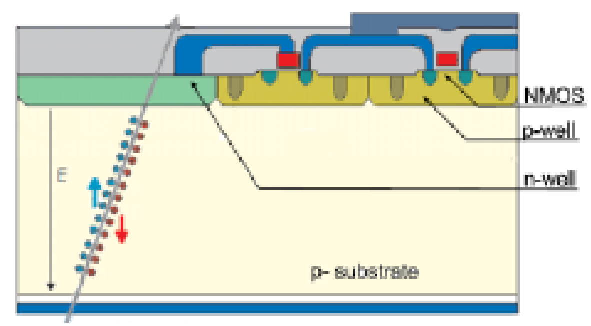
- Monolithic designs (MAPS, Chronopix)



- Vertically Integrated ("3D") Approaches (VIP Chip)

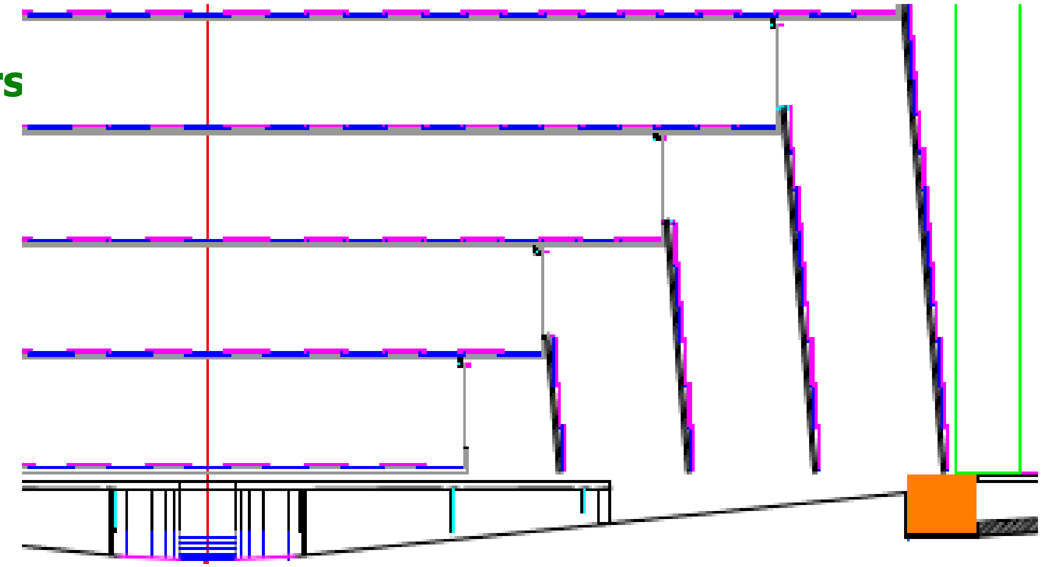


- High Voltage CMOS (snappy timing)



SiD Baseline Tracker

- **Support**
  - **Double-walled CF cylinders**
  - **Allows full azimuthal and longitudinal coverage**
- **Barrels**
  - **Five barrels, measure ϕ only**
  - **10 cm z segmentation**
  - **Barrel lengths increase with radius**
- **Disks**
  - **Four double-disks per end, lampshade geometry**
  - **Measure R and ϕ**
  - **Varying R segmentation**
  - **Disk radii increase with Z**



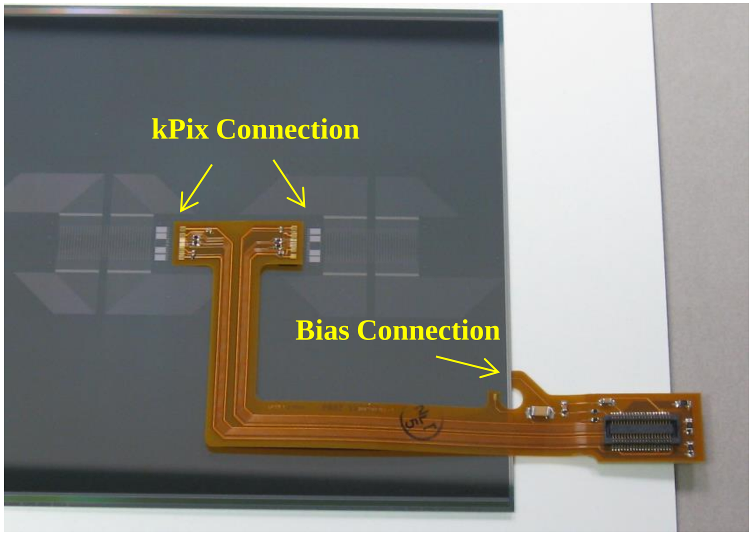
Slide courtesy Marcel Demarteau

- ***Demonstrate the mechanical stability of the lightweight carbon fiber support structures, especially under power pulsing (Lorentz forces) power pulsing to be addressed; are there ways to reduce the material budget?***

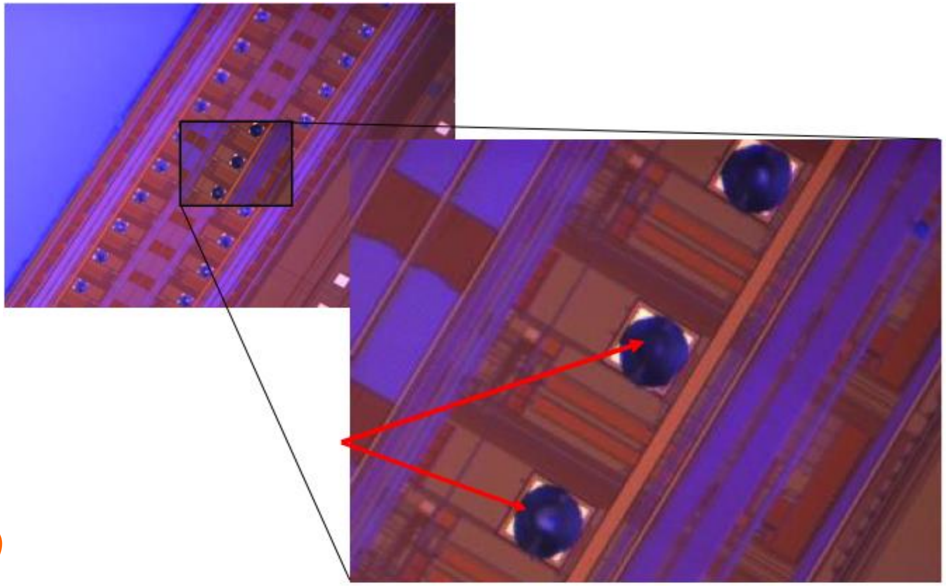
Tracker Sensors

Slide courtesy Marcel Demarteau

- **Silicon Strip modules with hybrid-less design**
  - **Two ASICs directly mounted on a HPK sensor with 2k strips**
  - **Double-metal trace routing**
  - **Power and clock routed over sensor**

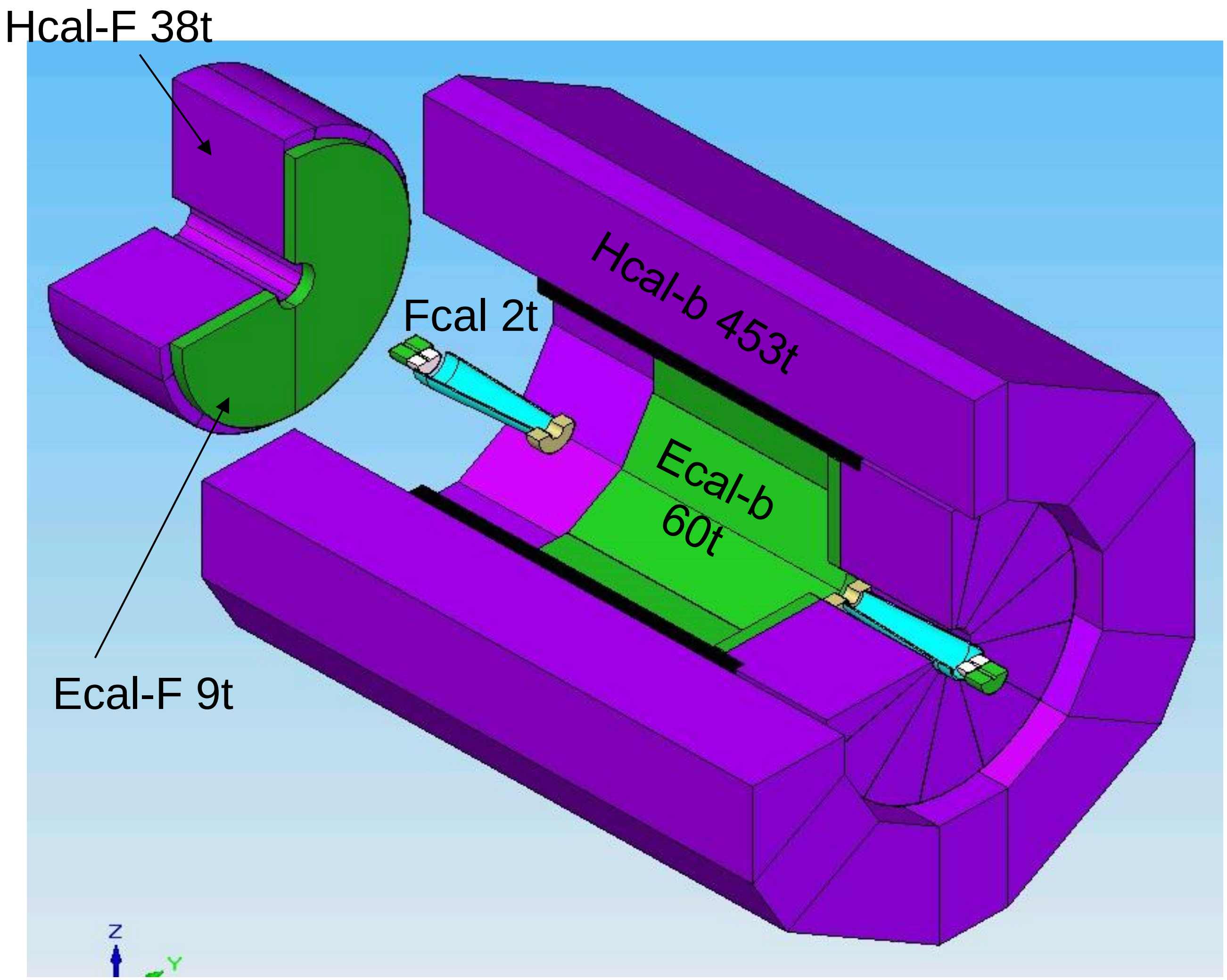


- **All components available:**
  - **kPix: 1k-channel ASIC**
  - **Low-mass cable**
  - **Low-mass ASIC bonding**
    - Gold stud attachment using thermo-compression 300-350 C
    - 160 g/bump ok



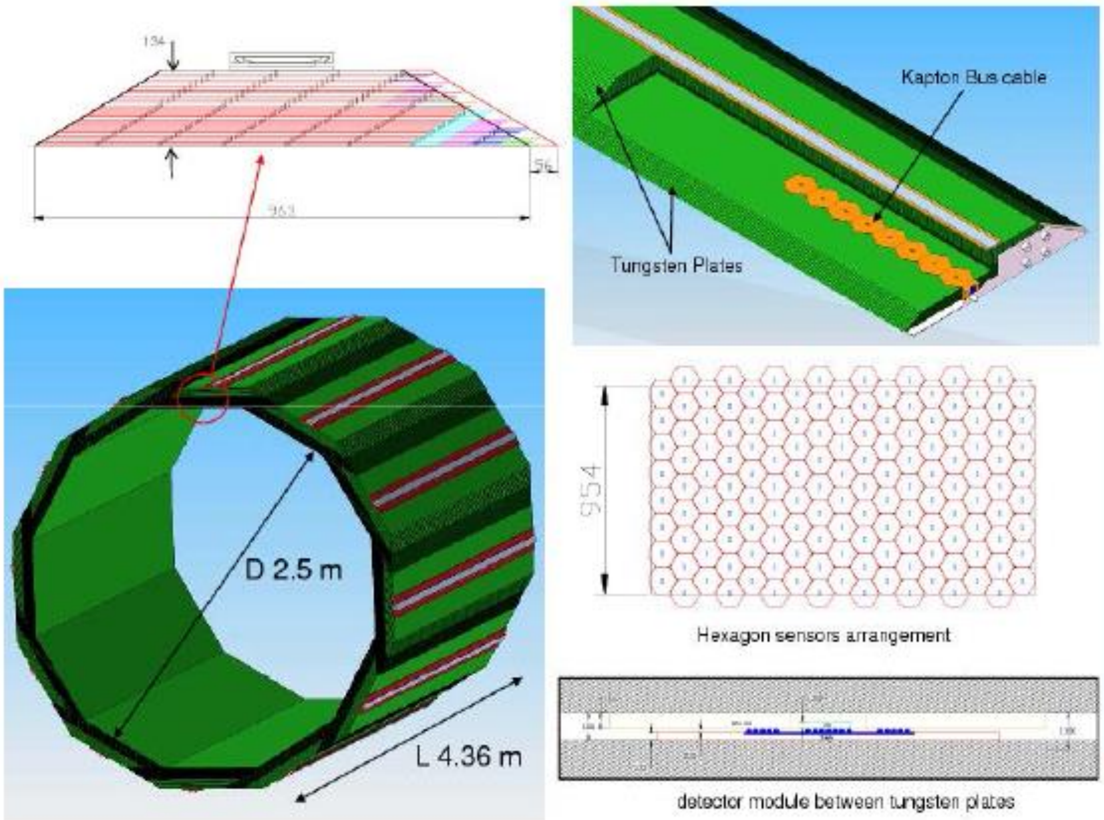
- ***Tests of silicon module:***
  - ***Sensor characterization***
  - ***Readout tests***
  - ***Tests in B-field (Lorentz forces)***

SiD Calorimetry



SiD Electromagnetic Calorimeter

An imaging calorimeter: 30 layers tungsten interleaved with 30 layers pixellated silicon



<u>Baseline configuration:</u>

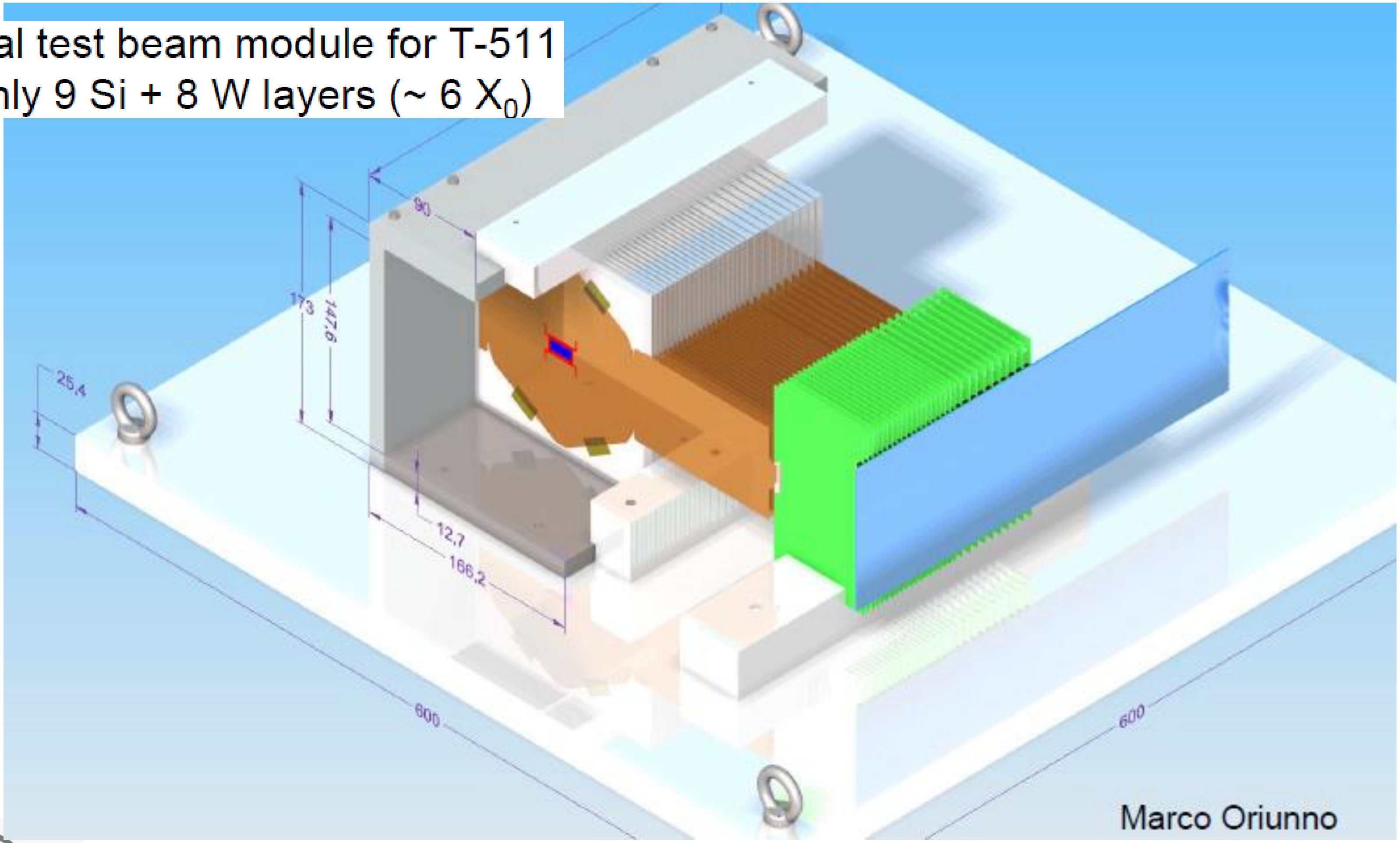
- transverse: 12 mm^2 pixels
- longitudinal: (20 x 5/7 X_0) + (10 x 10/7 X_0) ⇒ 17%/sqrt(E)
- 1 mm readout gaps ⇒ 13 mm effective Moliere radius

- Conceptual design is OK…but should be optimized
- Assembly is very labor intensive – use robot approach?
- Need further mechanical prototyping – W sheets/FEA

SiD Prototype ECAL

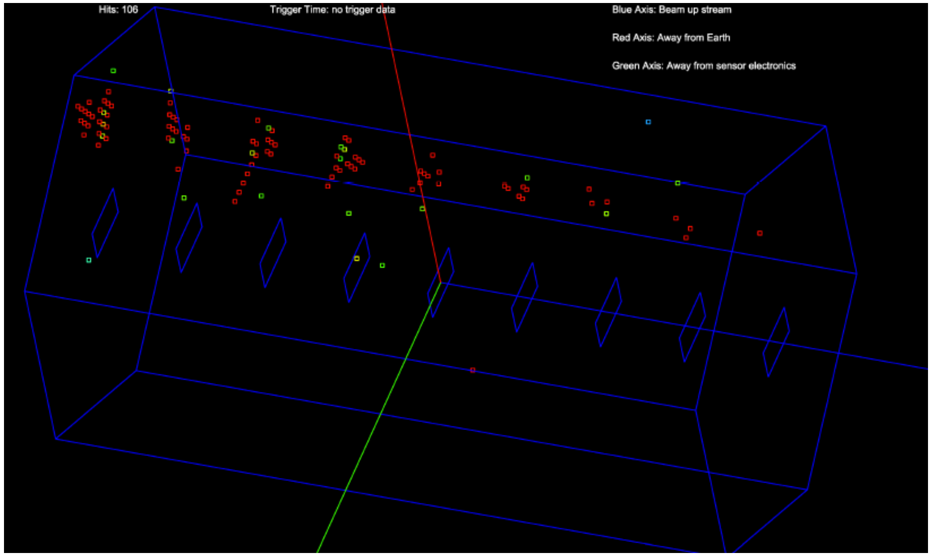
Test beam Ecal prototype design – 30 layers, with SiD longitudinal profile

Initial test beam module for T-511
only 9 Si + 8 W layers (~ 6 X_0)

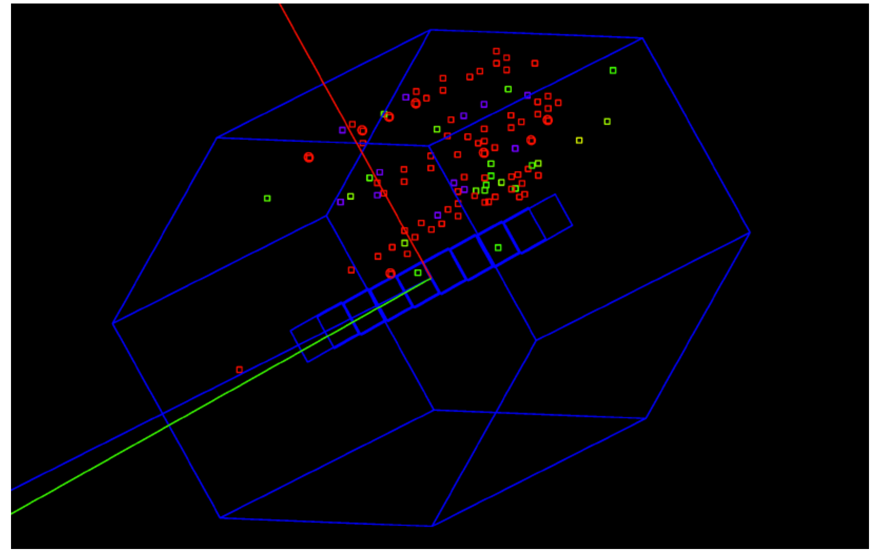


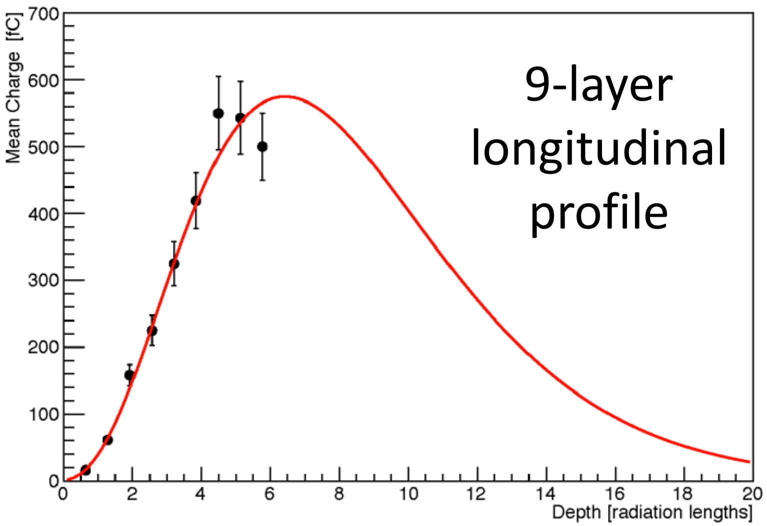
ECAL Testbeam Performance

One electron



Three electrons





Uncovered some unexpected behavior

Unphysical negative-amplitude hits – current hypotheses:

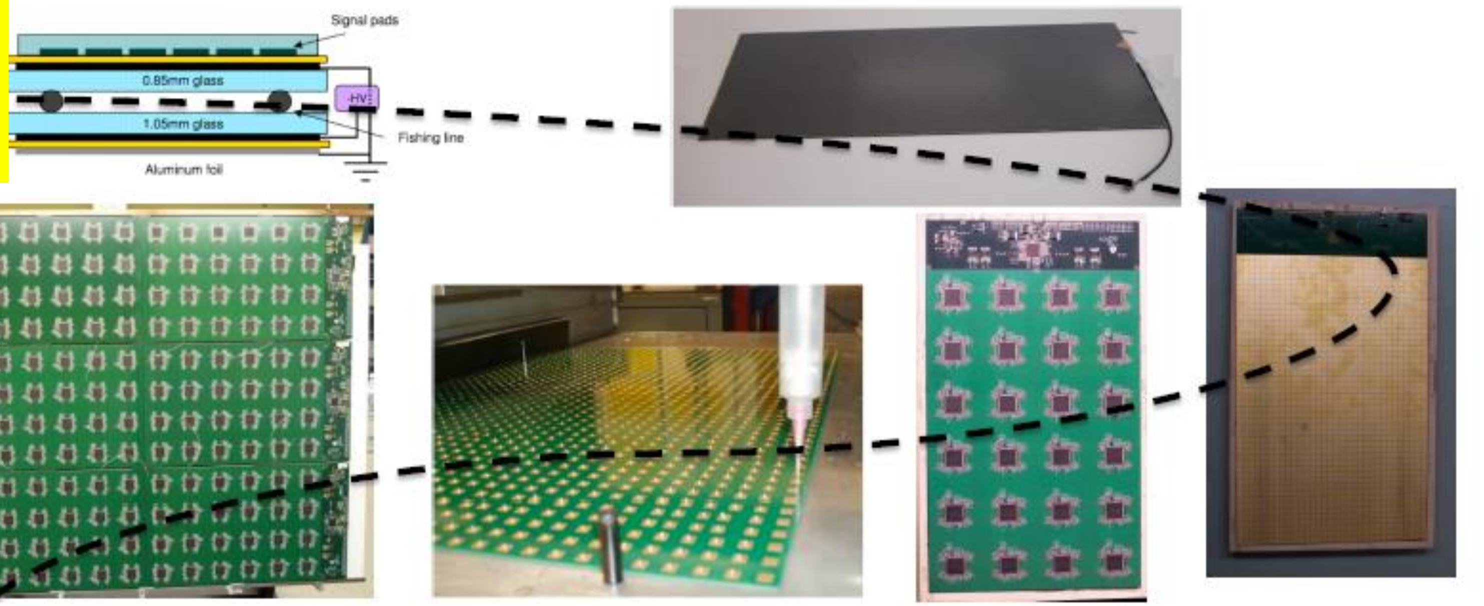
- Small number of in-time hits: cross-talk in sensor and baseline shift of KPiX virtual ground
- Many out of time hits for some layers when many hit pixels: associated with KPiX resets? cascading?

? Second generation sensor – with shielding between traces and pixels?

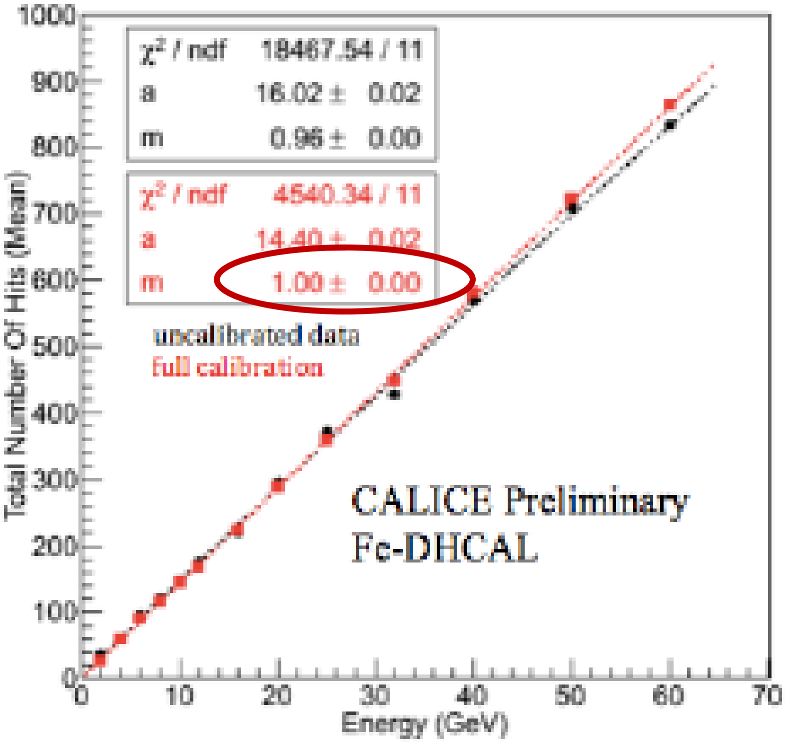
[Slide courtesy A. White]

Digital HCAL Baseline and Prototype

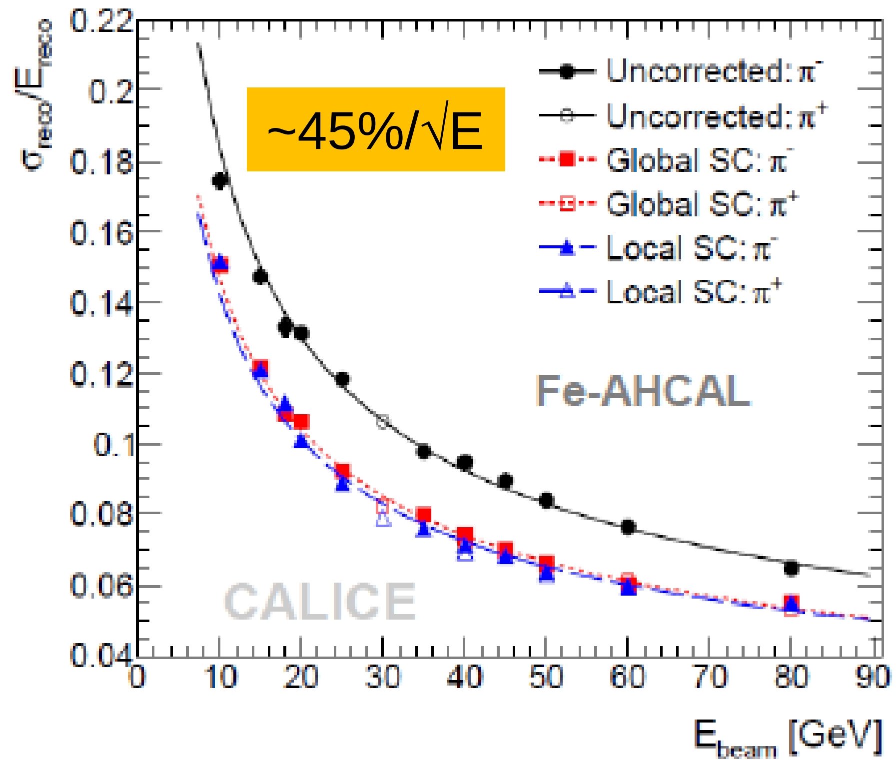
RPC Baseline



DHCAL Prototype Performance



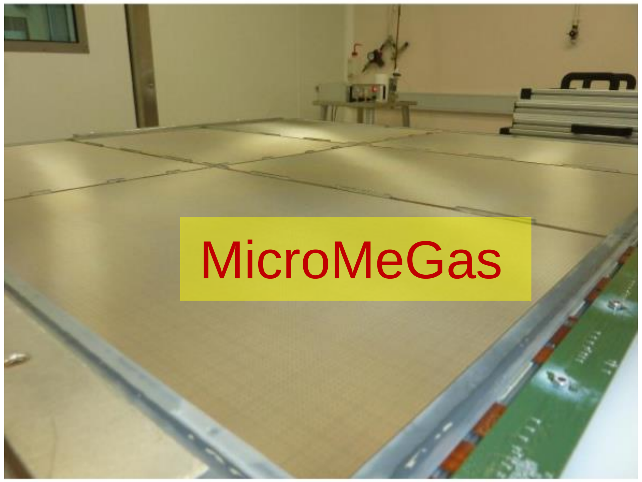
Pion energy resolution after software compensation

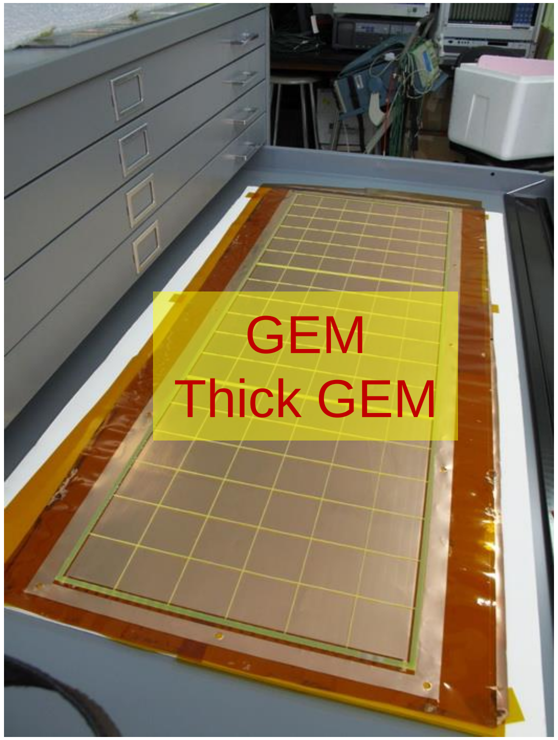


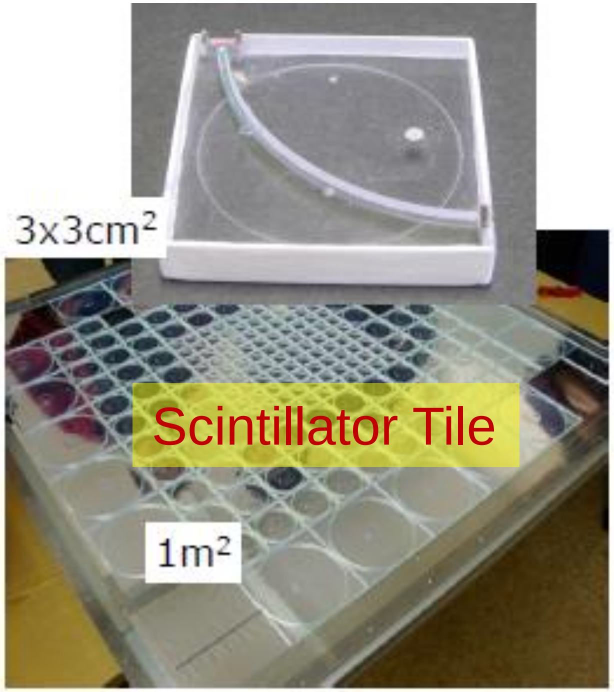
Linearity of pion response

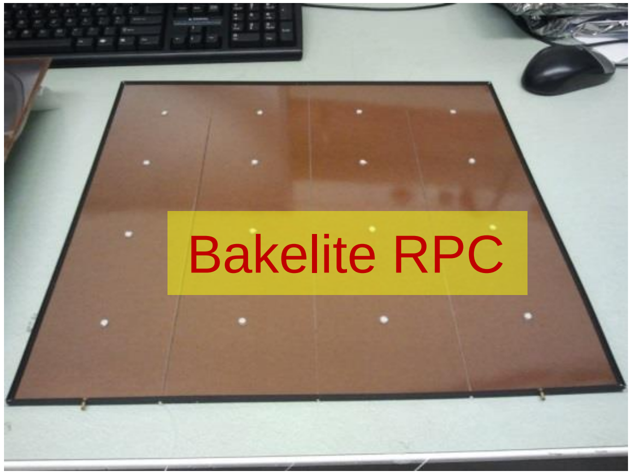
Fit to aE^m

HCAL readout alternatives



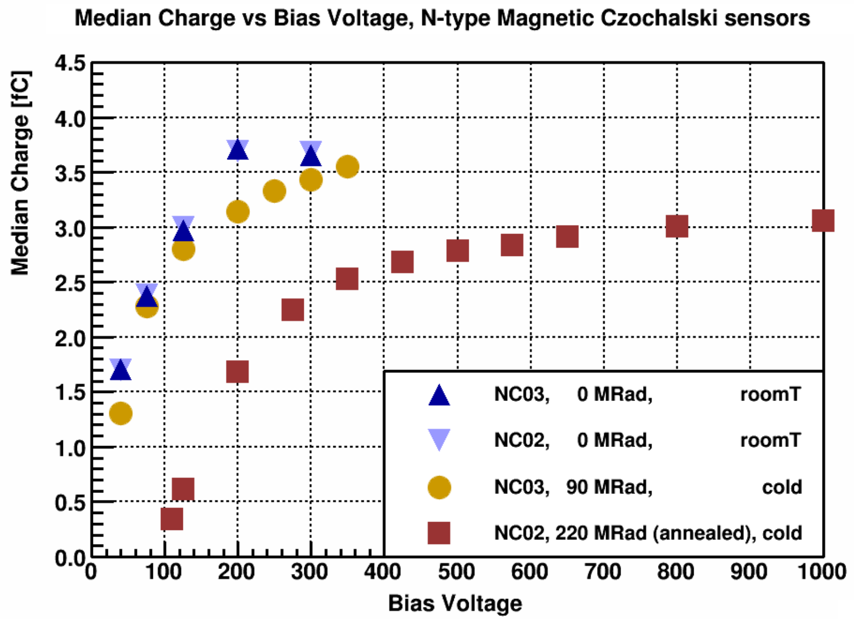






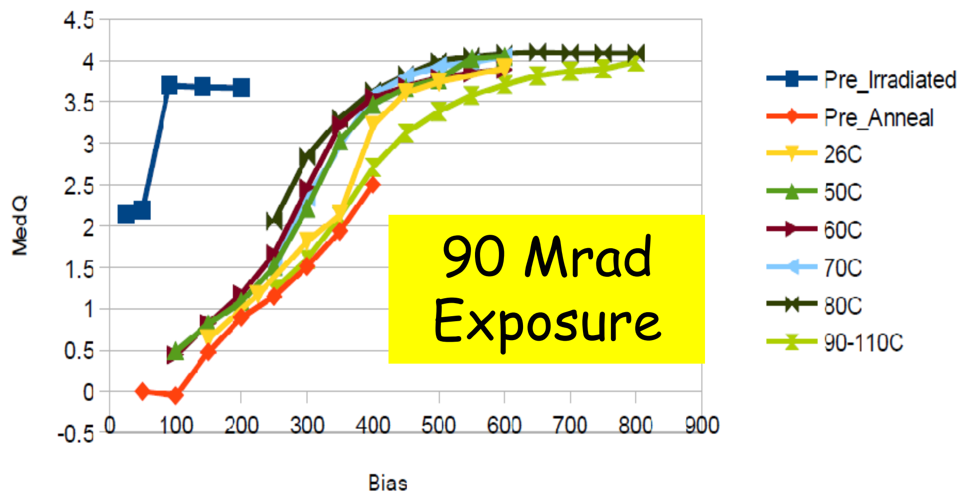
Many alternatives under exploration (largely under CALICE umbrella)

Forward Calorimetry



Ongoing electromagnetic radiation damage studies (Si diode, GaAs…) within FCAL Collaboration umbrella

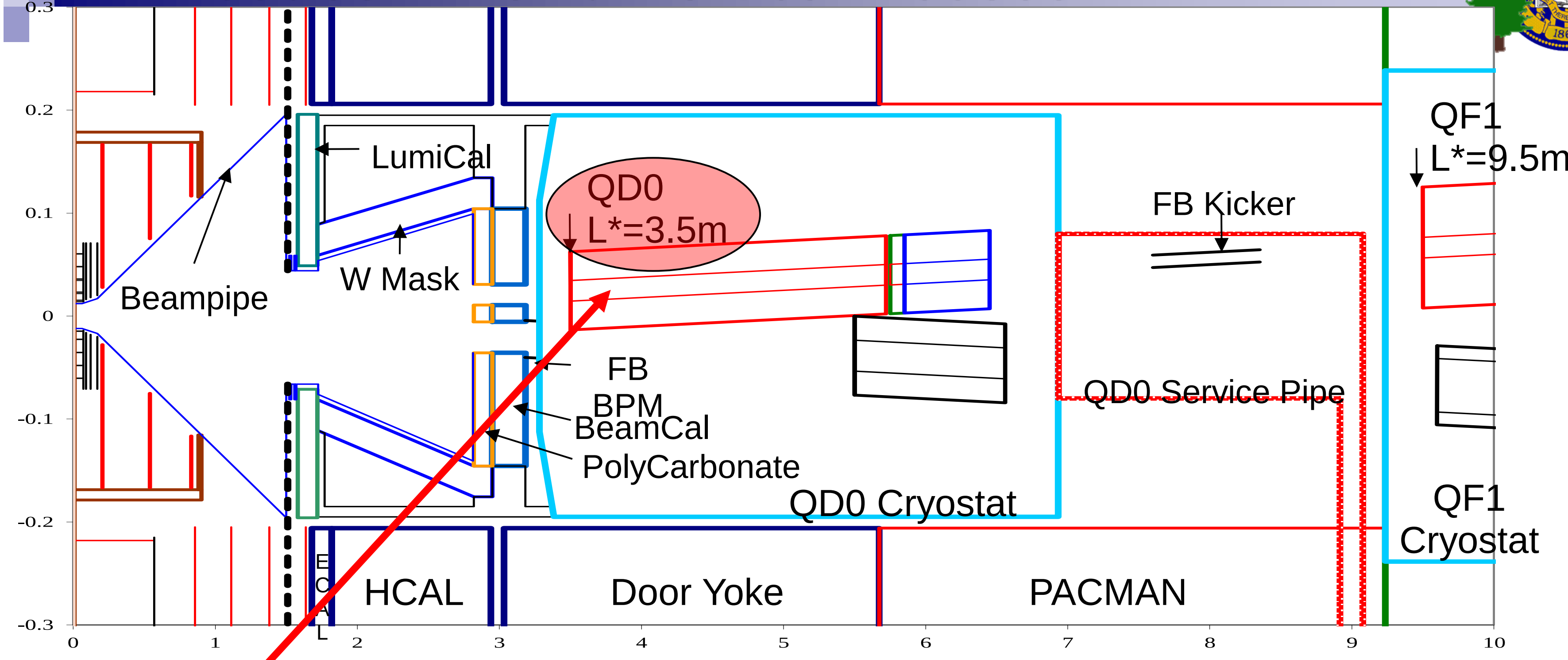
Annealing studies
90 Mrad exposure of N-type float-zone Si diode detector



N-type magnetic Czochralski Si diode detector

Increase in depletion voltage and decrease in charge-collection observed, but performance still adequate for calorimetry

IP Issues: L* and Vertical Access



Uniform L*

- ILC-driven request to have ILD and SiD L* the same (no retuning after push/pull)
- Easy change up to L* = 4m

Vertical Shaft

- ILD-driven request to consider vertical access to IP Hall
- Would work fine for SiD

Optimization Studies Continue…

SiD has reinstated its optimization studies group

Meet by phone once per week (Wednesday afternoon CERN time)

Incorporate realistic Kitikami site constraints in the exploration of SiD performance potential

See Jan Strube's Detector Optimization Plenary talk

- 9:00-10:45 Thursday
- Crown Plaza Mediterranean + Adriatic (80-140)

Many open questions…

Still ample room for groups to make fundamental contributions in a number of areas. An incomplete list would include

- Simulation studies ($e^+e^- \rightarrow ZH$ issues, low-angle $\gamma\gamma$ tagging, σ*BR($H \rightarrow BSM$), flavor tagging, V0 reconstruction
- Pixel sensor R&D
- Tracker optimization, tracker baseline R&D
- HCAL sensor development
- PFA optimization, including calorimeter geometry and tracking/calorimeter integration
- Reconstruction software, including PFA and pattern recognition (Kalman Filter tracker)
- …

Getting/Staying in Touch

Keeping Updated

- Webpage: http://silicondetecor.org
- We have a new *sid-general* mailing list
- Easy to subscribe to
  - Send a mail with `subscribe sid-all John Doe` in the body to **listserv@slac.stanford.edu**
  - https://listserv.slac.stanford.edu/cgi-bin/wa?SUBED1=SID-ALL&A=1
- List will be used for
  - Meeting and Workshop announcements
  - General SiD news
- SiD Newsletter
  - By Email and available via the Webpages

Next SiD Shindigs

At LCWS14:

Time: 9:00 – 10:30, Wednesday
Location: Adriatic (40-70) Crowne Plaza

Elsewhere:

January 12th-15th, 2015
  At SLAC
Everybody is welcome
Hot topics
- Detector optimization
- HCAL technology
- MDI/CFS
- Funding

Under discussion: MDI/CFS meeting attached to the Workshop

Don’t be a Stranger…

Backup

Silicon Tracker Primer II

For gaseous tracking, you need only about 1% X_0 for those 200 measurements (gas gain!!)

For solid-state tracking, you need 8x(0.3mm) = 2.6% X_0 of silicon (signal-to-noise), so 2.5 times the multiple scattering burden.

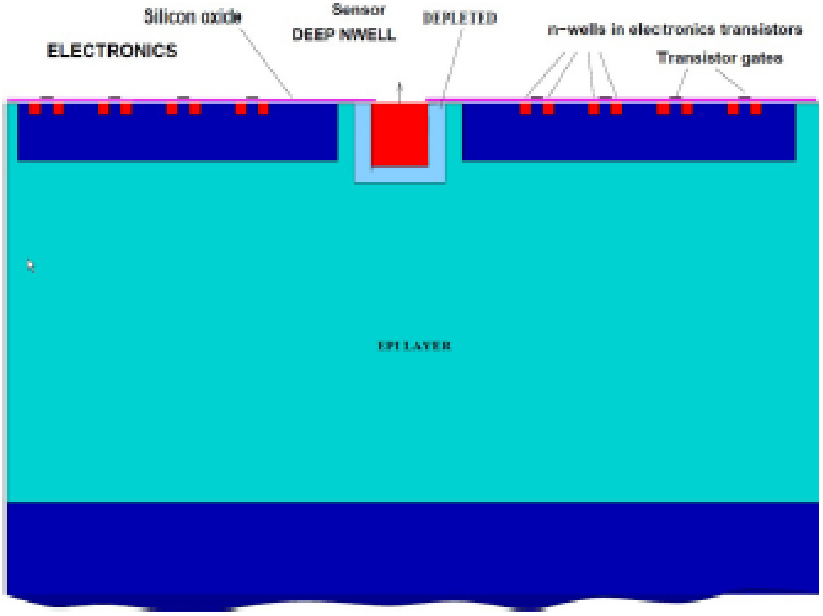
BUT: to get to similar accuracy with gas, would need $(7.1/2.5)^2$ = 8 times more hits, and so substantially more gas. Might be able to increase density of hits somewhat, but would need a factor of 3 to match solid-state tracking.

Solid-state tracking intrinsically more efficient

Chronopixel

Slide courtesy Marcel Demarteau

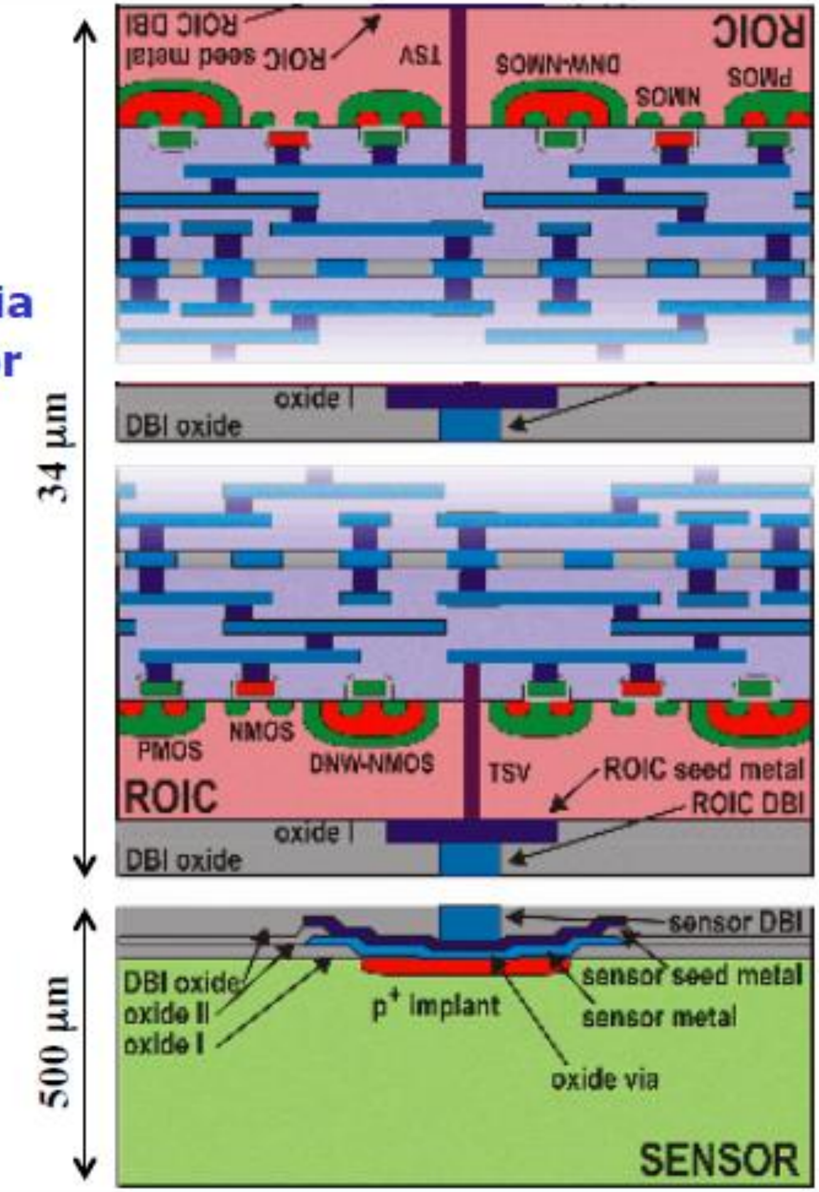
- Prototype 3 of the Chronopixel design has been submitted with many improvements:
  - Decreased sensor capacitance
  - Improved crosstalk
  - Improved timestamp memory robustness
- Prototype 3
  - 25x25 μm^2 pixels, 90nm TSMC
- Six difference sensor designs:
  - Deep and shallow nwells and variations on design
- *Broad program of characterizing the various versions of the sensor and perform quantitative comparison*



VIP Chip

Slide courtesy Marcel Demarteau

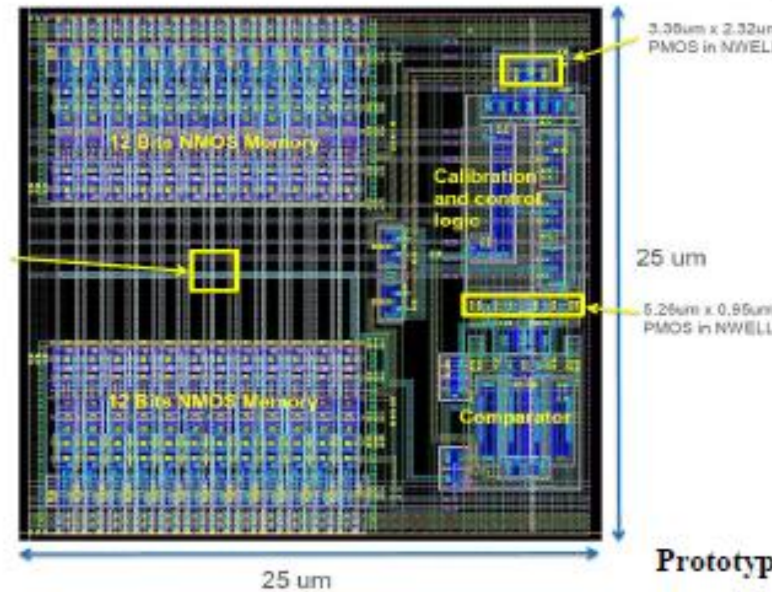
- **Two layer ASIC bonded to sensor**
- **ASIC is thinned to Through Silicon Via for the metal contact to the sensor or other layer of the ASIC**
- **Note: drawing is not to scale!**



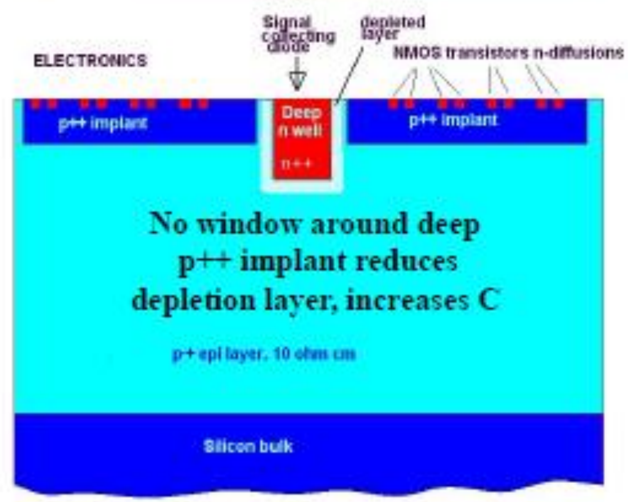
Chronopixel

Slide courtesy Marcel Demarteau

- Chronopixel design provides for single bunch-crossing time stamping
  - When signal exceeds threshold, time stamp provided by 14 bit bus
  - Comparator threshold adjusted for all pixels
- Prototype 1
  - 50x50 μm^2 pixels, 180nm TSMC
- Prototype 2
  - 25x25 μm^2 pixels, 90nm TSMC
- Results:
  - BX time stamping works (300 ns period)
  - Readout between trains demon-strated (sparse readout)
  - Pulsed power (2 – 200 ms ON/OFF)
  - Sensor capacitance larger than expected (because of design rules)



Prototype 2



Back-Up

Intro	2
Sim/Physics	2
VTX	2
Central Tracking	2
EM Cal	2
HAD Cal	3
Muon	1
Forward	2
MDI/Engineering	2
Closout/Appeal	2

1860

TODOs

Tracking: Marcel p37
Physics: Tim p 19
Marcel new summary p22 ff
Jan Opportunties p9
Andy Cal p33-34