

A pixel TPC for the Linear Collider: Towards a demonstrator module

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LCTPC Collaboration Meeting DESY 30.06.2014







- LCTPC-pixel collaboration
- Timepix Chip
- 2013 Testbeam and data analysis
- New demonstrator module
- Summary



LCTPC-pixel collaboration



- R&D towards a pixel-TPC: MPGD + pixel readout
- Groups:
 - NIKHEF: Module construction
 - University of Kiew: Simulation
 - LAL Orsay: Simulation
 - CEA Saclay / DESY: Data analysis
 - Uni Bonn: Module construction, readout system, data analysis
 - Uni Siegen: Data analysis
- Goal: build a demonstator module for a pixel-TPC



Timepix chip

- Universal readout chip
- Properties:
 - active surface: 1.4 x 1.4 cm²
 - pixel size 55 x 55 μm²
 - 256 x 256 pixel array
 - 14 bit counter in each pixel (ToA or ToT)
 - Noise threshold ~500e⁻ (ENC ≈ $90e^{-}$)





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Setup at DESY





Reconstructed tracks





<u>LP module: next steps</u>

~100 chip module (cover 50% of area, 6 mio. channels)

- Project: test a 32 InGrid board in September/October
 - Similar design as 8 InGrid module
 - Expandable to 96 InGrids
- Mechanical design (Bachelor student: Johann Tomtschak)
 - CAD drawings in SolidWorks
 - Construction of light LP frame in workshop
 - Construction of chip support structure in workshop
 - Use water cooling





LP module: next steps

- Powering (Bachelor student: Katrin Kohl)
 - Was already critical for a single octoboard
 - Low voltage supply for 4/12 octoboards?
 - High voltage supply

~100 chip module

- Field distortions between chips (Katrin Kohl)
 - Simulation, implementation and measurements with "road-like strips"
- PCB layout (Jochen Kaminski)
 - Depends on powering
 - Space is limited
 - Need many HDMI cables

InGrid bonding, testing, quality control, calibration^{iniversitätbon}

Field distortions













Scalable Readout System (RD51, CERN)





Chain: Chip – Adapter card+FEC – Computer







JTAG p-ogram

SRS FEC with Virtex 5 FPGA

Timepix chip on carrier

Intermediate board (can carry 8 daisy-chained chips)

Ethernet to PC

Adapter card Type A







Readout system status

- FEC5 based readout worked very well at testbeam
 - Virtex5 FPGA, DDR2 RAM
 - Readout of one octoboard
 - Updates of firmware
 - New hardware e.g. HDMI cables, intermediate boards
- For 96 chip module:
 - 4 octoboards / FEC
 - 3 FECs
- FEC6
 - Virtex6 FPGA, large internal memory
 - 3 FEC6 arrived in Bonn in April
 - Code migration started
 - Design of LP module shaped intermediate board for 12 octoboards started









Pixel-TPC project advances very well

- Successful testbeam 2013
- Data analysis ongoing
- Development of readout system
- Design of a 32 / 96 chip module



=> Demonstrator for a pixel-TPC at the end of this year



Timepix 3, Ceramic grid

Collaborators

LCTPC-pixel:



- CEA Saclay: Andrii Chaus, David Attié, Maxim Titov, Paul Colas
- DESY: Felix Müller, Ralf Diener, Ties Behnke
- NIKHEF: Fred Hartjes, Harry van der Graaf, Jan Timmermans, Rolf Schön, Wilko Koppert
- Uni Bonn: Alexander Deisting, Christoph Krieger, Jochen Kaminski, Johann Tomtschak, Kathrin Kohl, Klaus Desch, Michael Lupberger, Robert Menzen, Thorsten Krautscheid, Yevgen Bilevich,
- LAL Orsay/Uni Kiew: Sergey Barsuk, Oleg Bezshyyko, Oleksiy Fedorchuk
- Uni Siegen: Amir Shirazi, Ivor Fleck

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Scalable Readout System (RD51, CERN)





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Adapter card Type A



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March/April 2013: 2 LCTPC octoboard modules

- Different amplification structures: GEM / InGrid
- Test of readout system
- Readout rate: 2.5 Hz; 40MHz clock
- Electron beam of up to 6 GeV
- Gas: Ar:CF4:iC4H10 (95:3:2) = T2K gas
- ~ 2 Mio. frames recorded, including B = 1 T
- Extensive testbeam program
- Preliminary data analysis in MarlinTPC Robert Menzen



Preliminary Analysis: Cuts



Dataset for first analysis:

z-scan, B=0 T, E_{Drift} = 230 V/cm (D_T = 311 µm/√cm)

 \Rightarrow tracks parallel to x-axis

Cuts:

- Only hits within shutter window
- More than 200 hits per track



Preliminary Analysis: Cuts



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- Entries 400 Preliminary 350 300 250 200 Chip 150 100 50 0-50 -30 -40 -20 -10 0 10 20 30 40 d_0 in mm
- Tracks centred on lower chip row (z dependent)













Transverse spatial resolution





Fit function $f(x) = \sqrt{P0^2 + P1^2 \cdot z}$

P0: intrinsic x-y resolution 327 μ m dominated by field distortions P1 = 310 μ m/ \vee cm: diffusion in T2K for E = 230 V









Data analysis

Martin Rogowski: A new tracking algorithm



Reinvestigate field distortions of Roberts analysis



Algorithm from Forward Tracking Detector for ILD



2013 testbeam

Analysis



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Physics:

- Reconstruct tracks, identify characteristics
- Study detector properties
- Study point/track resolution
- Compare to traditional pad readout

