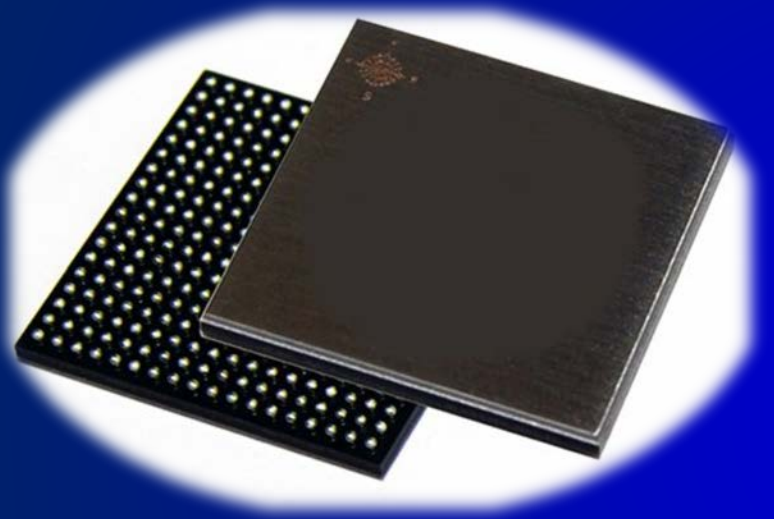
VMM2 electronics discussion

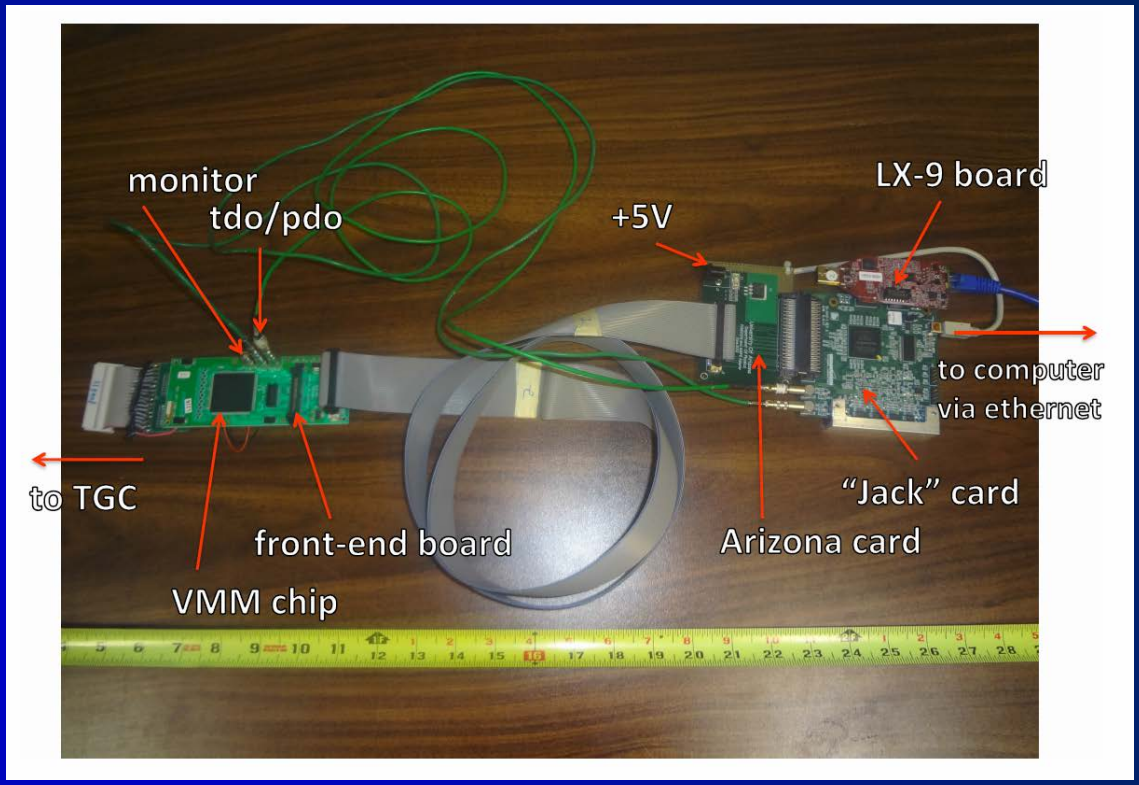
A. Bellerive – LCTPC June 30, 2014

Outline

- ECFA 2013 review suggested to explore using VMM electronics for future LCTPC readout
- Synergy of VMM development between RD51 and ATLAS NSW (sTGC + Micromegas)
- Carleton is interested to contribute to the instrumentation of MPGD modules with VMM2 chips (based on ATLAS NSW experience acquired)
- This talk:
  - VMM status (VMM2 first batch ready August 2014 – VMM3 for late 2015)
  - VMM2 architecture
  - FE boards (options to be explored with ART and trigger companion chip/card, etc…)

VMM Package





VMM2
custom BGA package
21 x 21 mm², 400-pin, 1mm pitch
developed by I2A

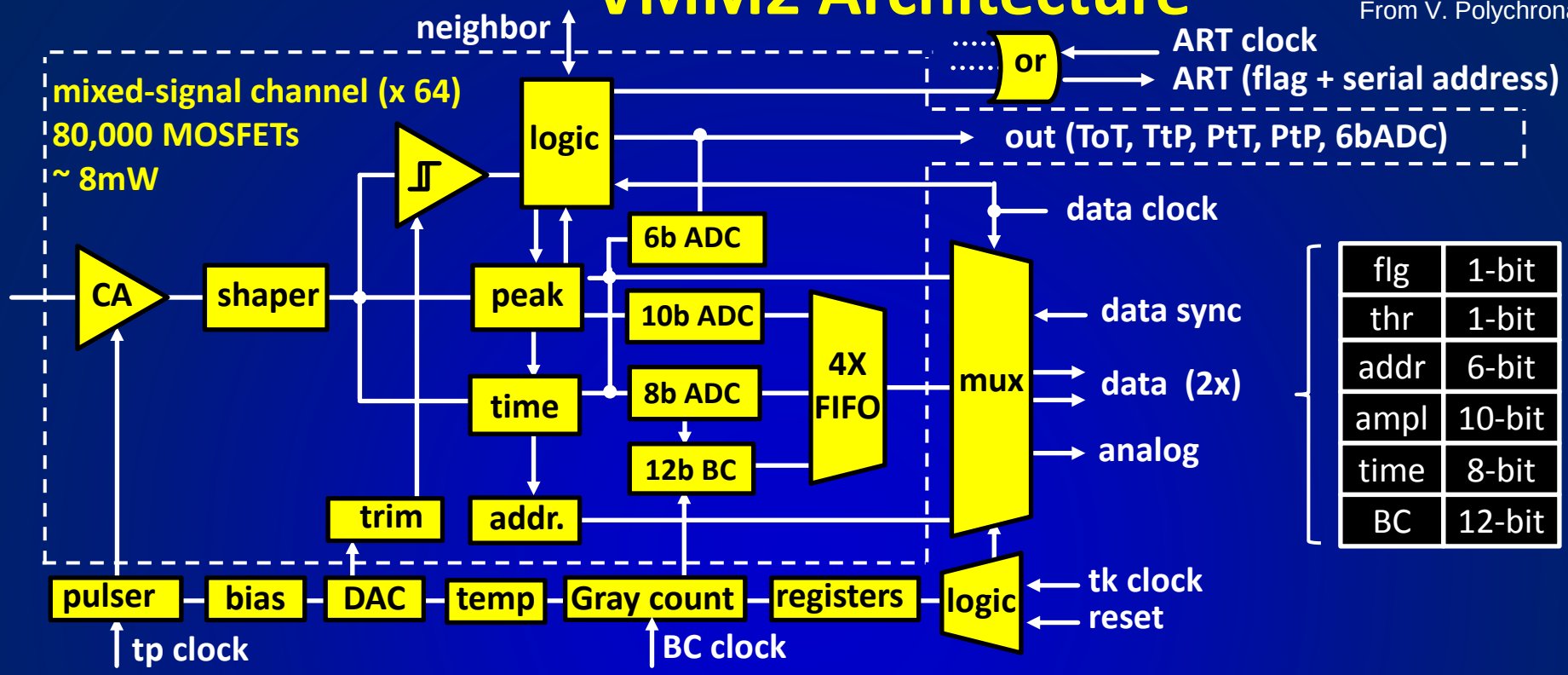
VMM1
Integration for ATLAS NSW
sTGC and MM

BROOKHAVEN NATIONAL LABORATORY

ATLAS

VMM2 Architecture

From V. Polychronakos

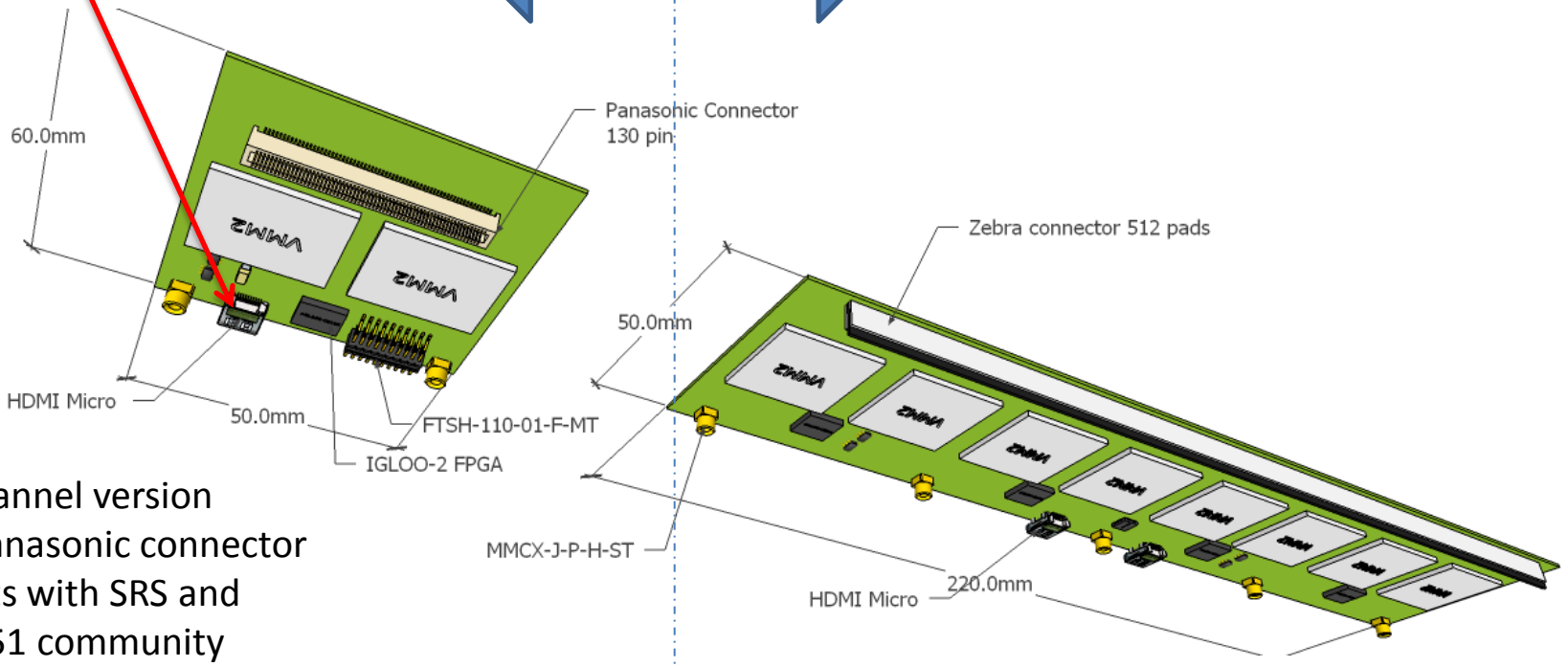


- adj. polarity, adj. gain (0.5,1,4.5,6,9,12,16 mV/fC), adj. peaktime (15,50,100,200 ns), test, mask
- sub-hysteresis discrimination, trimming, channel and chip neighboring
- real-time address (ART) with flag, dual-edge serialized
- peak detector, time detector, analog memories
- 64 direct outputs (ToT, TtP, PtT, PtP, 6-bit ~25ns ADC dual-edge serialized)
- multiplexed analog outputs, serialized address, token passing
- 10-bit ~200ns ADC peak, 8-bit 100ns ~ADC time, 12-bit BC t-stamp, 4x channel FIFO
- dual channel multiplexed digital output, dual-edge serialized with sync signal
- analog monitor, pulse generator, Gray-code counter, temp. sensor, PROMPT (ITAR)

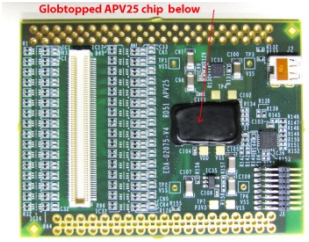
VMM2 hybrids

1 HDMI for L1 Readout
1 HDMI for ART

RD51 ⟷ Design Synergy ⟷ ATLAS NSW



128 channel version
with Panasonic connector
for tests with SRS and
for RD51 community



Modelled after the existing APV hybrid of RD51

512 channel version
with Zebra connector
for NSW

From V. Polychronakos

Summary

- Discussion…