Post-AFTER and Post-S-ALTRO electronics

P. Colas

Status

- Future electronics has been discussed at the previous LCTPC CM and at the ECFA review (november 2013).
- It was decided to start forming a ‘task force’ with electronics engineers, designers of various specialties, but not volunteers were found so far.

Recent developments

- Since then:
  - New ALICE's chip SAMPA (São Paulo, Brazil) chip. 10 Msample/s, self-triggering, but large (32 mW per channel) consumption, for muon chambers and TPC
- ATLAS VMM, VMM2 for Micromegas muon chambers. Canada interested. Possible beam test electronics, but no full-wave sampling.
- Production of a CFE (VFAT3/LCTPC) by AIDA in 130 nm
- Associative memories (in 65 nm) used for fast tracking in ATLAS tracking
- AIDA 2 not really addressing this (65nm, TPC electronics)
- Note that there was a successful implementation of the new DREAM chip (faster, self-triggered evolution of the AFTER chip) on standard FE cards for the HARPO experiment.

- Able to read a whole train continuously (self-triggering)
- Low-noise charge amplifier, about 100 ns shaping
- Prepare for power pulsing (but remain simple for this)
- 9 bit ADC, low consumption
- This does not give a new test electronics.