Electronics and Cooling

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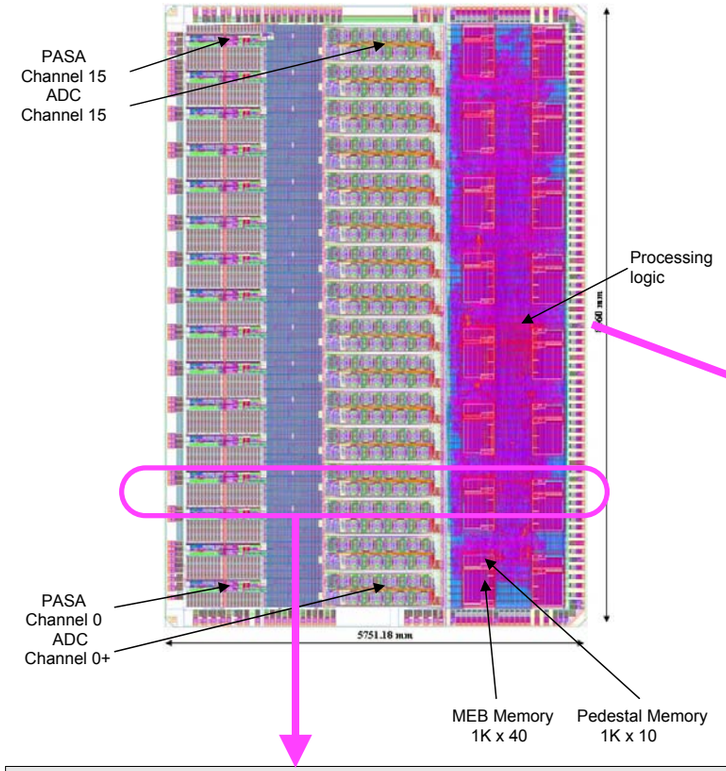
2014.6.1

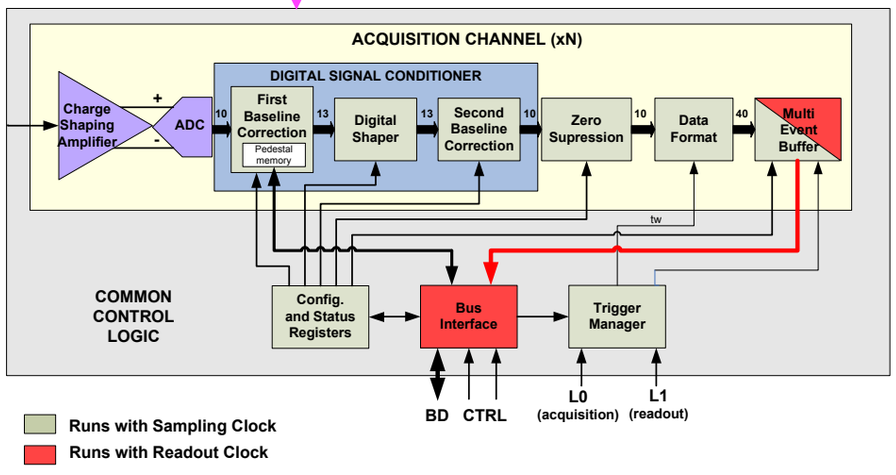
LCTPC face-to-face MTG @ KEK

Introduction:

LCTPC Electronics Development for Pad Readout

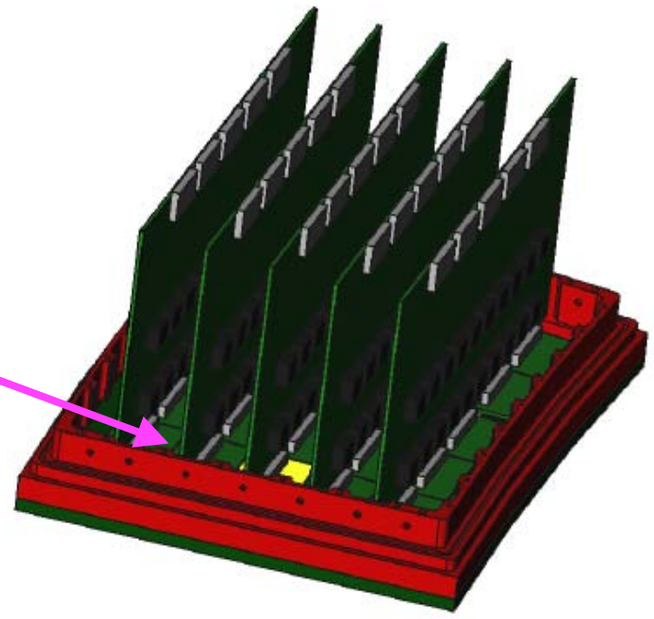
Next step
S-ALTRO16 (fabricated)



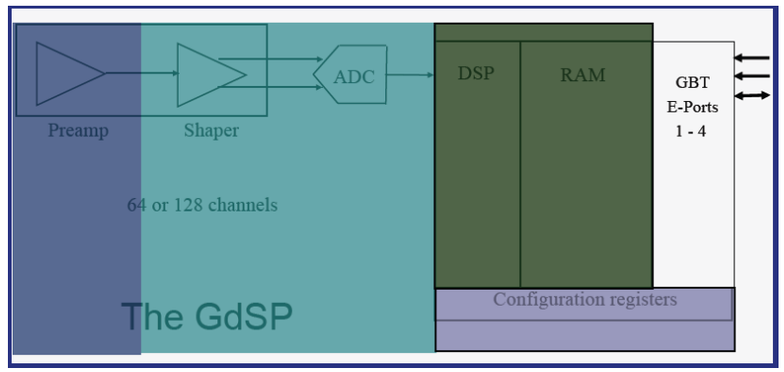


- 16 channels in a chip.
- 38 (56) mW per channel @ 20MS/s
  without (with) links and regulators.

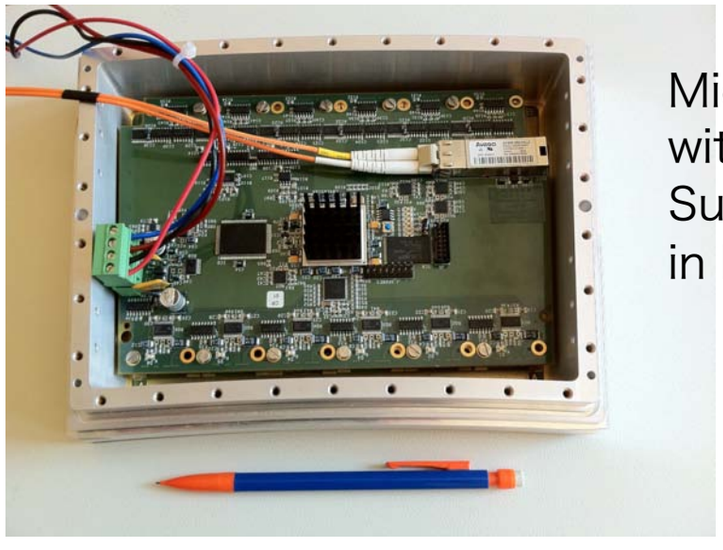
Electronics being prepared
by Lund group.



GdSP concept in the future?



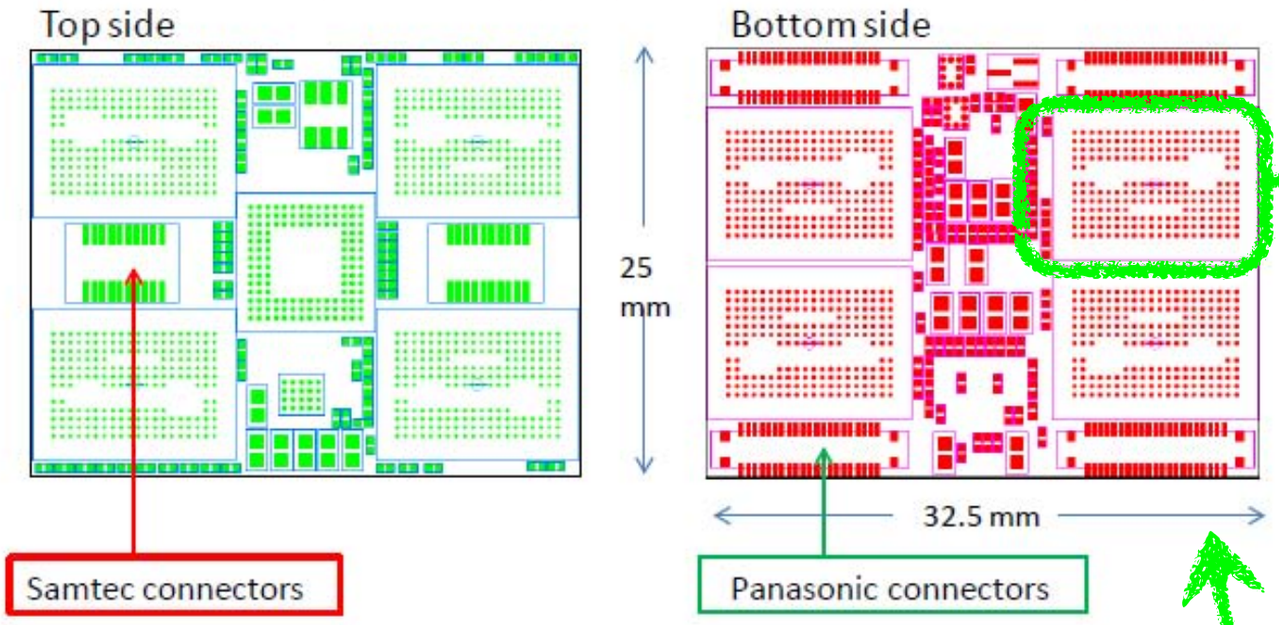
- 64 or 128 channels in a chip.
- Low power consumption (7-8mW/ch).
- 65nm process or less?
  not ready to start now?

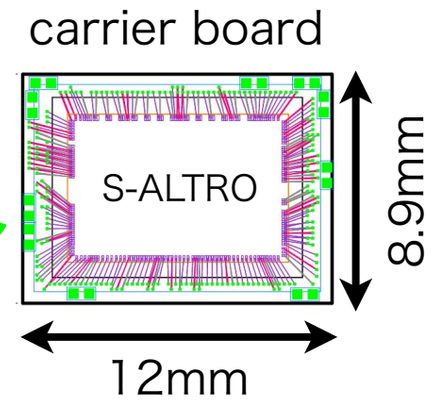


MicroMegas module
with AFTER-based electronics.
Success with CO_2 cooling
in beamtests Feb/2014.

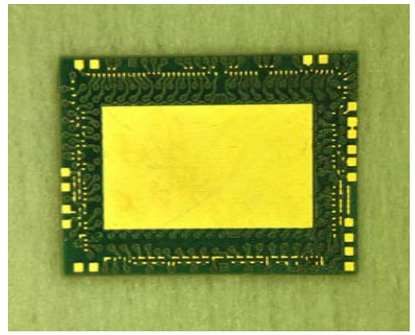
Readout electronics based on S-ALTRO16 chips

Final MCM Bd design by Lund Univ.

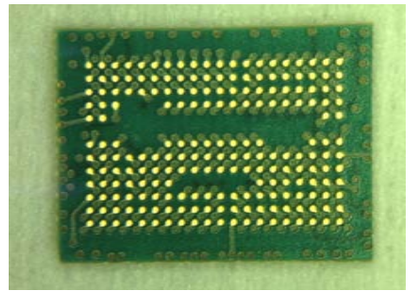




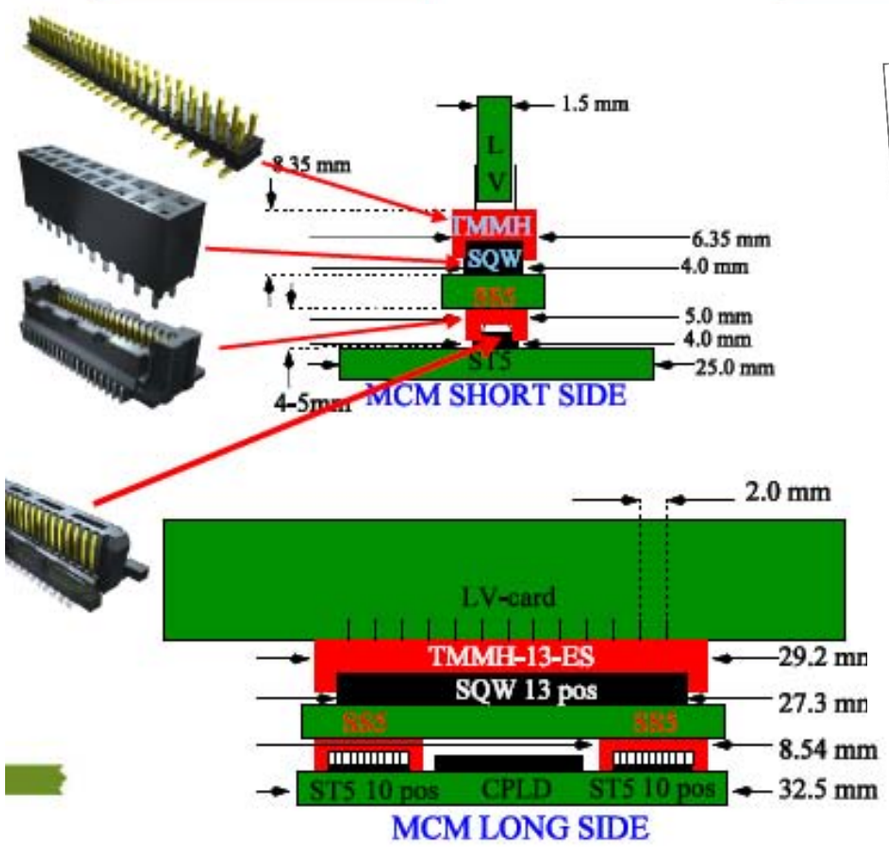
3 CBs were fabricated and ready for test

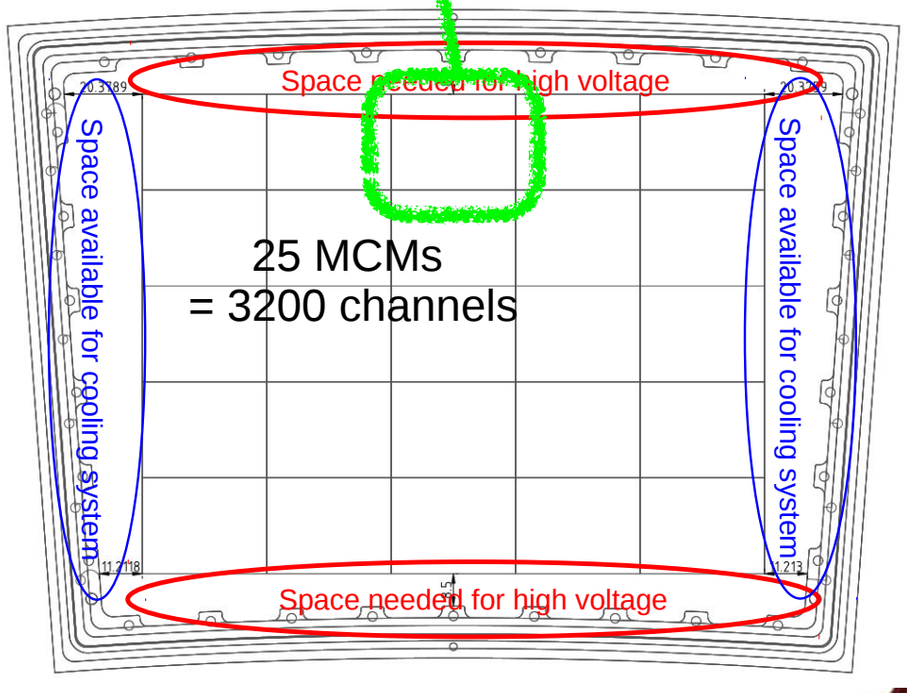


chip side

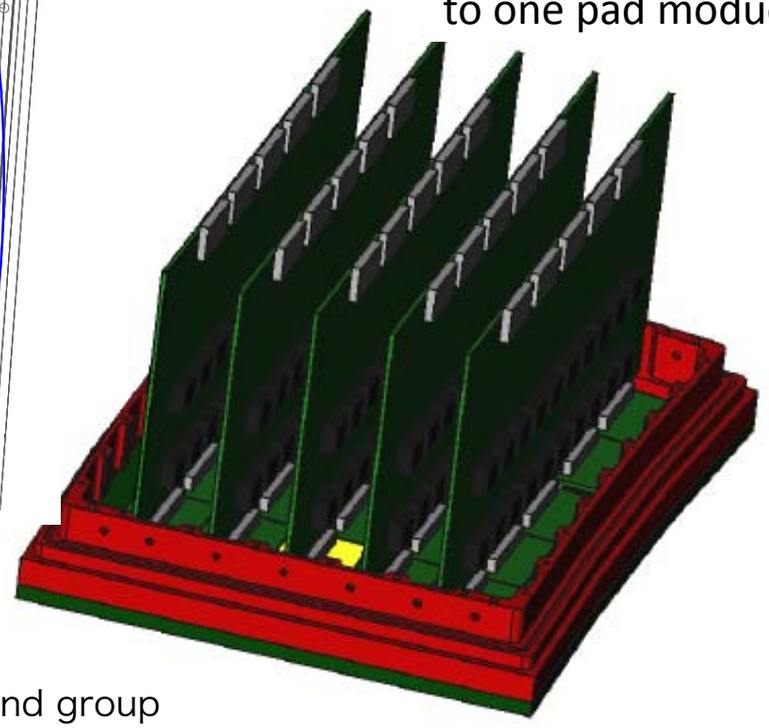


BGA side





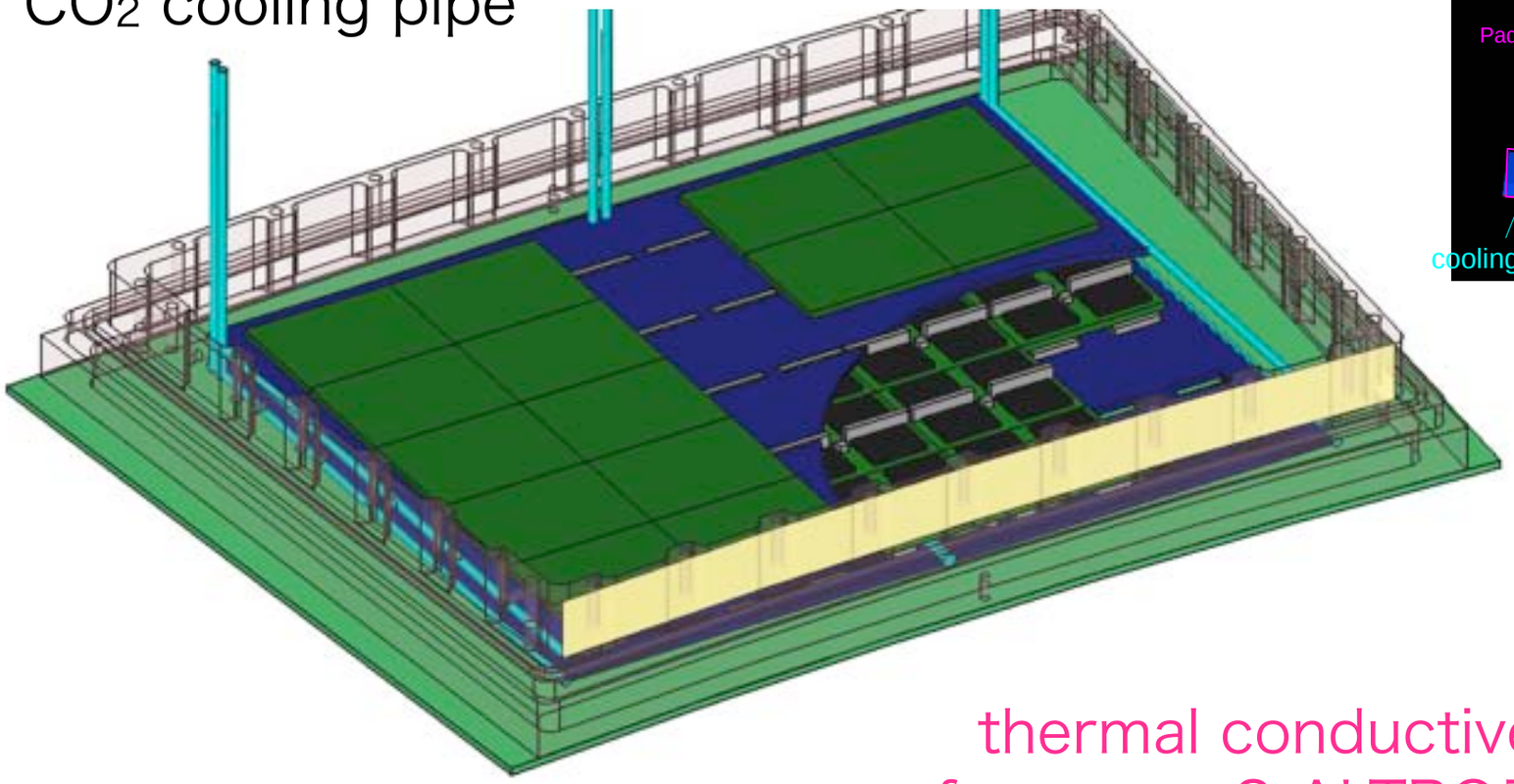
LV-boards attached to one pad modue

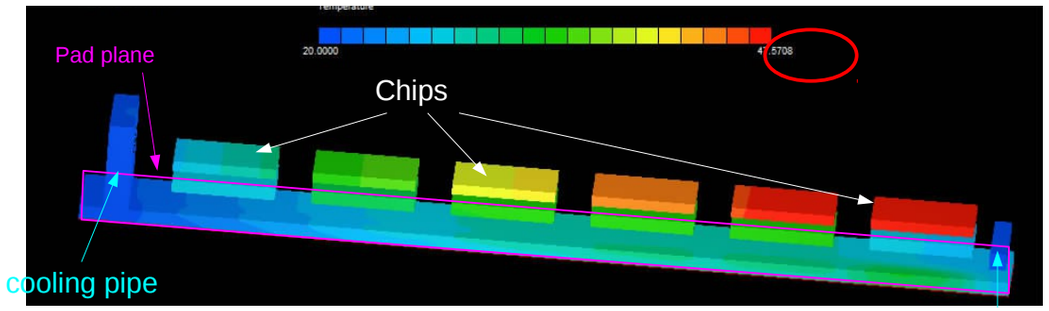


Figures from “Front-end electronics for the TPC in ILD; a status report April 2014,” etc. by the Lund group

Proposed Cooling for S-ALTRO16-based electronics

CO_2 cooling pipe

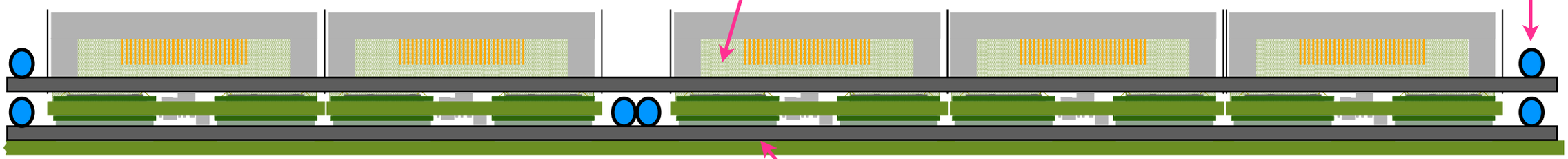




Simulation showed that
Middle pipe is necessary

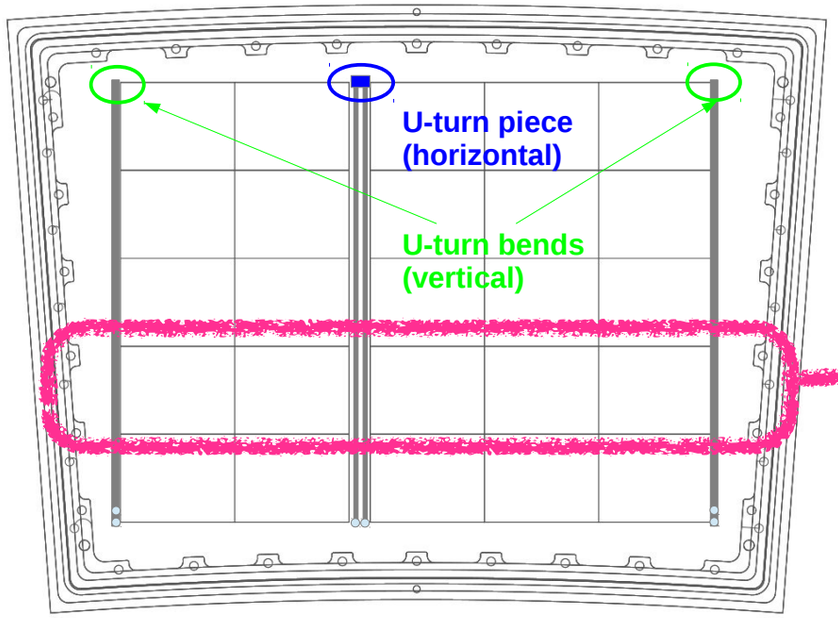
thermal conductive plate
for upper S-ALTRO16 chips

CO_2 cooling pipe

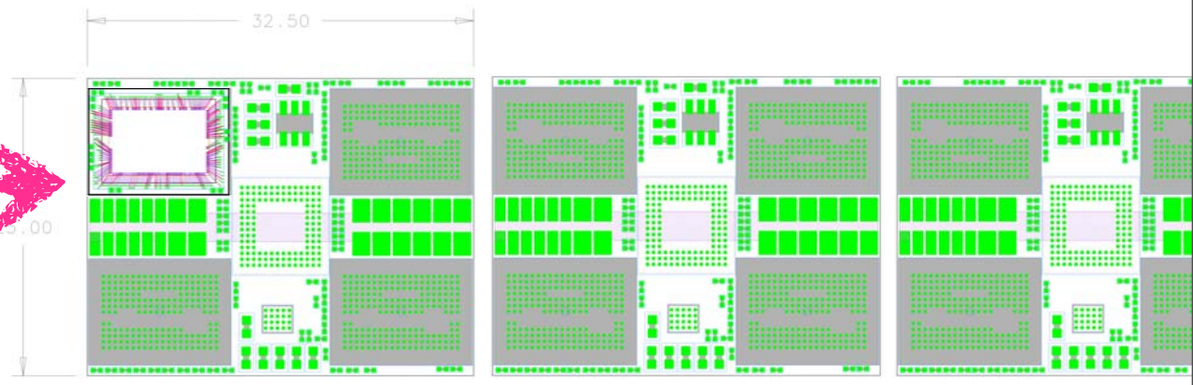


thermal conductive plate
for lower S-ALTRO16 chips
and to keep pad-plane temperature

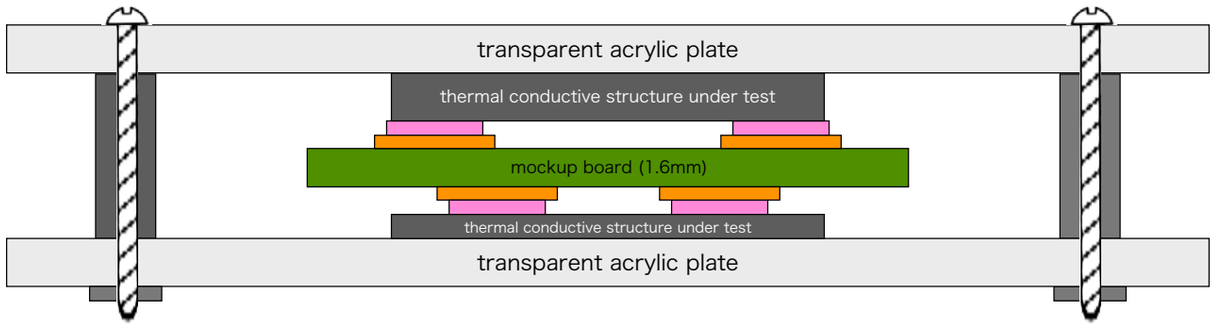
Mockup Test Plan

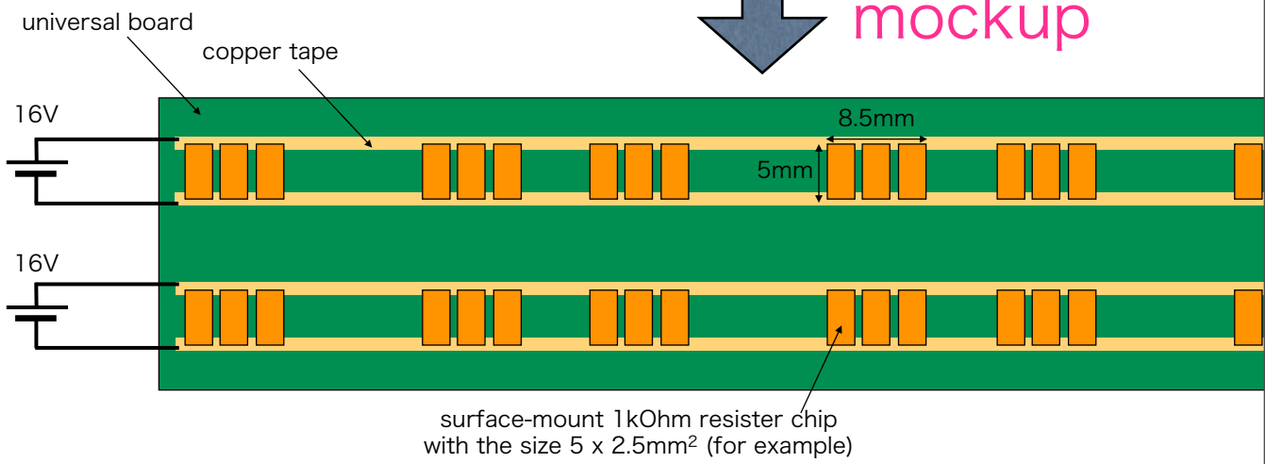


5 MCMs



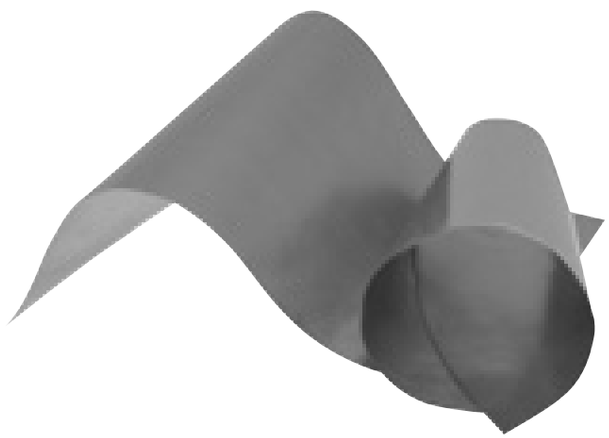
mockup





Combination of various thermal conductor/insulator will be tried

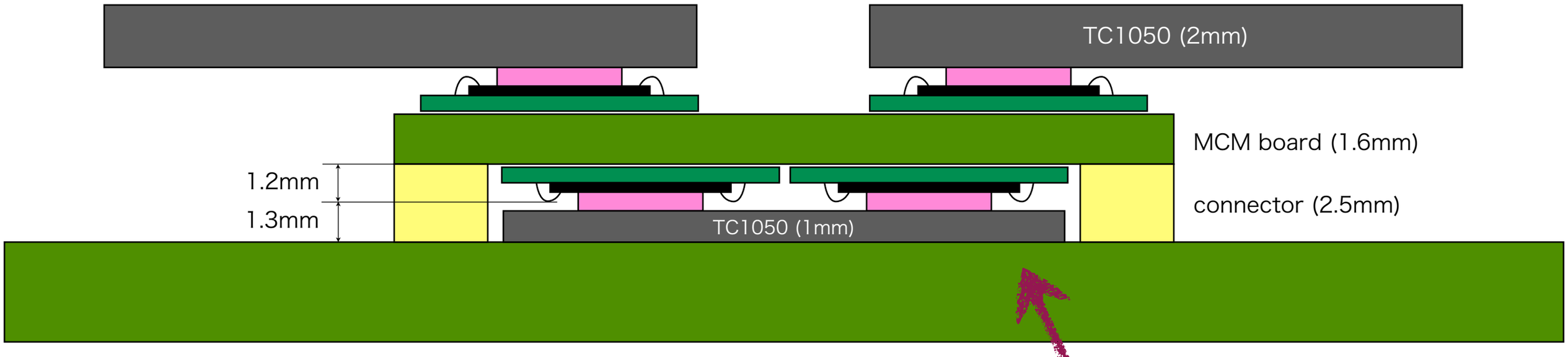
TPG plate (by Momentive)
~1500W/m・K
sandwiched by Al plate

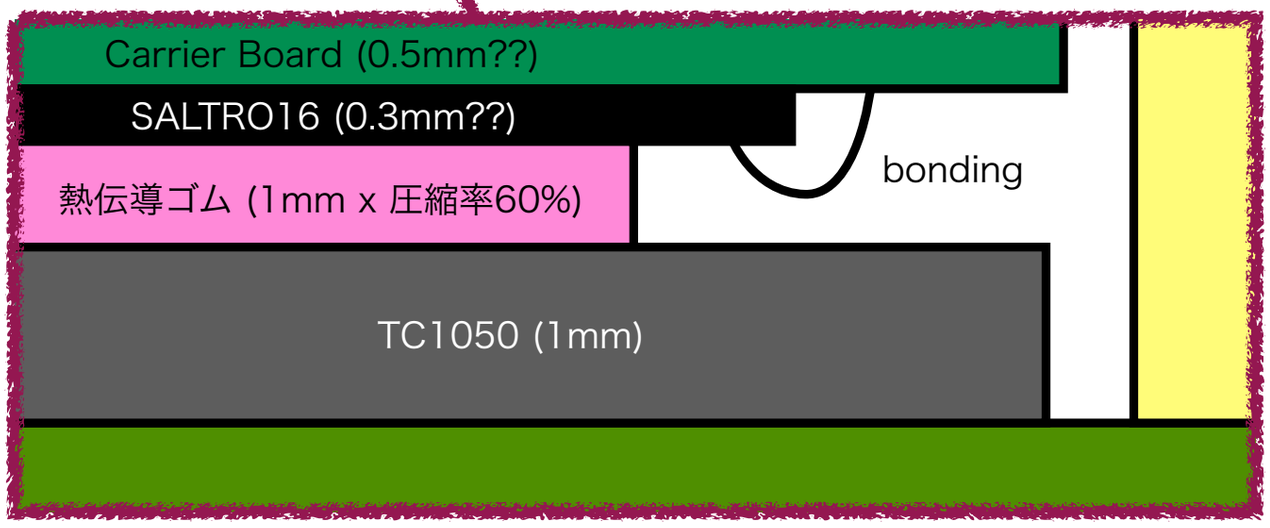


PGS graphite sheet
(by Panasonic)
~1500W/m・K

heat insulating sheet
(by Polymatech)
~0.02W/m・K

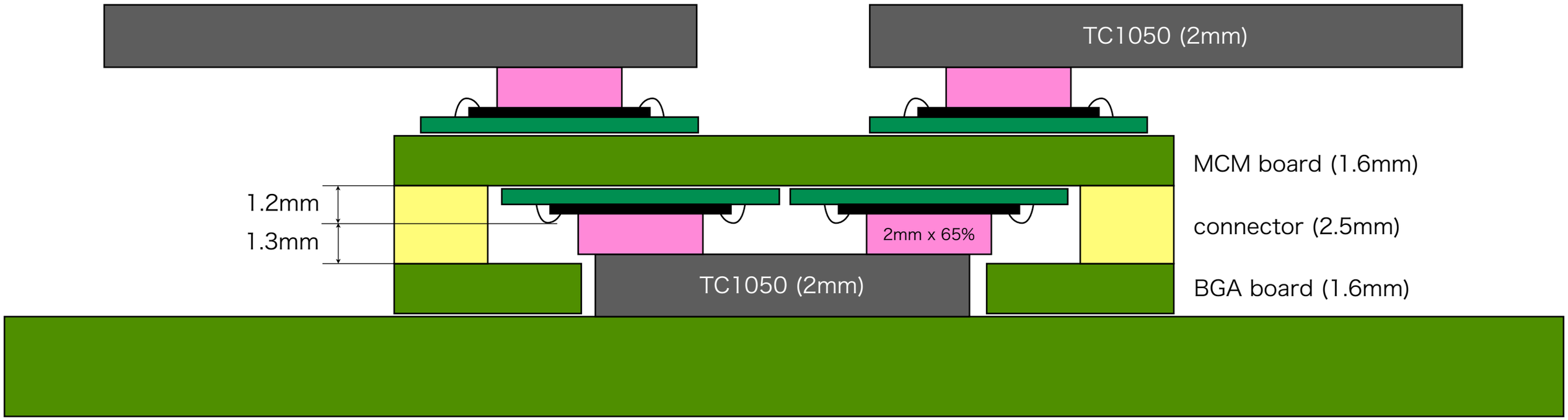
2.5mm space limited by the connector height





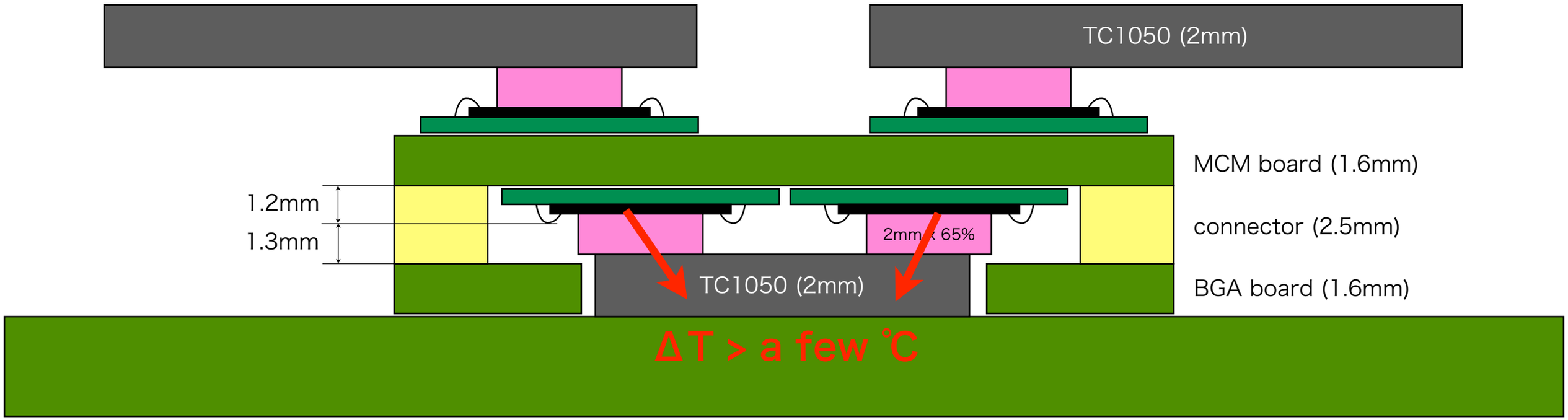
Taking into account the epoxy protecting the chip and bonding, insertion of 1mm-thick TC1050 will be difficult.
→ This structure will not go well.

Idea: BGA board can increase the height



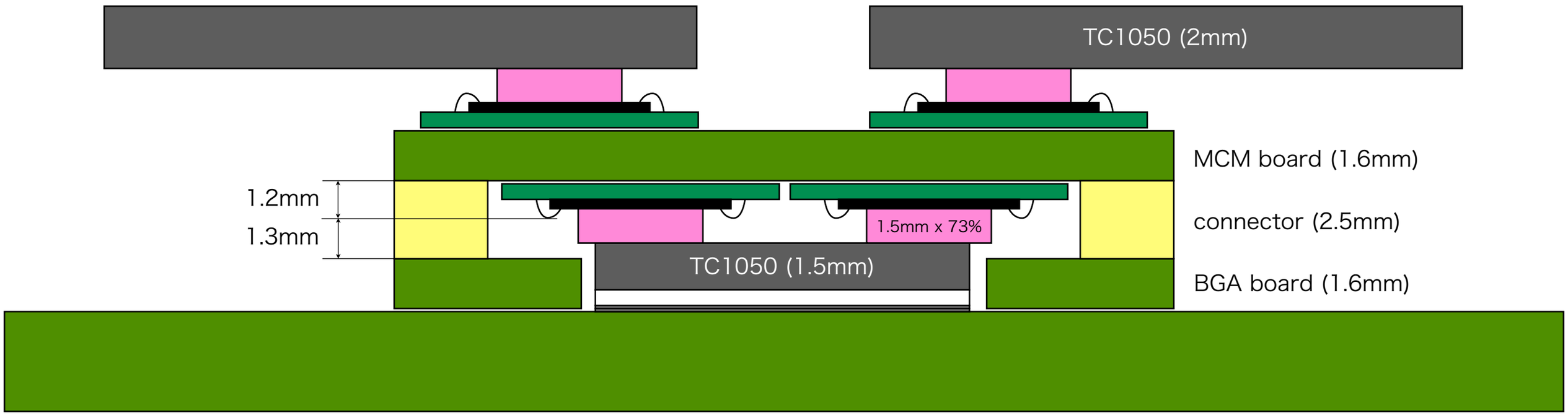
Make it higher so that 2mm-thick TC1050 can be inserted.

Idea: BGA board can increase the height

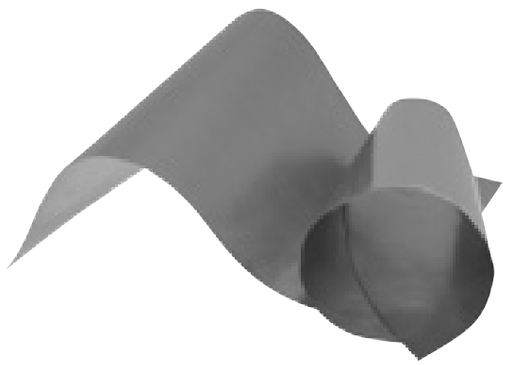


Even with this setup, temperature gradient will be a few ℃.

Idea: combination of conductor and insulator



"PGS® graphite sheet

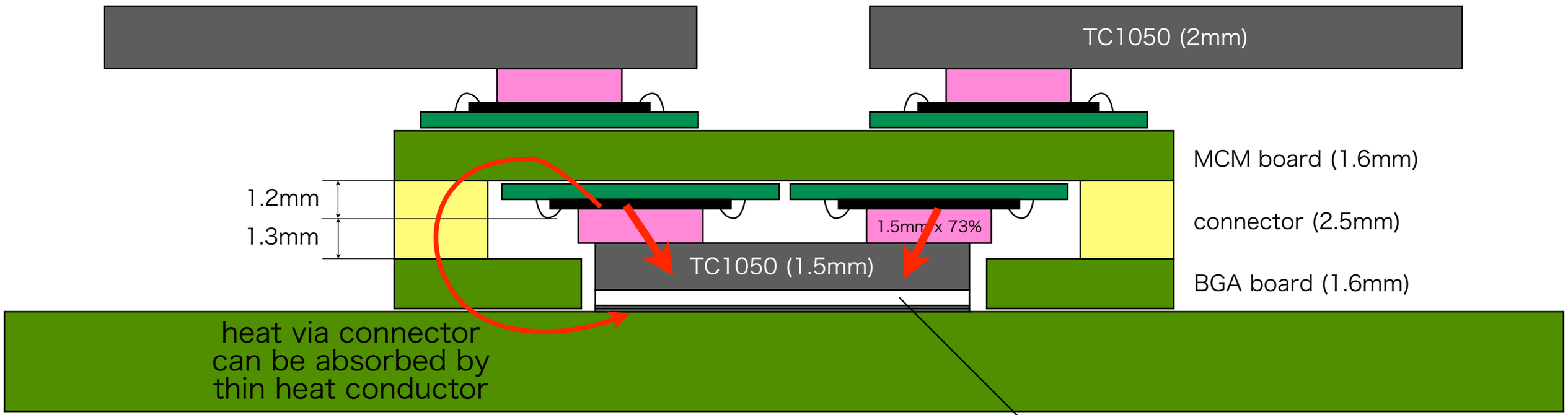


http://industrial.panasonic.com/www-ctlg/ctlgj/qAYA0000_JP.html

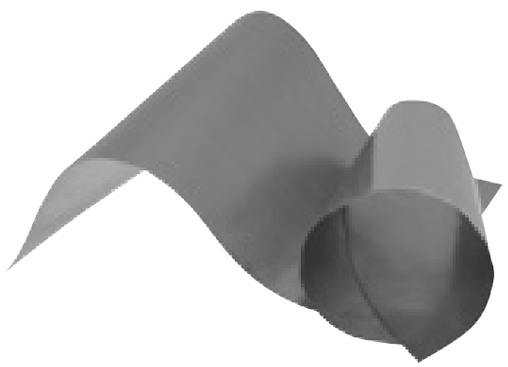
700W/m・K

heat insulator with conductance 1/10 of kapton and less than air.
http://www.polymatech.co.jp/c-6.html

Idea: combination of conductor and insulator



"PGS® graphite sheet



http://industrial.panasonic.com/www-ctlg/ctlgj/qAYA0000_JP.html

700W/m・K

heat insulator with conductance 1/10 of kapton and less than air.
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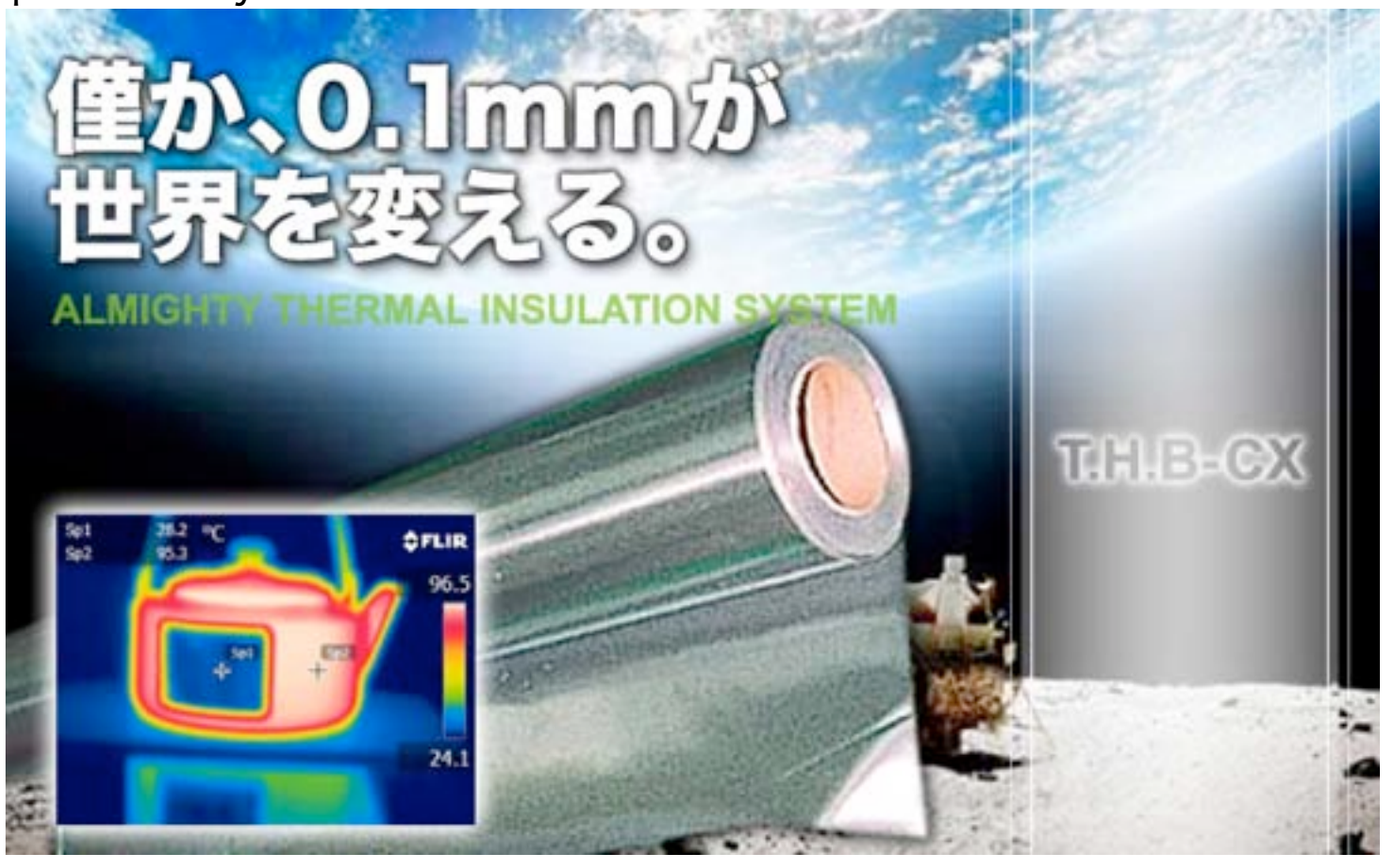
Better heat insulator?

product by nihon-shanetsu.

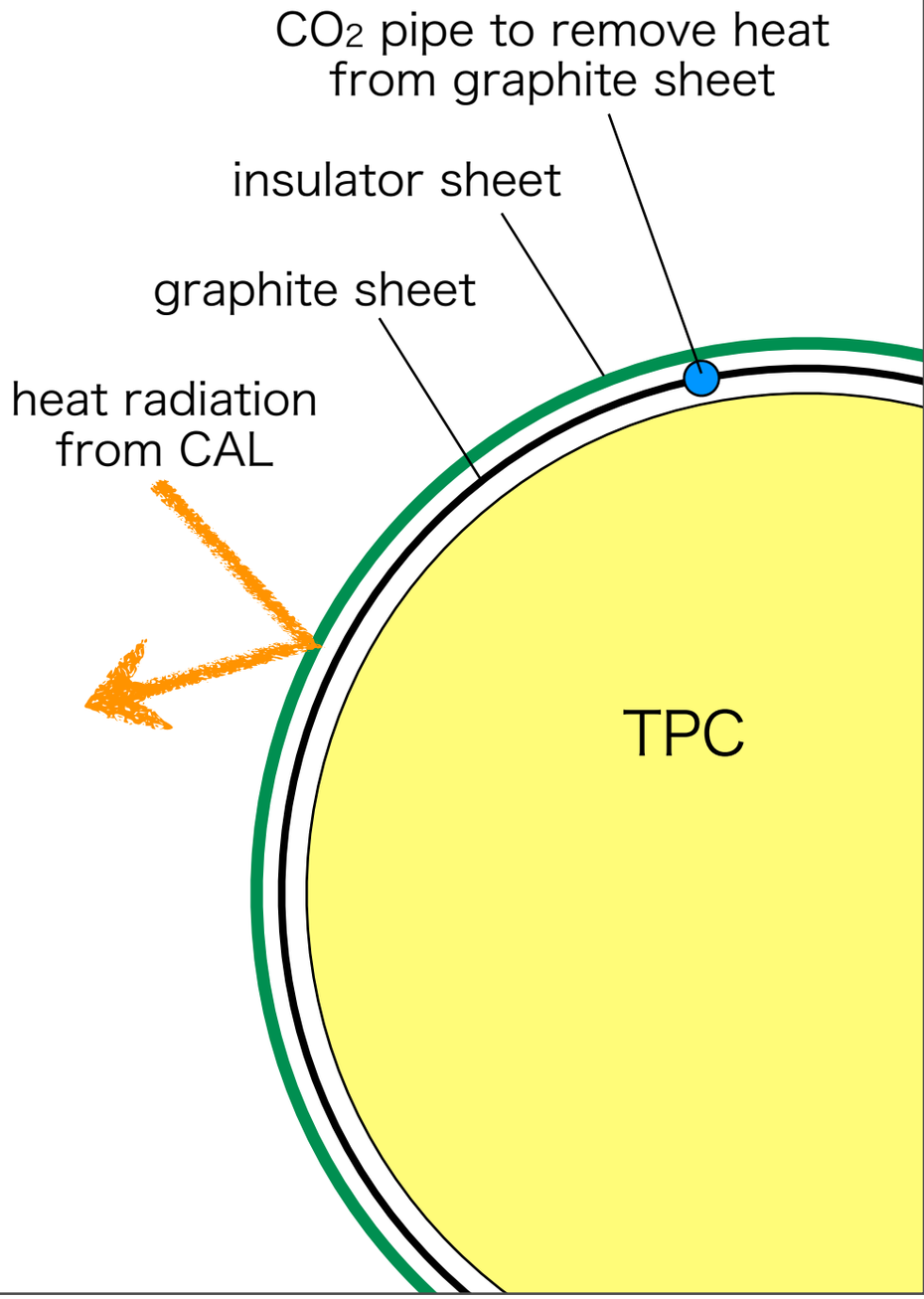


http://topheat.jp/product/index.html

0.1mm-thick with 5 layer structure.

According to the website, pressure may increase the heat conductance, which is not good for us.

Instead, the material may be useful for blocking heat transfer btw. VTX and TPC, or btw. TPC and CAL.

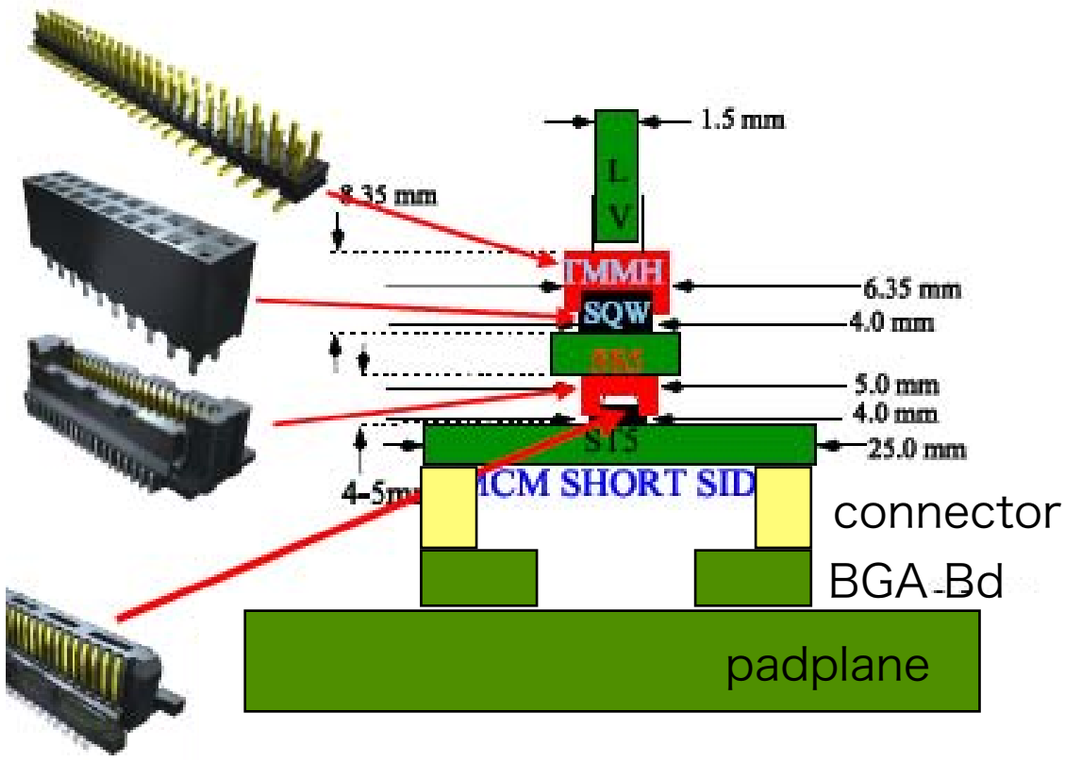


Issue: Next generation of frontend ASIC

- GdSP seems waiting technology advance.
- In the meantime, how can we obtain our necessary chips?
- Possibility: Launch our ASIC development group?
  w. help of an expert at Nagasaki I.A.S. (for example)?
  w. help of OpenIt consortium?

Issue: Development of Pad-plane for S-ALTRO16

Complicated structure!

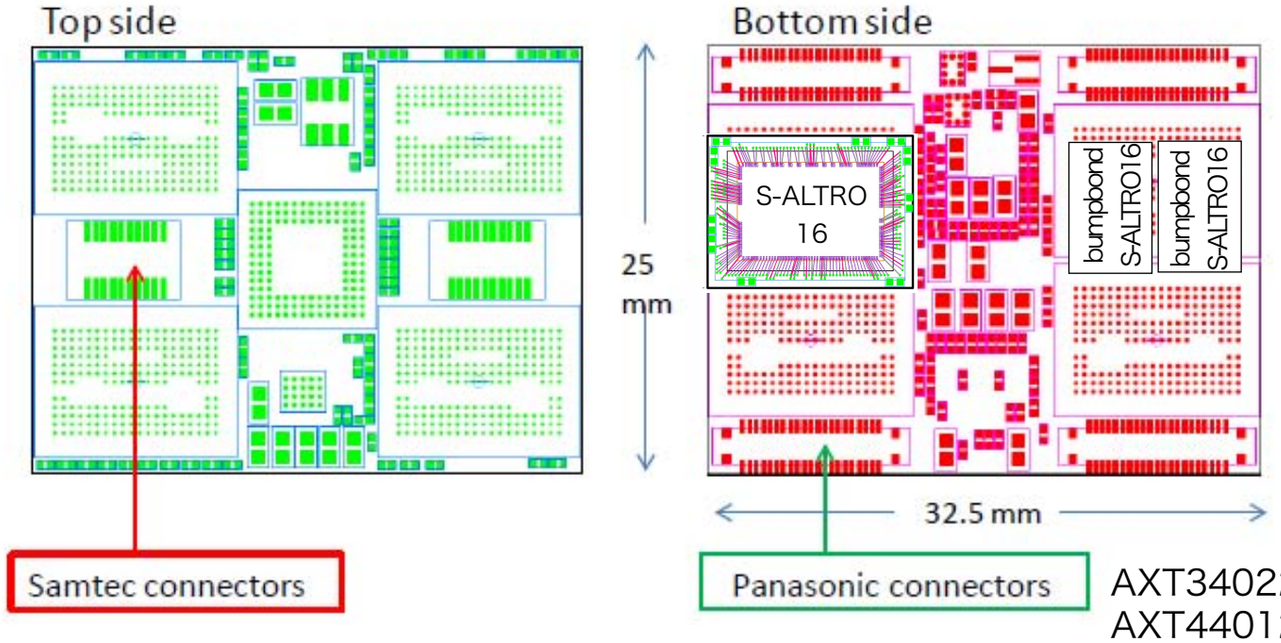


(according to the Lund report)

The design of the MCM-board is essentally ready but will be redesigned in so called High Density Interconnect (HDI) technology. This allows for a higher routing density, for both signals and voltage supply, compared to conventional PCB design. A reduction in the number of layers, from the current 20 layers to maybe 10, can be envisaged. Vias can be made as small as 25-50 μm by laser drilling. This technology also offers the possibity to mount components, electrical or mechanical, into cavities in the PCB, which are covered with one or more dielectric layers. The components are, thus, embedded into the PCB and the suface is essentially left free for surface mounting of readout chips. This will be a valuable excercise for the final design. If this technology is applied to the pad plane it might offer a solution to integrate the cooling into the PCB by including a layer of RO4000 hydrocarbon ceramic laminate, which has a high thermal conductivity and is compatible with multilayer PCB construction. Such solutions have to be discussed and developed together with the relevant PCB manufacturers.

We plan to produce a mock-up system to check that the mounting of the components and connectors on the MCM-board does not lead to unexpected difficulties and that the various parts fit together.

Can we monut full channels (5000ch) as next step?



Twice the channels, twice the power,
twice the connectors, half the cooling area.

→ ・no enough area for S-ALTRO16
even with bump bonding.
・4-times thickness of TPG necessary.

If replacing the ADC by SAR type makes the chip area half, it might be possible.

AXT340224 (socket)
AXT440124 (header)