VXD Optimisation

Yorgos Voutsinas
DESY FLC group

georgios.voutsinas@desy.de

Outline

- Long term goal
  - Define the (often conflicting) set of VXD parameters
- Single tracks study
  - Momentum – Impact Parameter (IP) resolution
- Tracking performances
  - Address few questions on time – spatial resolution trade off for CMOS VXD concepts
- Proposed physics studies

Single Tracks – Examined VXD Concepts

- Scope of the study
  - Focus on spatial resolution
  - See how Impact Parameter & Momentum resolution behave as a function of the sensors single point resolution
    - Could indicate if the assumed sensor single point resolution values are sufficient
    - Could give hints for the VXD parameters optimisation
      - More relevant for detectors who slices the bunch train (e.g. CMOS, DEPFET)
  - Start addressing again the VXD layout
    - Double layers (FPCCD, CMOS)
    - Single layers (DEPFET)
  - Use DBD VXD concept as a reference
- Procedure
  - Take the DBD VXD and substitute the relevant spatial resolution values (with the exception of the single layers model)
  - Use the std tracking software
    - We don't examine time resolution – beam bkg here

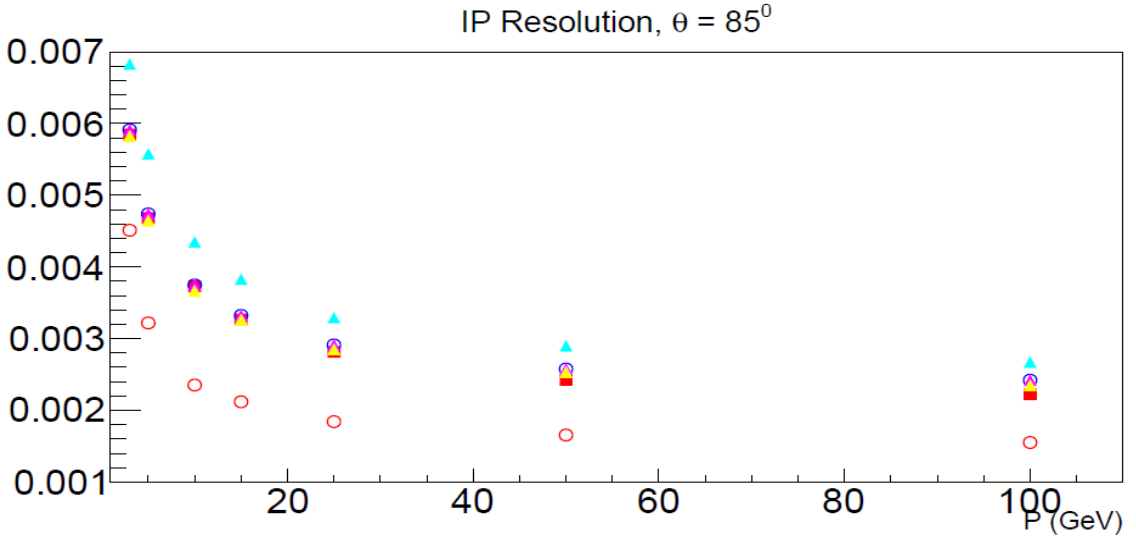
Single Tracks – Examined VXD Concepts

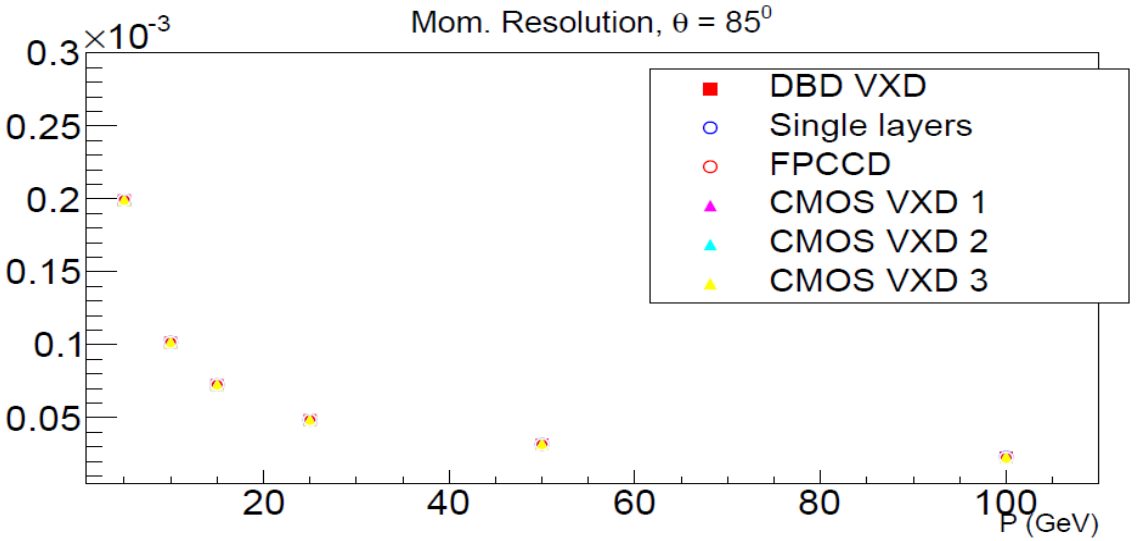
- Examined models
  - DBD VXD
    - Hybrid det., CMOS – like ladders and FPCCD – like shell and cooling system
  - Various CMOS design
  - FPCCD design
  - Single layers VXD (remained unchanged since LoI)
    - R_{in} 15mm, MB 0.11% X_0 / layer, s.p. resolution 2.8μm

	DBD VXD		CMOS 1		CMOS 2		CMOS 3		FPCCD	
layer	σ_{sp} (μm)	σ_{time}(μs)	σ_{sp} (μm)	σ_{time}(μs)	σ_{sp} (μm)	σ_{time}(μs)	σ_{sp} (μm)	σ_{time}(μs)	σ_{sp} (μm)	σ_{time}(μs)
L1 / L2	3 / 6	50 / 10	3 / 6	50 / 2	5 / 5	8 / 8	3 / 5	50 / 8	1.4 / 1.4	Full bunch train
L3 / L4	4	100	4 / 10	100 / 7	5 / 5	16 / 16	5 / 5	16 / 16	2.8 / 2.8	
L5 / L6	4	100	4 / 10	100 / 7	5 / 5	16 / 16	5 / 5	16 / 16	2.8 / 2.8	

Single Tracks – Results

- All VXD models exhibit similar momentum resolution
  - TPC plays the dominant role
  - ILD goals are satisfied
- DBD VXD vs CMOS 1: one can optimise the outer layers for time resolution & power dissipation
  - s.p. res of outer layers : from 4→10 μm (>10Xfaster, more power efficient) → negligible effect to IP resolution
- The same doesn't hold true for the inner layer
  - CMOS VXD 3 (3μm) clearly better than CMOS VXD 2 (5μm)
- All concepts (except CMOS 2) behave similar or better (FPCCD) than the DBD detector
- FPCCD has the best IP resolution
- Even CMOS 2 goes asymptotically to 3μm – is it good enough for c – tagging ?





Tracking Perf. vs VXD Parameters

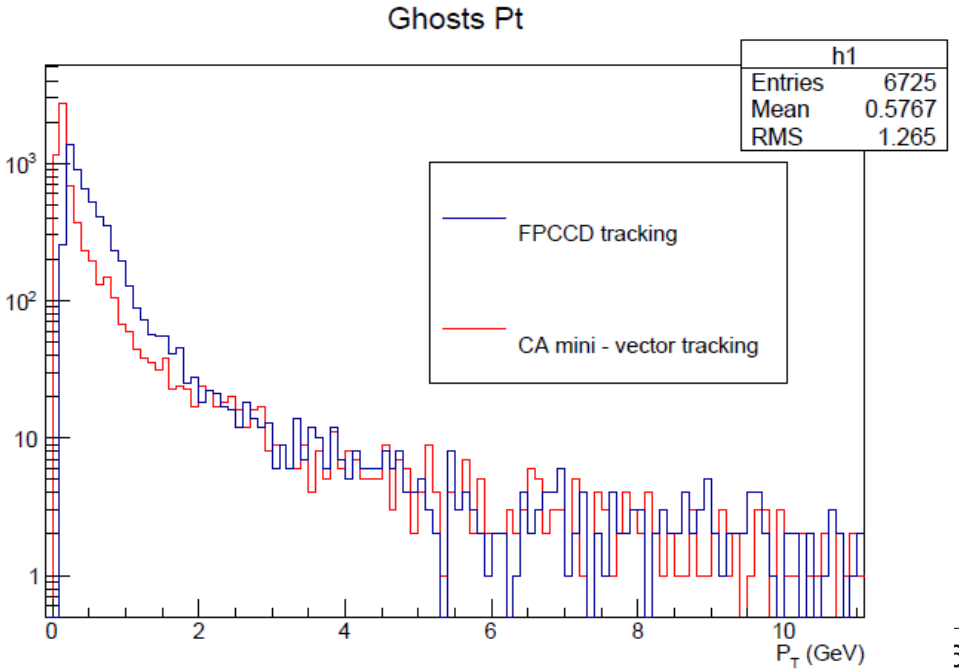
- To address the optimisation of VXD par. the pair bkg should be taken into account
  - Study tracking performances as a function of VXD parametrisation
  - Use ttbar sample, $\sqrt{s} = 500$ GeV, pair bkg overlaid
- Large parameter space to be explored
- We probe two questions in these slides
  - Q1: do we need a very fast 2nd layer or 8 – 10μs time res. is enough?
  - Q2: a more precise (but slower) innermost layer is beneficial for IP resolution. What's the impact on Ghost / bkg tracks rate & CPU time / evt?
- Approach
  - Use new mini – vector tracking
  - Fast algorithm that provides satisfactory efficiency for low P_T tracks
    - Algorithm is under development but can cope at this stage with beam bkg
    - Next slide we summarise its performance
    - See AWLC 14 slides

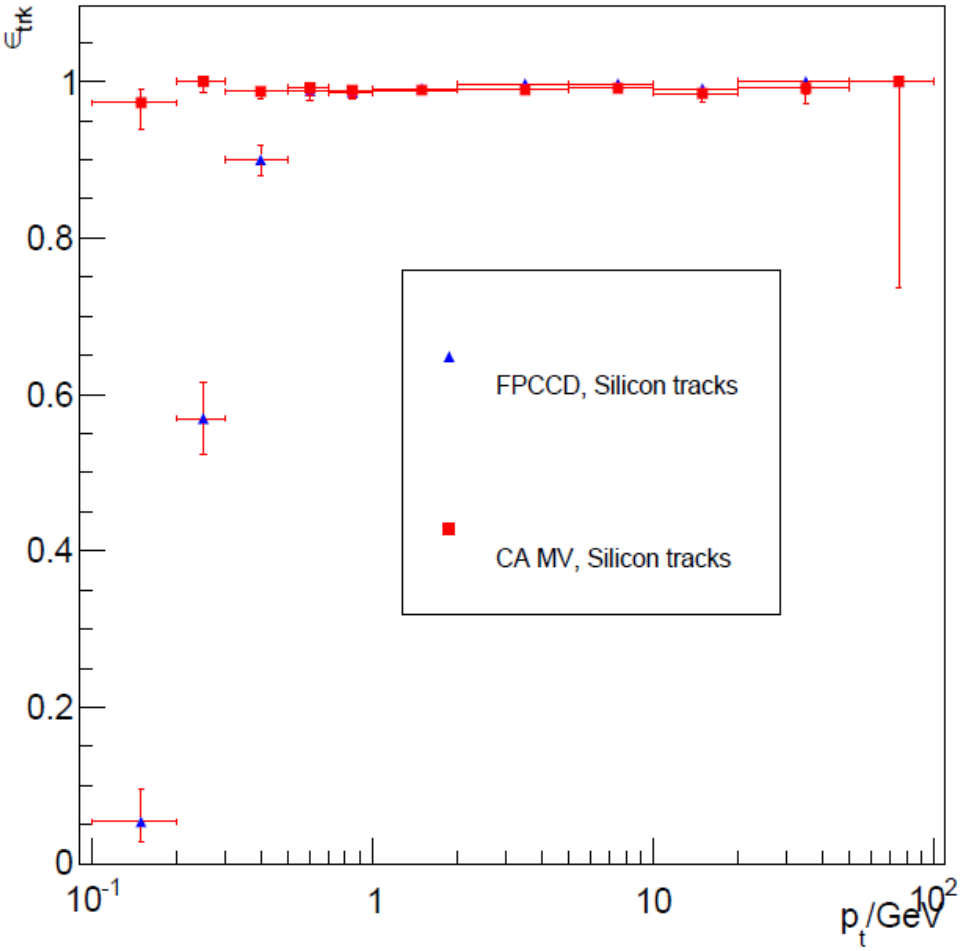
https://agenda.linearcollider.org/getFile.py/access?contribId=84&sessionId=17&resId=0&materialId=slides&confId=6301

New Mini – Vector Algorithm

Sample: ttbar, √s = 500 GeV, fast CMOS VXD, pair bkg overlayed, 120 events

- Ghost tracks / evt (P_T > 1 GeV)
  - FPCCD: ~ 10
  - CA: ~ 8
- Time / evt
  - FPCCD: ~ 75 s
  - CA: ~ 25 s

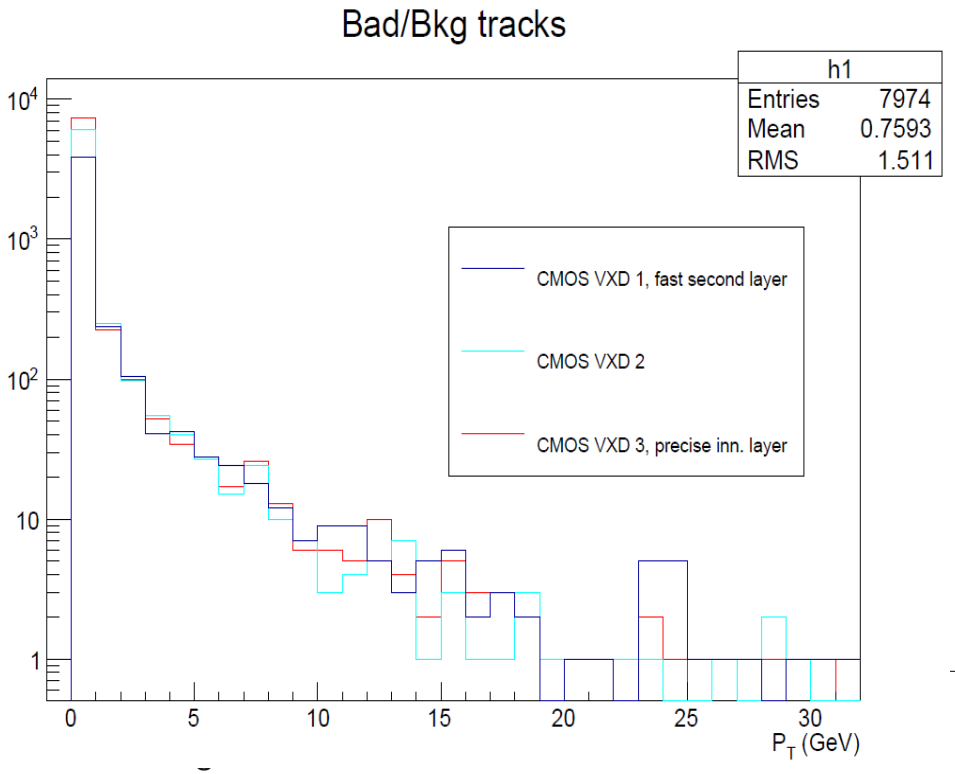




Tracking Perf. vs VXD Parameters

- Q1
  - A fast layer is quite helpful to bkg and / or ghost track suppresion
  - CMOS 1 with 2μs readout at L2 has lower “bad” tracks rate than CMOS 2, despite need to handle X4 more hits in pattern rec.
- Q2
  - Very granular L1 crucial for IP resolution
  - Seems better to combine with very fast L2
    - Reduce “bad” tracks, CPU time
- Various other questions need to be addressed

	CMOS 1	CMOS2	CMOS3
Hits (x103)	~120	~30	~100
Bad trks/ evt	~56	~84	~100
Time / evt (s)	~25	~5	~100



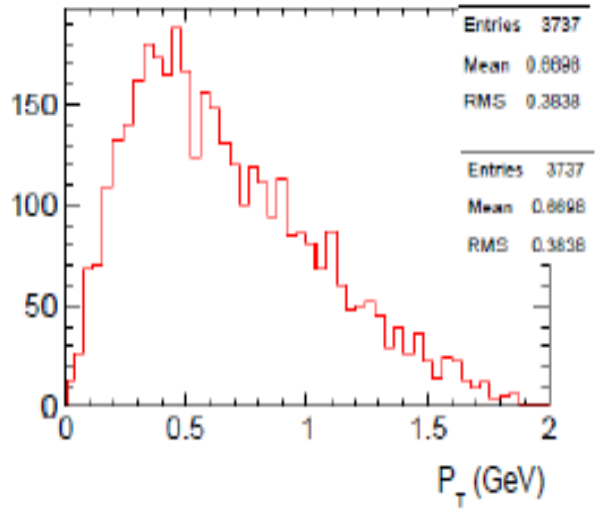
Proposed Physics Studies – Flavour Tagging

- Tracking studies are good but one needs physic studies to draw more solid conclusions
- VXD main goals
  - Flavour tagging
  - Reconstruction of low momentum tracks
- Flavour tagging
  - B – tagging rather trivial
  - C – tagging will drive the VXD specifications
  - Study of c – tagging performances in the presence of beam bkg
    - Flavour tagging neural nets need to be trained with beam bkg
    - Study of Higgs hadronic branching fractions

Proposed Physics Studies – Low Momentum Tracks

- Mini – vector tracking + fast detector provide satisfactory efficiency down to ~ 100 MeV
- The price to pay: reconstruction of pair bkg tracks as well
  - Can be suppressed by optimising some VXD layers for speed
  - But how fast we should go?
  - A study demanding on low mom. tracks can point up to which bkg track rate we can cope
  - Possible candidates
    - Light Higgsinos
      - Studied by Hale Sert
    - Vertex charge
      - Forward – backward asymmetry of $e^+ e^-$ → ttbar, in hadronic channel

$$e^+e^- \to \tilde{\chi}_1^+\tilde{\chi}_1^-\gamma \to 2\tilde{\chi}_1^0\gamma\ W^*W^*$$
$$e^+e^- \to \tilde{\chi}_1^0\tilde{\chi}_2^0\gamma \to 2\tilde{\chi}_1^0\gamma\ Z^*$$
$$\to 2\tilde{\chi}_1^0\gamma\ \gamma$$



P_T distribution of stable and charged MC particles ($\cos\theta < 0.9397$)

Summary – Outlook

- One can reduce the granularity in outer layers (to gain in speed and power dissipation) w/o penalising the IP resolution
- The above doesn't hold true for the innermost layer
  - More concrete conclusions on spatial – time resolution trade off can be drawn by a c – tagging study, where beam bkg is taking into account for neural nets training
- Mini – vectors help increase the tracking efficiency for low P_T tracks
  - But also the bkg / “bad” tracks
  - A fast VXD layer can help to better control bkg – ghost tracks
  - Light Higgsinos or vertex charge studies could be ideal to point uo to which bkg track rate we can live with
    - Thus the needs for time resolution