Status report on the development of a TPC readout system based on the SALTRO-16 chip and future plans

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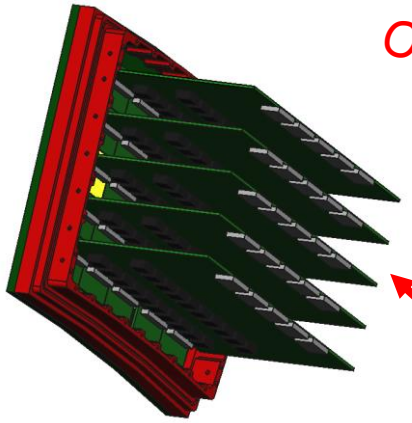
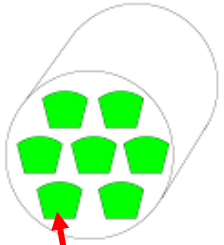
Status of electronics development

Overview of the SALTRO16 readout system

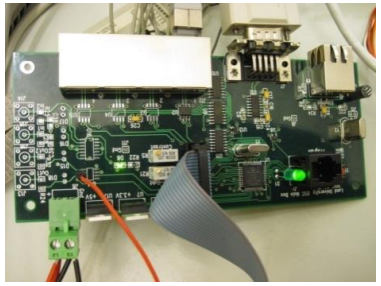


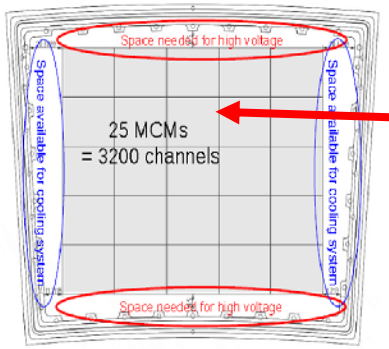
LowVoltage boards attached to one pad module



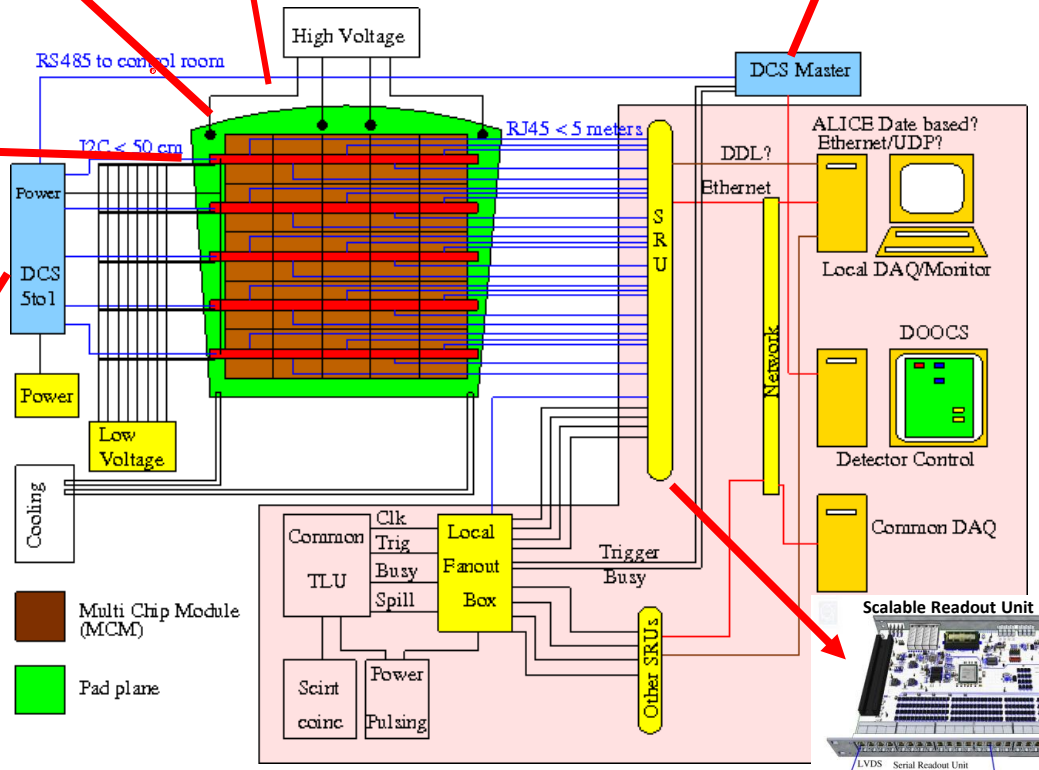
The Large Prototype TPC

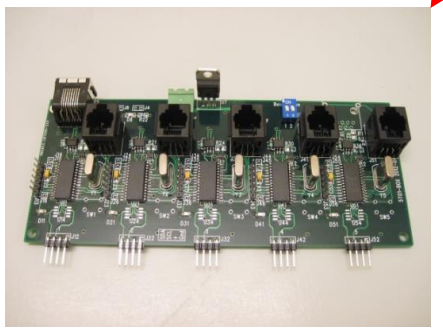
Detector Control System – Master module





MultiChipModules on a pad module





Detector Control System – 5to1 slave module

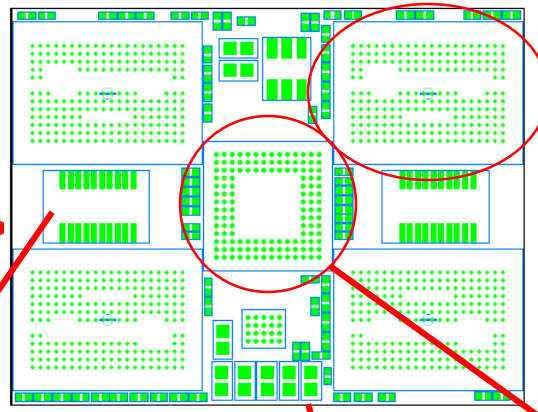
From ALTRO to SALTRO16
A decrease in size by a factor 40 of the front end electronics

FEC with 8 ALTRO

17 cm

19 cm

MCM with 8 SALTRO on carrier boards

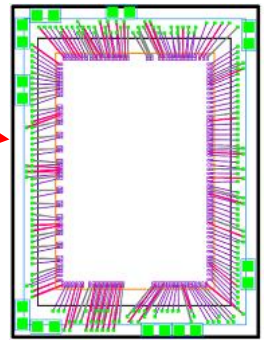


25 mm

32.5 mm

CPLD

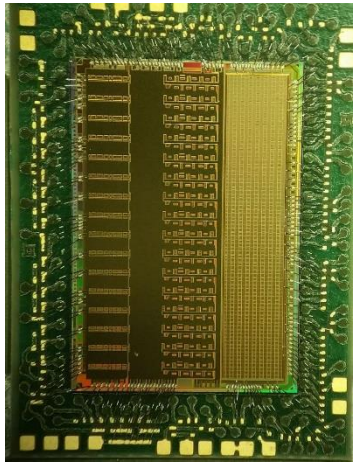
Carrier Board



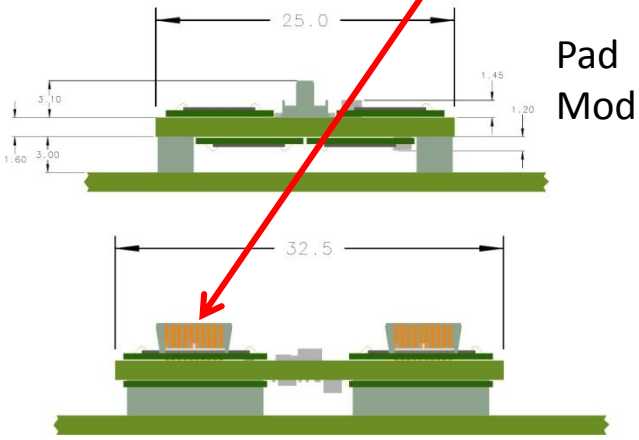
12 mm

8.9 mm

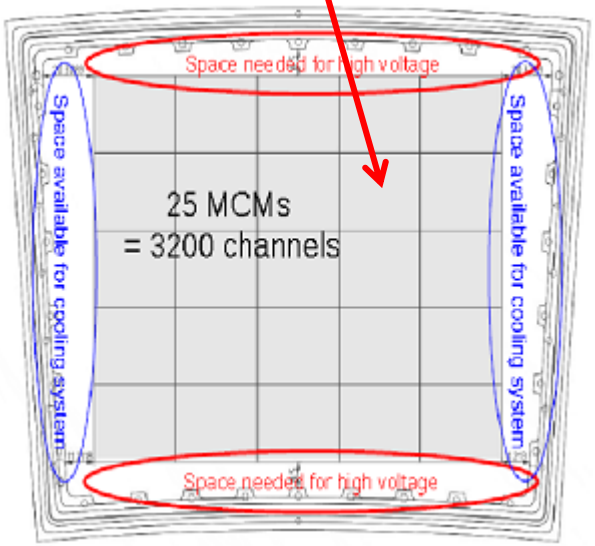
Carrier Board with SALTRO



Side views of an MCM



Pad Module



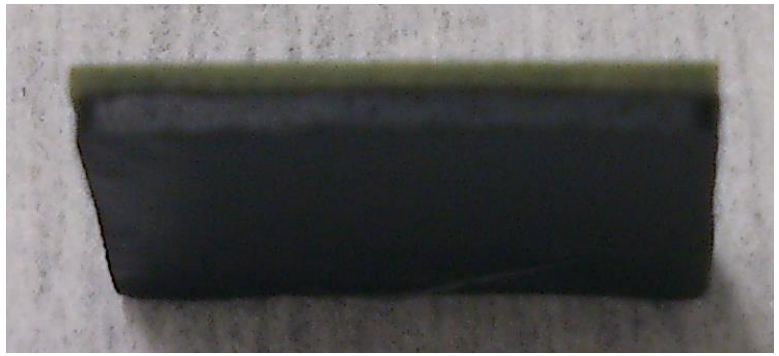
Tests of Carrier Boards

The preparation for tests of a carrier board include the following steps:

- Place the carrier board in the test socket, in which it fits very precisely, so that the sensor pins are directed towards the tin balls on the bottom side of the board.
- A fairly big force must be applied to the top surface to make sure that all pins make electrical contact to the balls.
- This require a certain flatness of the epoxy layer, applied to the top side of the carrier board.
- We might be forced to introduce some elastic material to distrbute the force more evenly over the full surface.
- Test will be made with a globbed dummy carrier board.

- An unmounted carrier board with shorted top surface will be used to test the connections of the test system

Globbing tests



Best globbing procedure so far:
Fill the mould with epoxy of low viscosity in the bottom, fill up with epoxy of high viscosity and then let it harden.
⇒ Flatness better than 0.2 mm

It has already been established that the globbed boards fit into the test socket.

Next step:
One board with shorted top side and one board with mounted SALTRO-chip has been sent for application of tin balls on the bottom side.
The board with shorted top side will be used to test whether connection to all test pins can be accomplished and whether the epoxy layer can stand the force applied.
If this is the case then the board with the SALTRO-chip will tested for the functionality of the carrier board

Next globbing test;
Let the first layer of epoxy harden before the mould is topped up with low viscosity epoxy

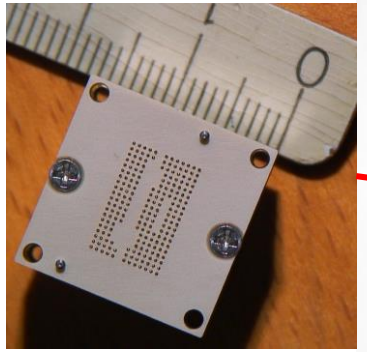
Three Carrier Boards with bonded chips have been produced.
As soon as the flatness of the epoxy surface is satisfactory:

- The next step is to test the three mounted Carrier Boards to investigate the performance of the Carrier+SALTRO.
- If ok bonding of the remaining SALTRO-chip and testing (Financial support for this is needed).
- If not ok another iteration of the Carrier Board design.

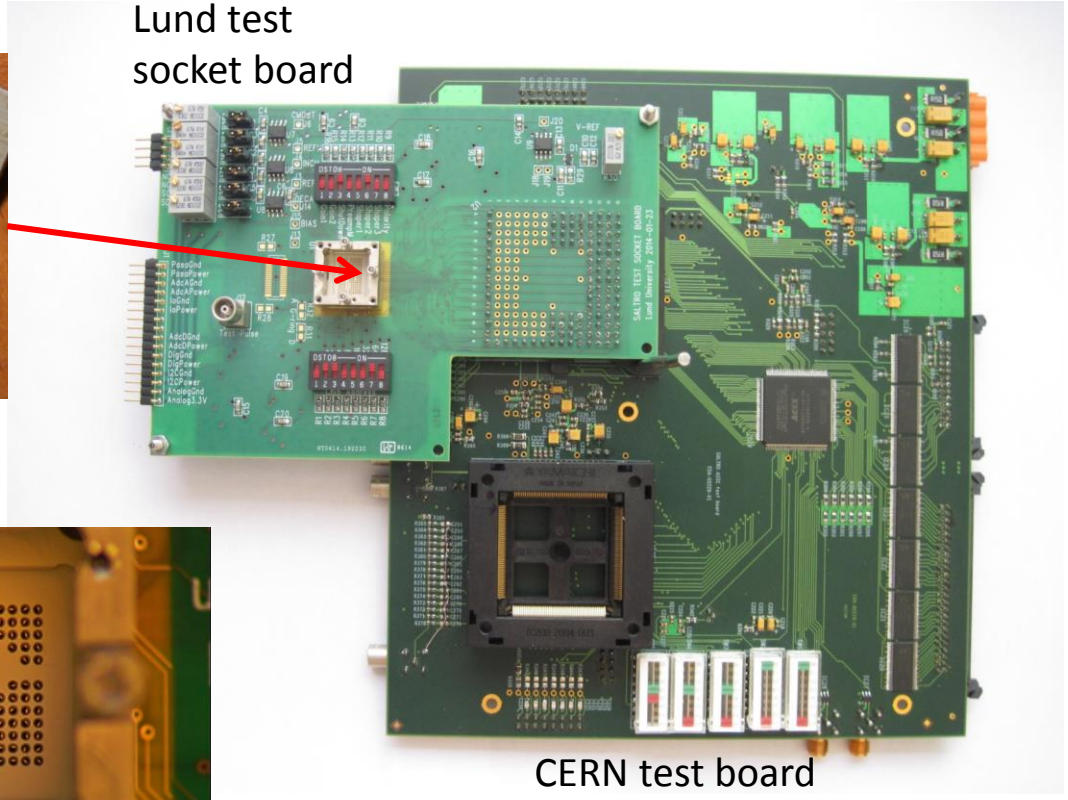
Test set-up for testing SALTRO16-chips on Carrier Boards

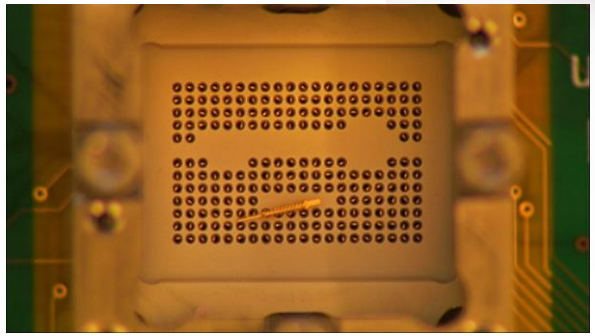
- The test set-up for testing SALTRO-chip mounted on Carrier Boards is assembled and we are ready to start testing.

Test socket

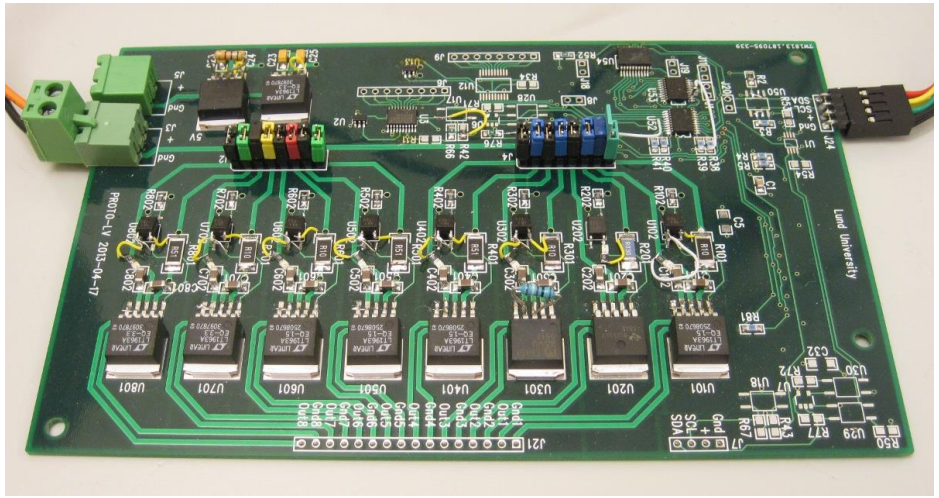


Lund test socket board



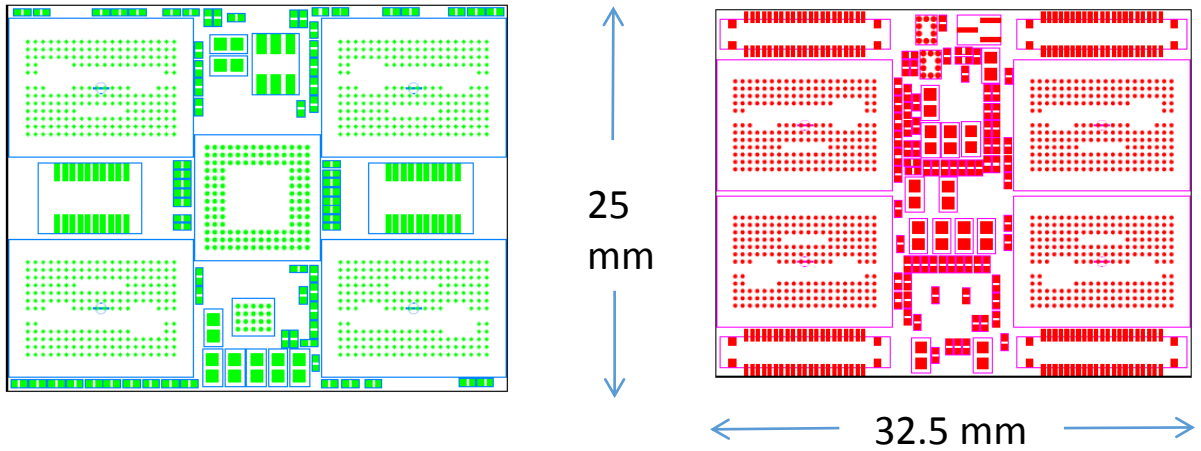


CERN test board

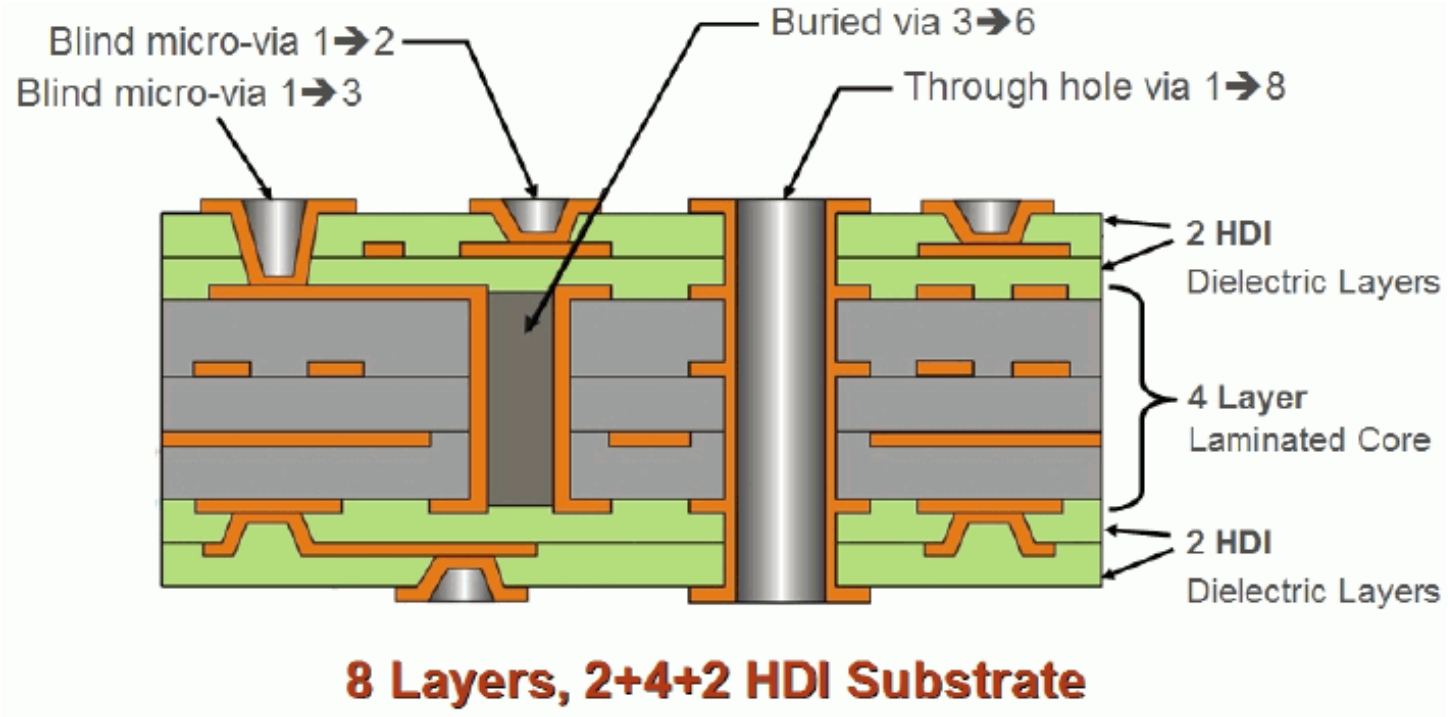


LV-prototype board

The MCM-board and HDI (High Denisty Interconnect) technology



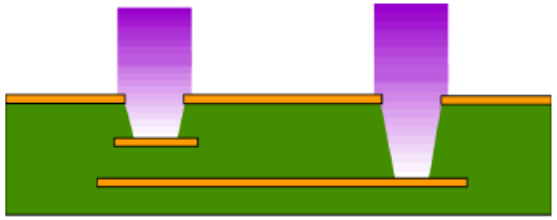
The MCM-board will be redesigned in HDI technology



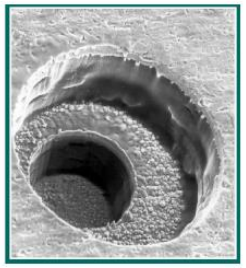
- The core is a standard multilayer PCB.
- Onto this a thin prepreg layer (dielectrica +copper) is laminated.
- This is etched, laser drilled and plated.
- This procedure can then be repeated such that a thin multilayer board is constructed on top of the regular PCB.

Advantages of HDI (1)

- Routing density higher both for signal and voltage supply ⇒ number of layers can be decreased
- Laser drilling allows for a holes as small as 25 μm diameter with collars of 50 μm.
- The drilling can be performed to different depths depending on the energy in the laser beam.



Single level via

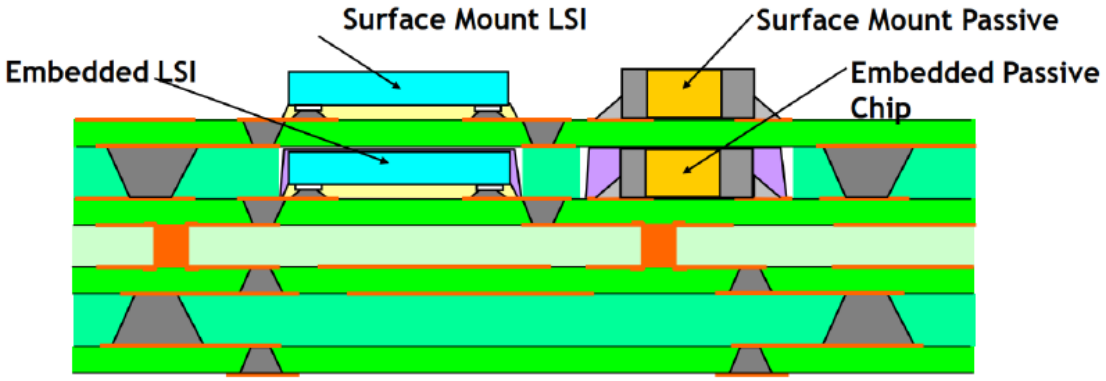


Stepped via

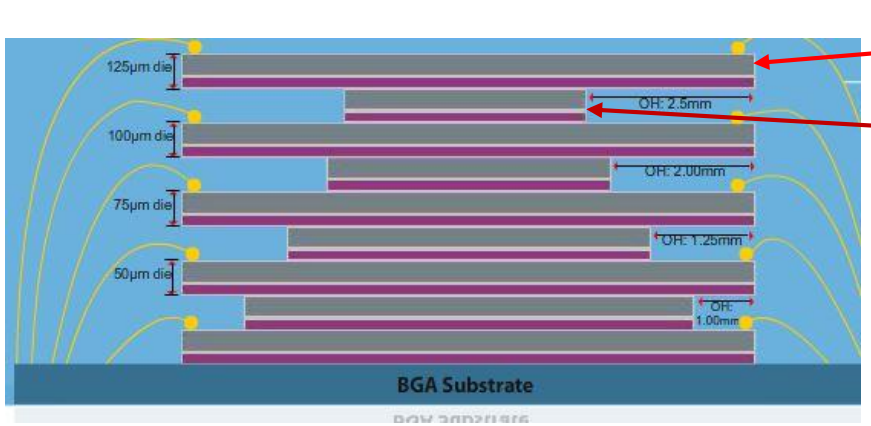
- Together with sequencial laminate application vias can connect different layers.
- The prepreg layers can be as thin as 5 μm.
- Due to via-in-pad techniqies all routing can be performed in the inner layers such that essentially the whole surface can be used for mounting of components.

Advantages of HDI (2)

This technology also offers the possibility to create cavities in the PCB where electronic och mechanical components can be mounted and thus embedded into the PCB so that essentially the full surface is available for surface mounting of chips.



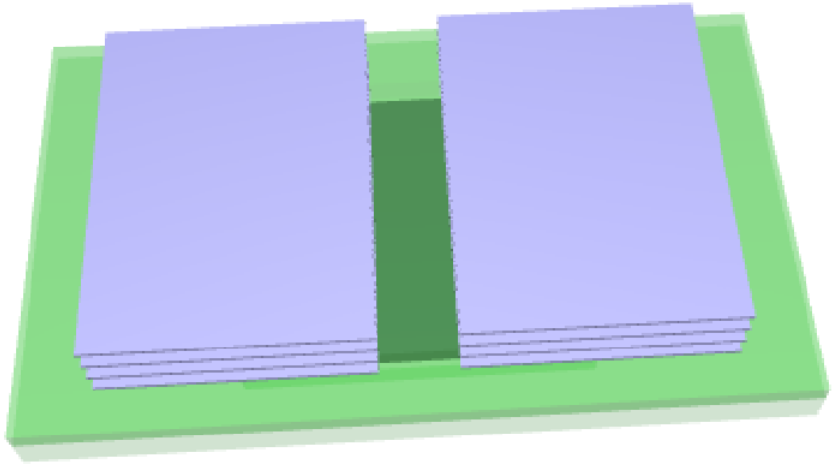
Chips mounted on small carrier board in 3D technology, where the carrier boards are soldered on a hybrid board, which in turn connects to the pad plane.



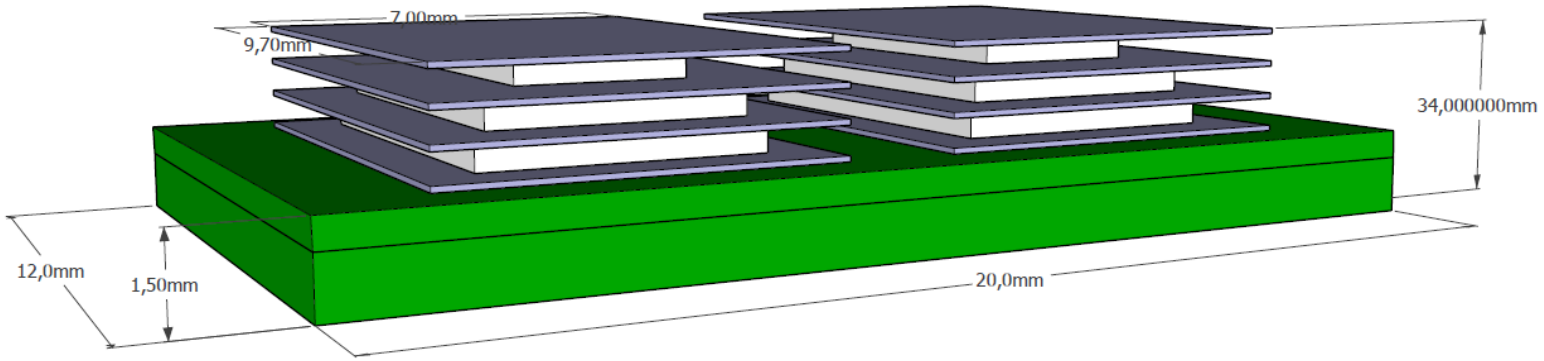
Die

Ceramic substrate

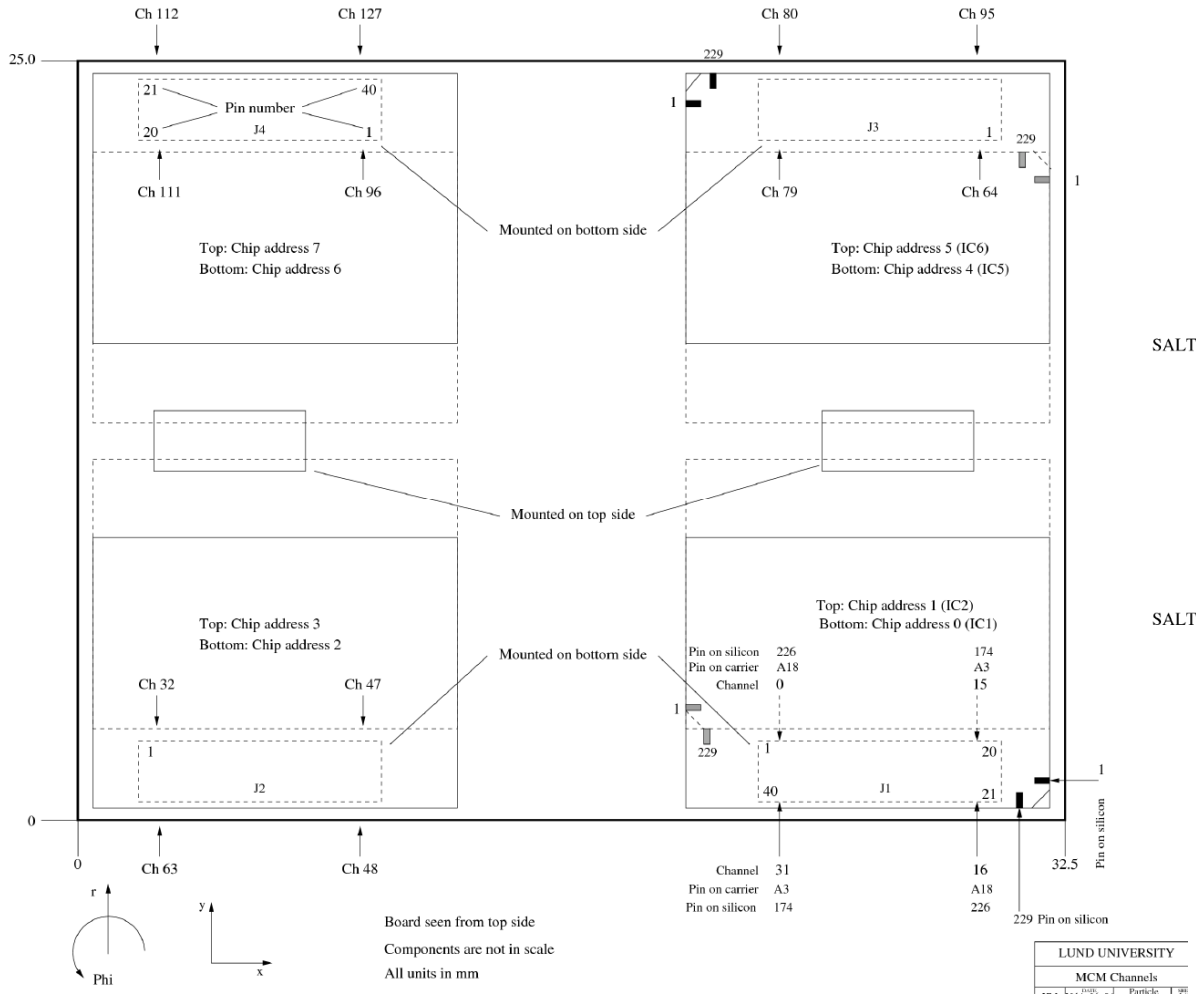
Conceptual layout of an hybrid-board mit 2x4 stacked SALTRO-dies

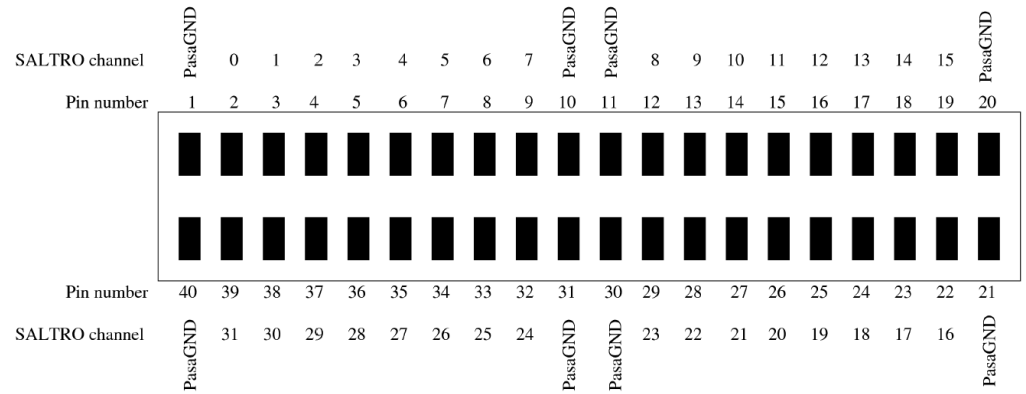


- The hybrid HDI-board has a size of 20.0 x 12.0 mm^2
$\Rightarrow$ less than 2 mm^2 per channel.
- The hybrid board contains a CPLD, DAC and other components burried in the prepreg.
- 4 hybrid boards can be mounted on an MCM-board, which will contain 512 channels (compared to 128 with the present system)
- The MCM-board will contain the analogue electronics and a fast seriell connector
- The MCM-boars will be free from components on the bottom surface and can thus either be soldered directly against the pad plane or alternatively it provides more space for connectors



Positioning of the Panasonic connectors on the MCM-board





For more details see: http://www.hep.lu.se/eudet/saltro/numbering-20140603.pdf

Future work

- Production of a mock-up system with dummy Carrier-, MCM- and adaptor boards to verify the soldering procedure and check that the various parts fit together.
  For this we need a dummy Padplane and a dummy carrier-, MCM boards as well as an adaptor-board
  Production of the latter ones can be realized in a short time.

- The final MCM-board will be redesigned in HDI-technology.

- As soon as the mechanical support structure and the layout of the cooling pipes is fixed the design of the LV-board can be finished.

- Modification of the firmware for the CPLD and the SRU and further tests of the DAQ communication.
  - Packaged SALTRO-chips have been mounted on three MCM-prototypeboards.
  - The communication SALTRO – CPLD – SRU has been tested in Brussels.
  - Identical systems will be built up in Brussels, Wuhan and Lund for an efficient development of the DAQ firmware, which will be an Ethernet based DAQ-system and allow for common DAQ integration.
  - A Linux PC has been installed in Wuhan and the development for the communication between the Graphical User Interface – PC server – SRU – SALTRO has started.
  - This week Yifan is in China and will together with Fan try to establish the full communication. So far they have managed to read events from the prototype MCM.

- DOOCS: The layout of the DOOCS implementation and hardware communication have been agreed upon together with Oliver Schäfer, who has agreed to perform the main part of the work.

What have we learned so far and what is the situation we have to deal with?

- The SALTRO-chip is not an ideal solution but required many cumbersome compromises in the PCB-design
  - -too many connectors to interconnect the various subsystems
  - -too many voltage levels → bulky voltage supply
  - -too many functions set external (gain, shaping time, decay time etc.)
  - -bulky cooling system

- Design of a new chip:
  - - the new chip should have ≥ 64 channels
  - - lower power consumption with fewer voltage levels
  - - integrate functions that are now provided externally
  - - should have a fast serial bus

- However, a new chip will most certainly not be available for some years yet

⇒ We have to live with the SALTRO16-chip for another few years

- 3D mounting of SALTRO-chips may help to achieve the required channel density corresponding to a pad size of few square millimeters

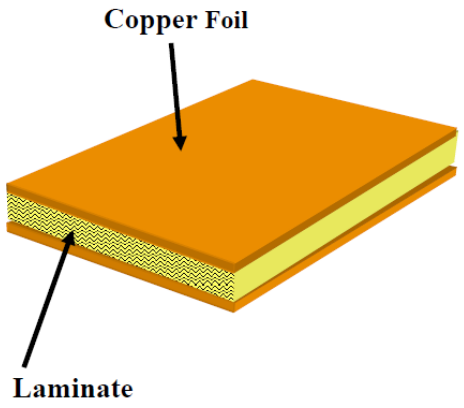
- However, the sampling depth is not sufficient to cope with the drift length of the final TPC.

Ideas on pad planes with intergrated cooling

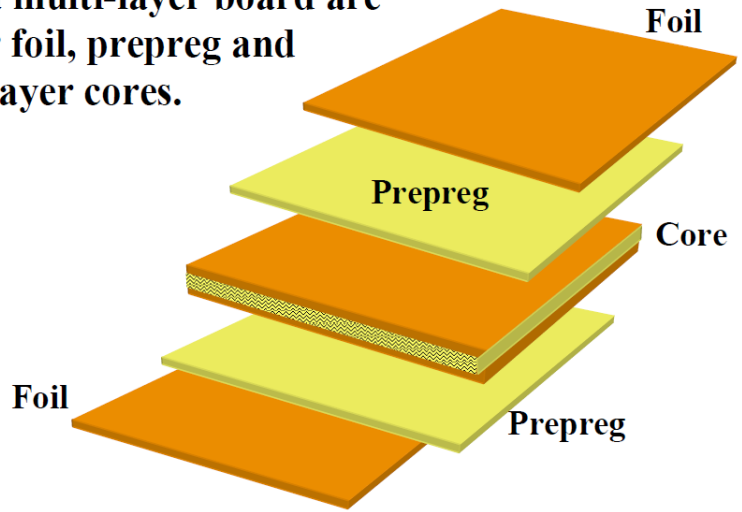
The principle layout of the multi layer board

- A multi layer PCB is produced by stacking a number of core layers and pre-preg layers.
- A core layer is a thin dielectric consisting of cured fibre glass epoxy resin, with copper foil bonded to both sides.
- A pre-preg layer is a thin sheet of fibre glass, impregnated with uncured epoxy resin, which hardens when heated and pressed in the PCB fabrication process.
- Pre-pregs can be stacked to achieve the desired thickness.
- The difference between core and prepreg layer lies in the roughness of the fibre material and what epoxy material being used.

Multi-layer fabrication begins with the selection of an inner layer core – or thin laminate material of the proper thickness. Cores can vary from 0.038" to 0.005" thick and the number of cores used will depend upon the board's design.

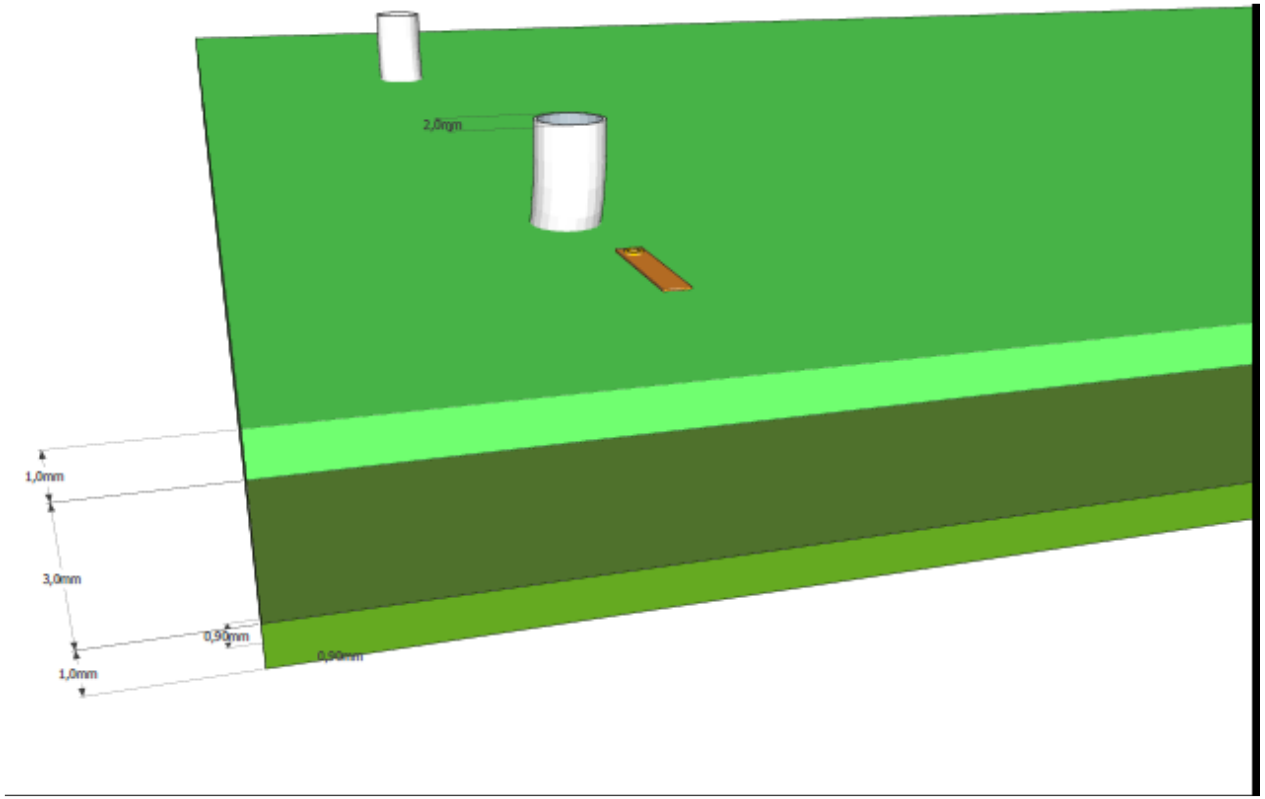


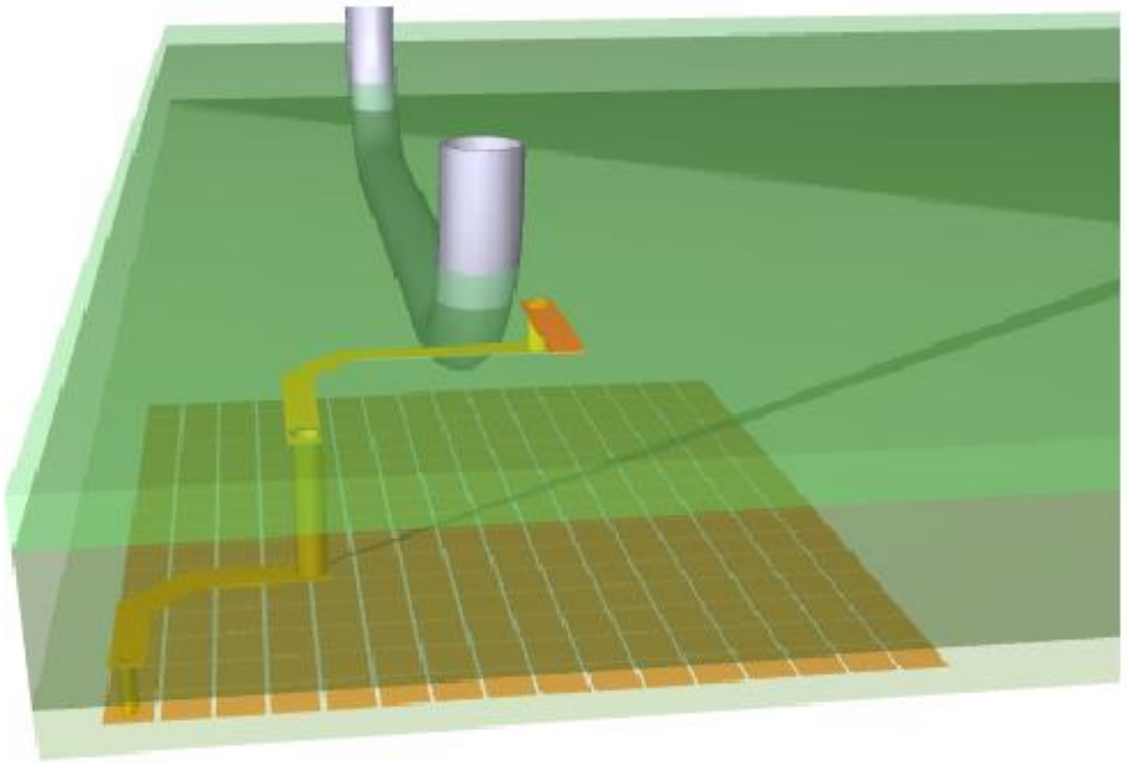
The basic materials needed to build a multi-layer board are copper foil, prepreg and inner-layer cores.



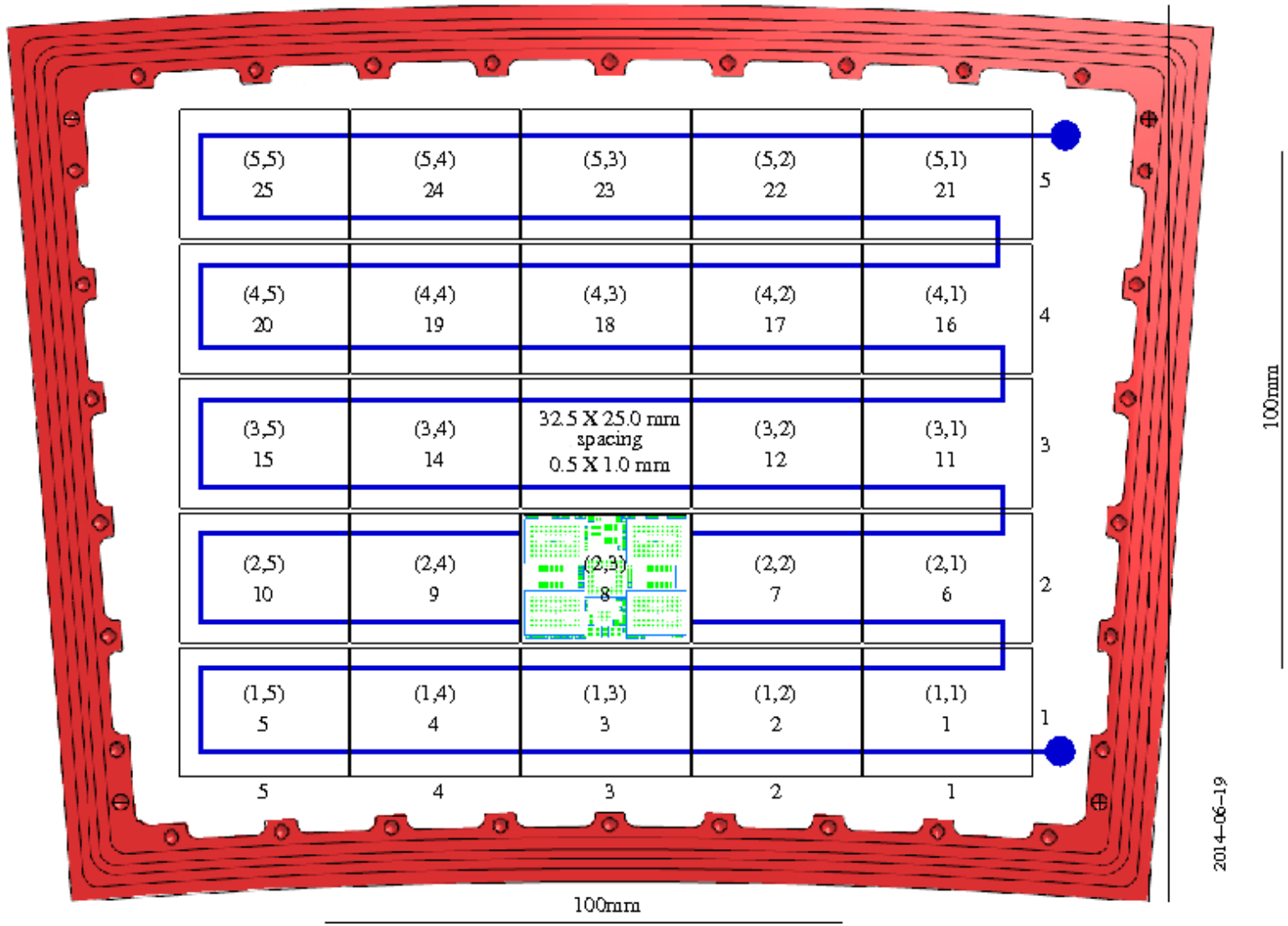
Integration of the cooling pipes in the PCB

- The cooling pipes can be integrated in a prepreg layer of sufficient thinkness.
- In this case the prepreg has to cure before stacking in order to allow for machining.
- After the cooling pipes have been inserted a thin laminate is added on top.
- All further layers have to be machined before stacking.





A possible layout of the cooling pipes



Summary

- We are ready to start the testing procedure
- The redesign of the MCM-board in HDI technology will start after the vacation
- We need help with:
  - Producing a dummy pad plane
  - Financing to mount the bulk of SALTRO-chips onto the Carrier Boards
  - Designing the layout of the cooling pipes

- We have presented new ideas on:
  - 3D mounting of chips to meet the pad size required
  - Integrated cooling in the pad plane