FNAL ILC LLRF Controls and Fast Tuner R&D Status

Ruben Carcagno, Brian Chase, Gustavo Cancelo,
Yuriy Pischalnikov
(on behalf of the FNAL LLRF Working Group)
8/31/06

Outline

- FNAL ILC LLRF Control Task Status (Ruben Carcagno)
- CC2 Piezo Tuner Results (Yuriy Pischalnikov)
- Status of LLRF activities at FNAL-CD (Gustavo Cancelo, if time allows)

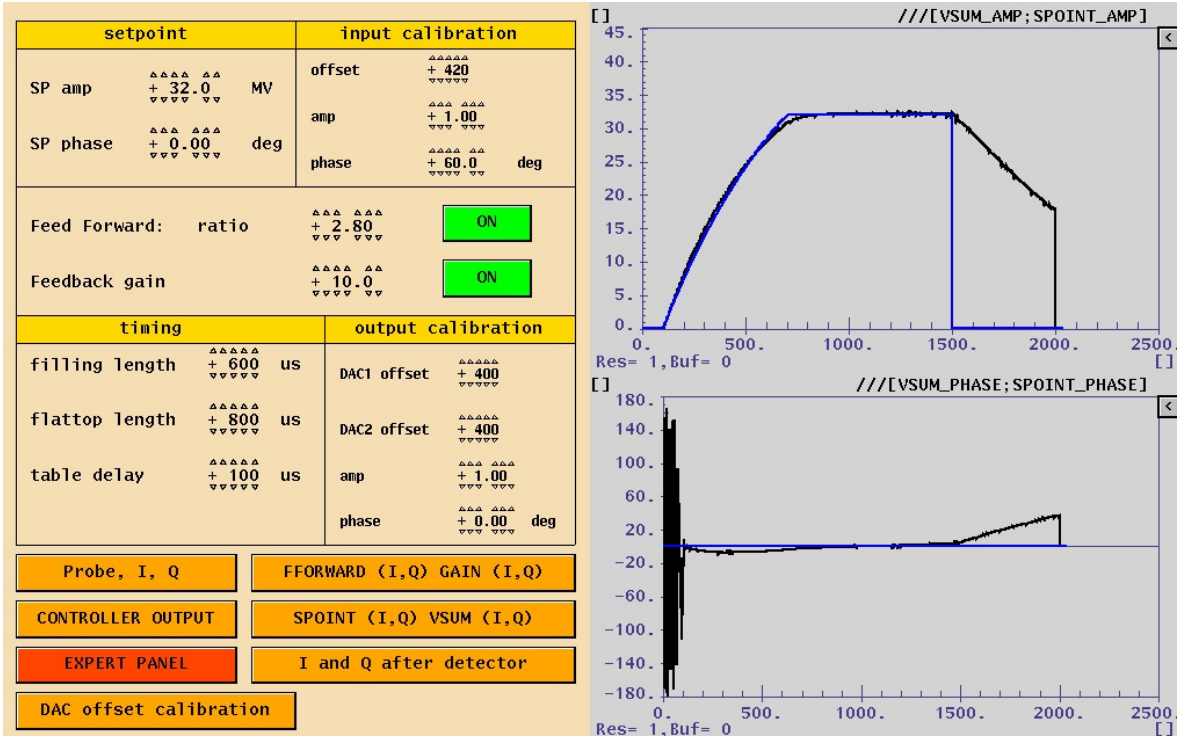
ILC Americas
WBS 5.8.4: LLRF Controls

- **Motivation**
  - To develop LLRF systems for ILCTA and work towards an ILC LLRF system
- **Milestones and Deliverables**
  - Design and fabrication of the LLRF system for the Horizontal Test Stand (HTS) in the Meson Area (ILCTA_MDB) by May 2006
- **Status**
  - All milestones and deliverables have been met: a LLRF system was delivered ahead of schedule for ILCTA_MDB commissioning using the Capture Cavity 2 (CC2), and the system is ready to support the HTS when needed

WBS 5.8.4: LLRF Controls
ILCTA_MDB LLRF System

- Based on the latest DESY's FPGA-based controller VME card, Simcon 3.1
- Successfully supported the first CC2 test on March 2006
- Result of a strong collaboration with DESY which started on FY2005 and continued into FY2006
- System was first fully tested and fine-tuned using Fermilab's Capture Cavity 1 (CC1) in the A0 photoinjector area: good confidence about the performance of this system to support ILCTA_MDB commissioning with CC2
- Other components delivered to ILTA_MDB
  - A new Fermilab designed and built programmable muti-frequency, low-noise Master Oscillator (MO)
  - A new Fermilab designed and built Downconverter and Vector Modulator, and a 3.9 GHz up/down converter
  - A Fermilab built fast piezo tuner assembly instrumented with a novel method developed at Fermilab to continuously monitor piezo preload forces together with the associated electronics to monitor and control this device
- In parallel, a second LLRF system based on a modified SNS LLRF system for 1.3 GHz operation was also developed in collaboration with the SNS LLRF team and was ready as a contingency for ILCTA_MDB.

WBS 5.8.4: LLRF Controls
ILCTA_MDB LLRF System: CC2 Results



From J. Branlard (8/29/06)

-Fill time: 600 µs

-Flat top: 800 µs

-Gradient: 29.7 MV/m

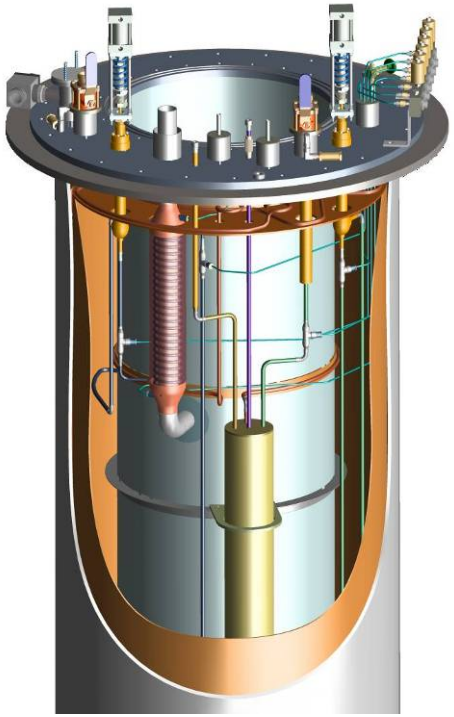
-Feedback Gain: 12

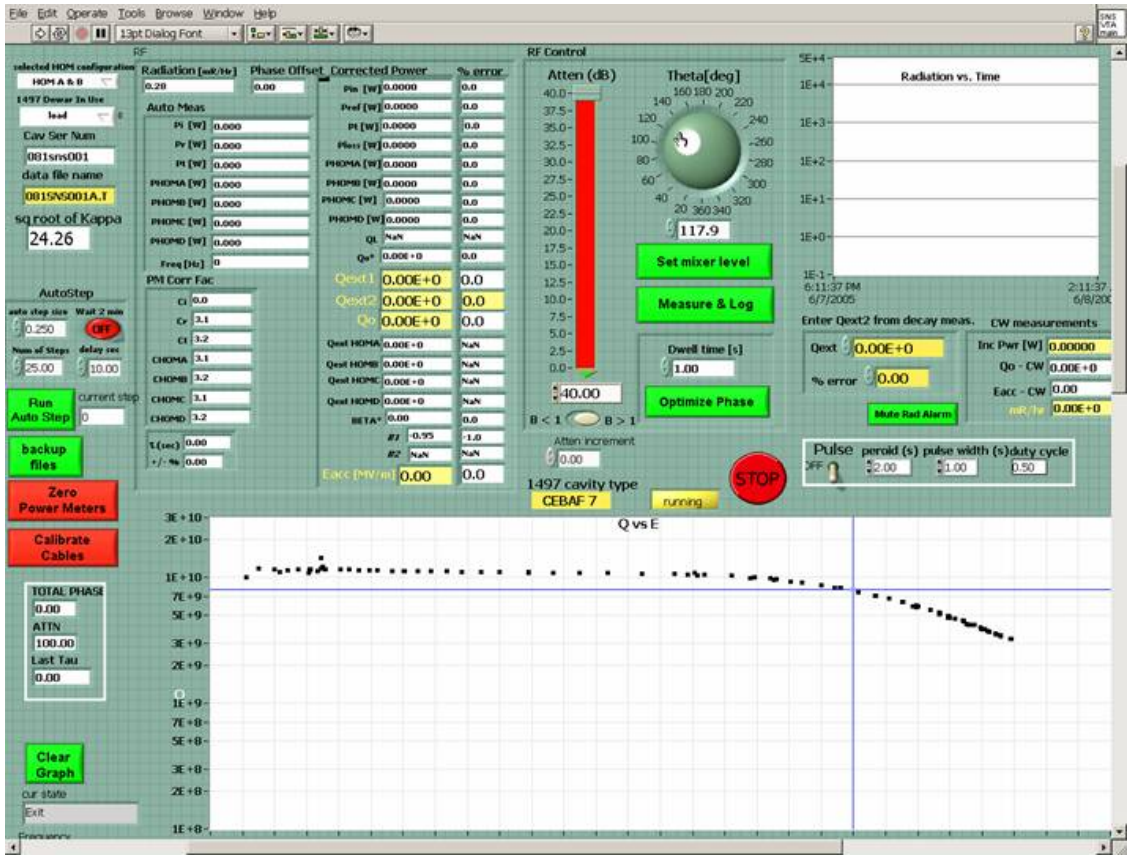
Working to understand excessive microphonics noise source and mitigate (more on this during piezo presentation)

WBS 5.8.4: LLRF Controls
ILCTA_IB1_VTS LLRF System

- Design completed by Joe Ozelis (FNAL), Roger Nehring (FNAL), and Tom Powers (Jlab)
- Design reviewed on 8/24/06 (Review Chair: Ralph Pasquinelli)
- Based on proven JLab's VTS VCO/PLL system (with improvements)
- Collaboration with Jlab established (Tom Powers, Christiana Grenoble)
  - Jlab MOU addendum to pay for this help approved by FNAL ILC management and forwarded to Jlab for approval
- FNAL/Jlab team in place, procurements being placed, ready to start implementation phase
- Schedule: full system test with cold cavity by 4/30/07

WBS 5.8.4: LLRF Controls
ILCTA_IB1_VTS LLRF System





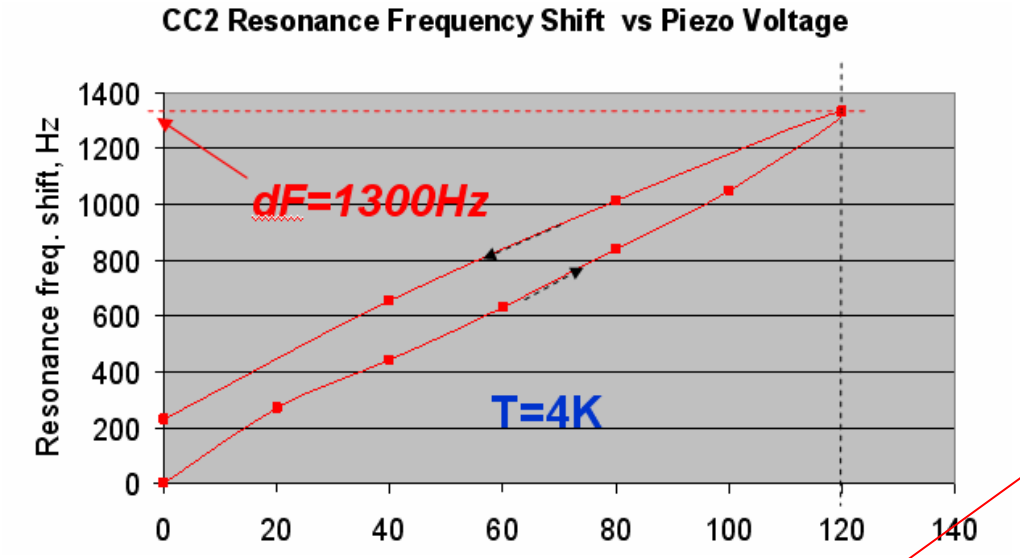
WBS 5.8.4: LLRF Controls
LLRF System R&D

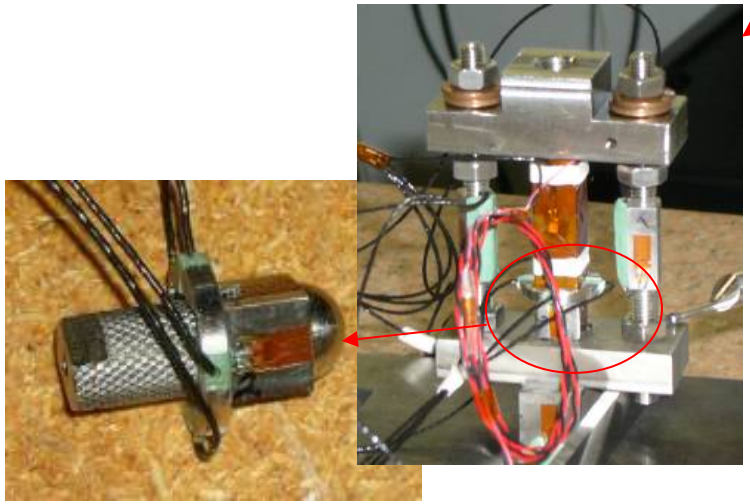
- **Simcon 3.1 board modifications to improve noise characteristics**
  - Purchasing parts to build prototype and manufacture six modified boards to populate ILCTA in FY07
- **Simcon 3.1 FPGA firmware developments for higher intermediate frequency (IF) capabilities (lower latency controller)**
  - Developed FNAL ability to modify and compile Simcon 3.1 firmware
- **Simcon 3.1 control System integration with DOOCS, EPICS, etc**
  - Developing EPICS interface
  - Developing generic "C++" driver to easily interface Simcon 3.1 to **any** control system (DOOCS, EPICS, Matlab, Labview, etc)
- **Feasibility of using commercial boards (Lyrtech) and high level FPGA programming (Matlab/Simulink/Sysgen) for LLRF applications**
  - Purchased a Lyrtech board and software, developed IQ detector block
- **Prototyping 32-channel in-house LLRF controller for an ILC RF unit**
  - Lower cost, higher density technology
- **UPenn collaboration: development of an ILC real-time RF unit simulator**

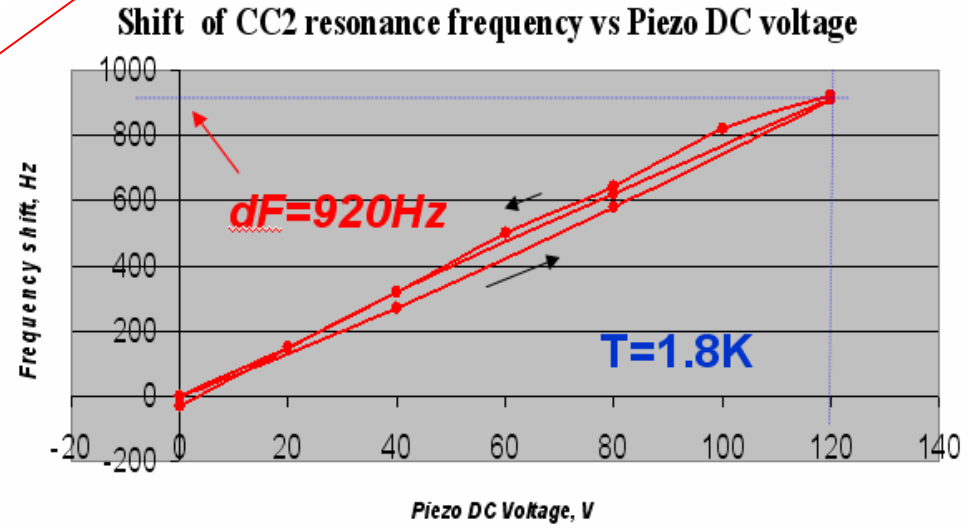
ILC Fast Tuner R&D Status

Yuriy Pischalnikov
(on behalf of the FNAL Fast Tuner Working Group)
8/31/06

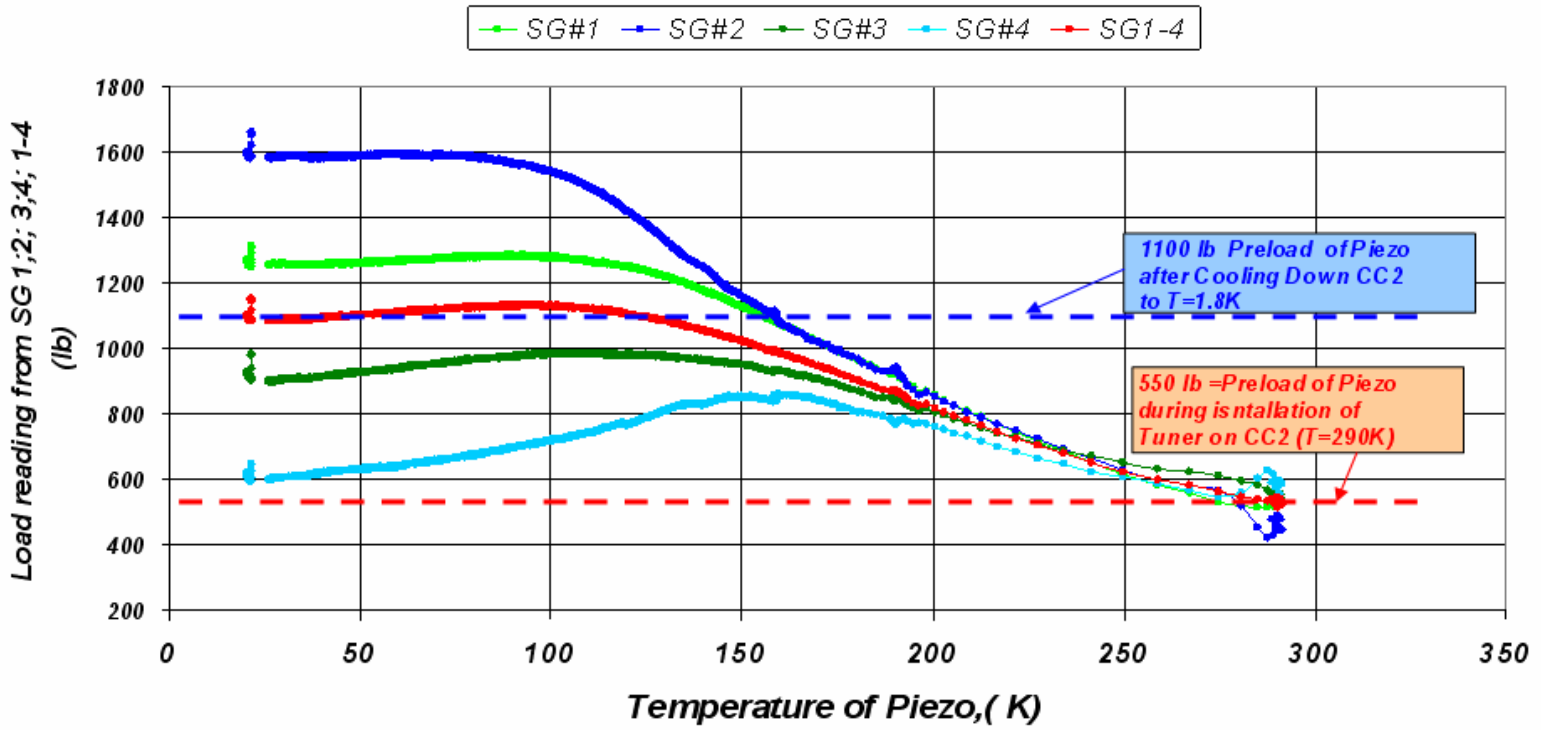
CC2 Piezo Tuner
(diagnostic instrumentation => 11SGs & 2RTD)

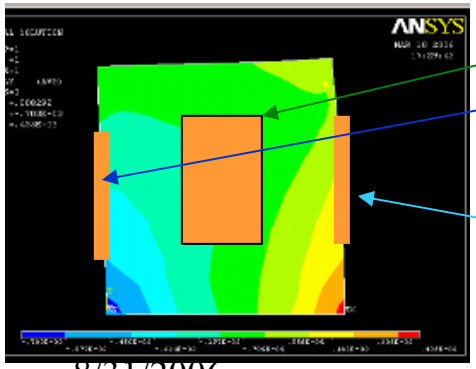




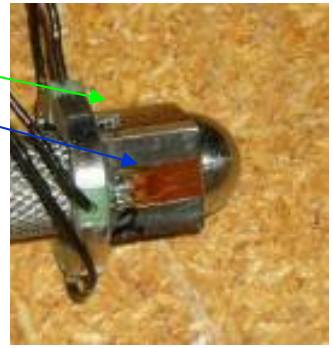


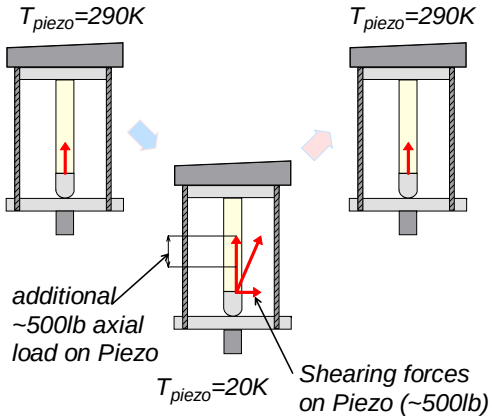
Preload on Piezoactuator during cooldown & warmup of CC2 (reading from bullet's SGs)



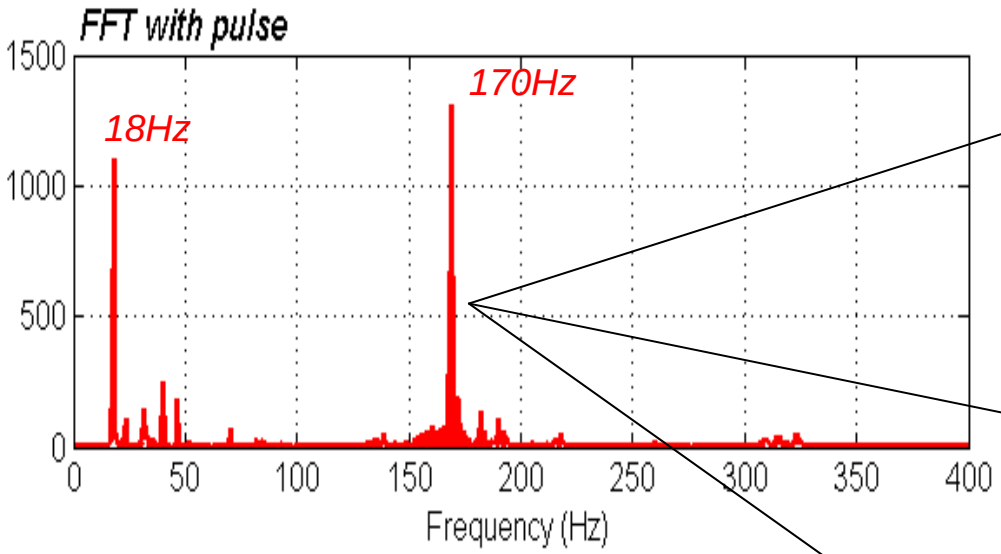


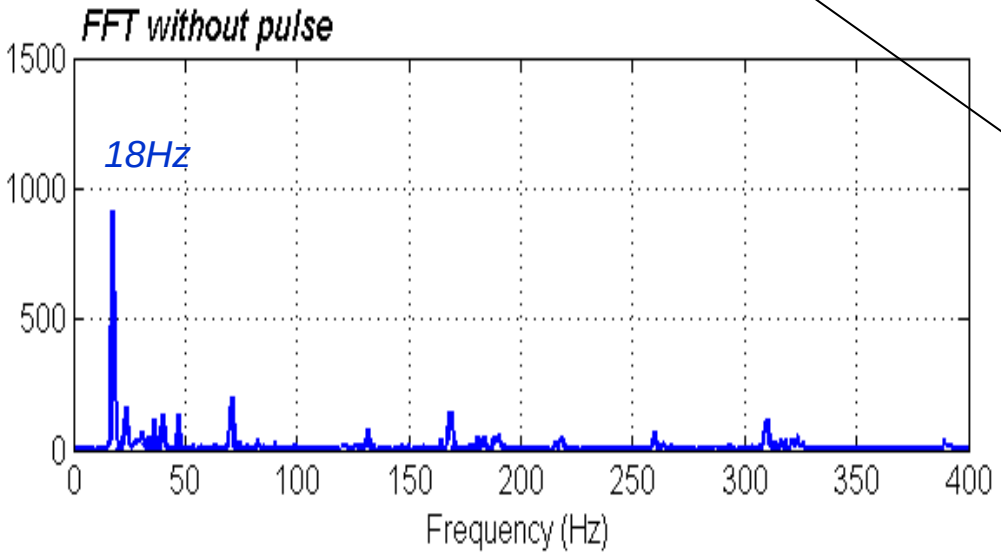
SG#1
SG#2
SG#3
SG#4



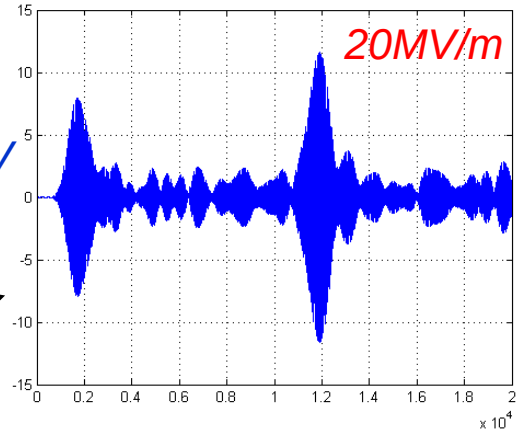


CC2 Microphonics measurements.
Pulse mode operation. Piezo => sensor.



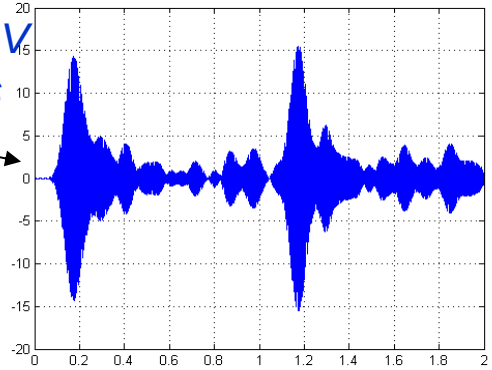


A=10mV
τ=0.17s

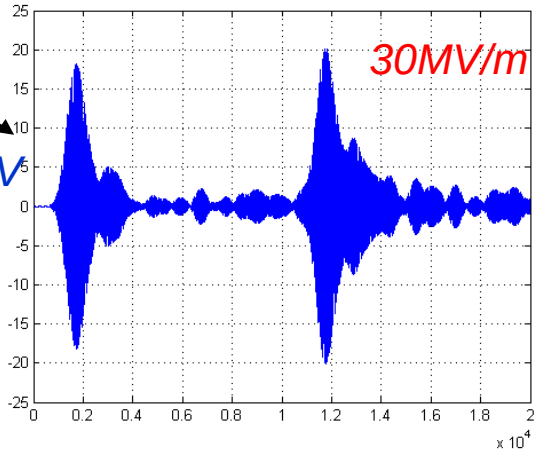


25MV/m

A=15mV
τ=0.12s

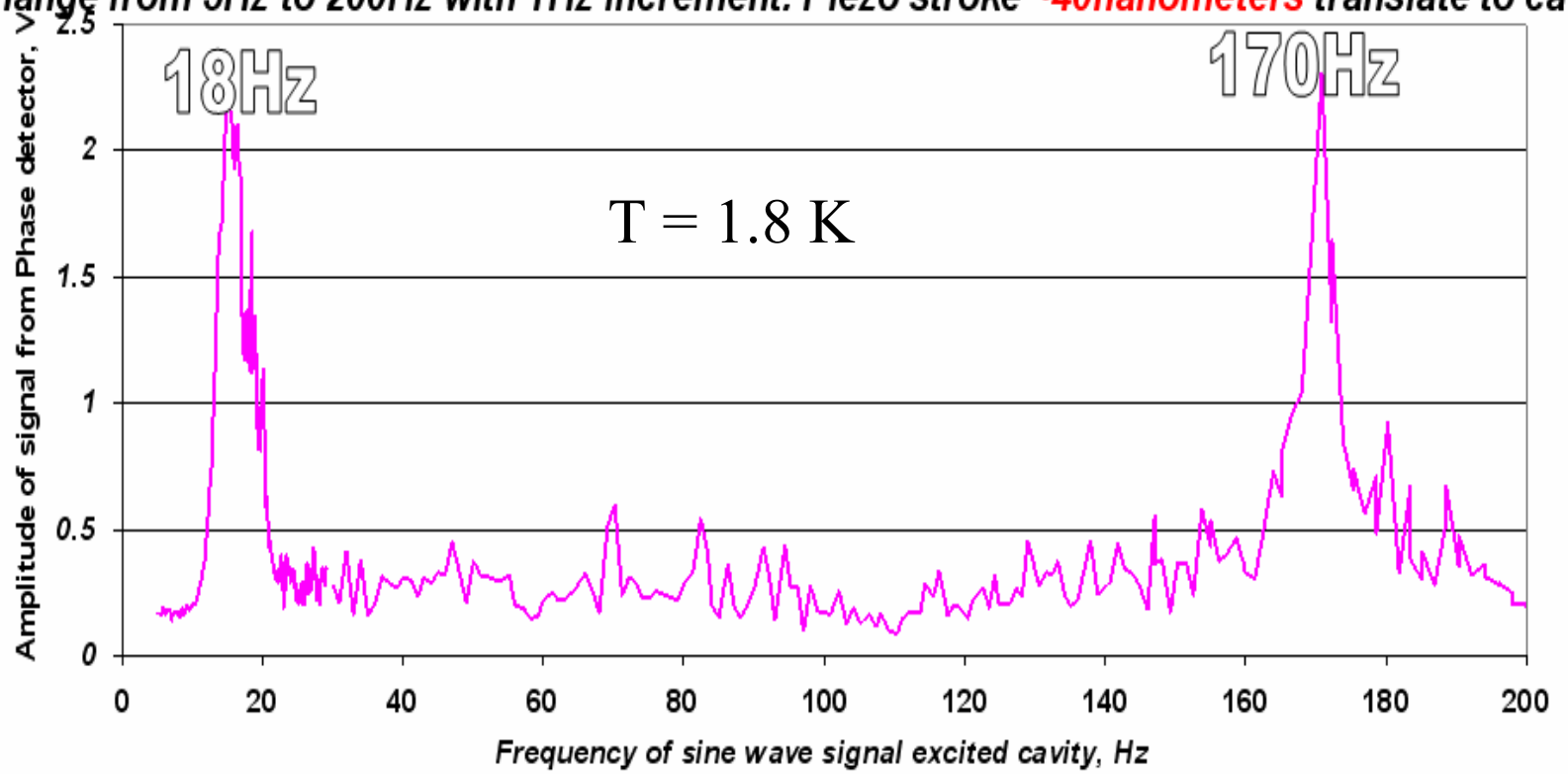


A=20mV
τ=0.10s



CC2 Transfer Function Measurements.
CC2 operation at CW mode. Piezo work as Actuator.

Piezoactuator driven by sinewave signal (amplitude pick-to-pick ~1.5V) Frequency of sinewave change from 5Hz to 200Hz with 1Hz increment. Piezo stroke ~40nanometers translate to cavity.



Status of LLRF activities at FNAL-CD

Gustavo Cancelo

ILC meeting

Thursday, August 31 2006

FNAL-CD Activity list and effort

- FNAL-LLRF controller hardware design.
  - 10 input, 4 output channels, 14 bits dynamic range, 125 Ms/s.
- Algorithm development and implementation for new LLRF controller.
  - Using high level tools such as Matlab/Simulink/System Generator.
- Cavity modeling and feedback control.
  - Some models implemented. We are interfacing with UPENN. More effort is needed to address the control problem.
- LLRF project management and FNAL collaboration.
  - Working in close collaboration with TD (Ruben Carcagno et al. and AD (Brian Chase et al.)
- Collaboration with other labs and universities.
  - Weekly TUE meeting 9am with DESY, KEK, UPENN, LBNL, ANL, SLAC and FNAL.
- CCII and ILCTA support.
  - This effort should increase in 07.

FNAL-CD Activity list and effort

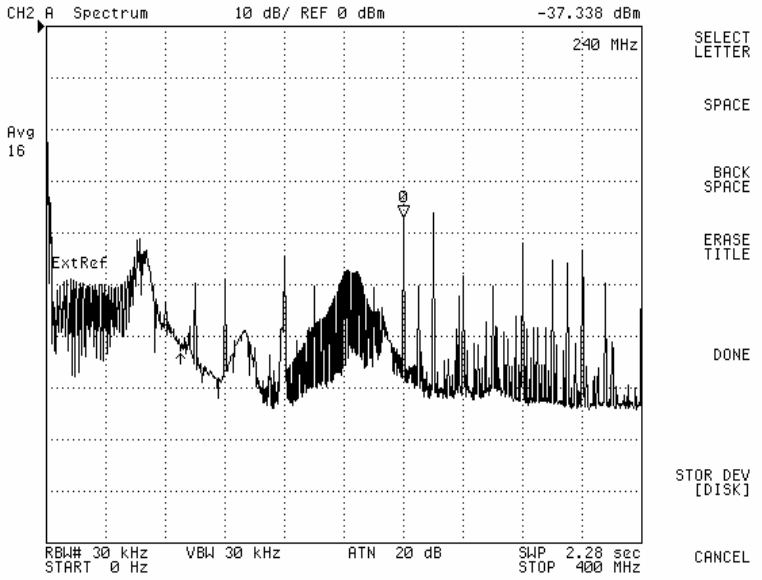
- Effort used in 2006 plus the estimated for the rest of the year:
  - 2.8 FTEs
- Effort requested for 2007:
  - Between 4.0 and 4.2 FTEs.
- List of names working for LLRF at CD:
  - Ken Treptow
  - Ted Zmuda
  - Rick Kwarciany
  - Bill Haynes
  - Neal Wilcer
  - Gustavo Cancelo

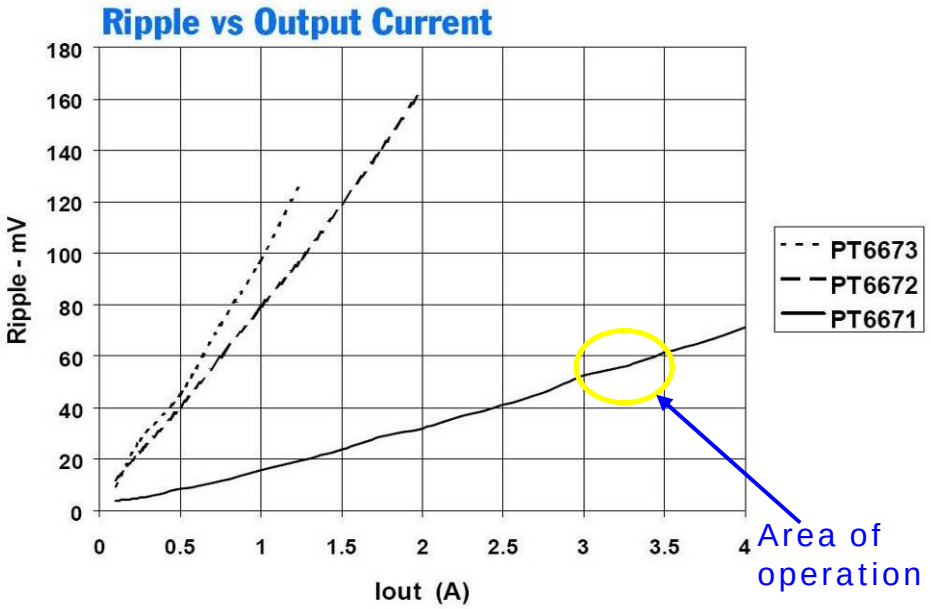
Motivation for designing a 10-channel LLRF controller at FNAL

- The LINAC is one of the main focus of R&D at Fermilab.
  - FNAL LLRF group needs to master the hardware and software design of LLRF components to meet the required specifications for ILCTA and ILC.
- We have worked in close collaboration with DESY
  - Operated and tested DESY LLRF controllers Simcon 2.1 and Simcon 3.1.
  - We currently use Simcon 3.1 for CC2.
  - Noise measurement results can be found in ILC-docdb # 274: "Simcon3_1_noise_measurements", G.Cancelo, K. Treptow, (https://docdb.fnal.gov/ILC-private/DocDB/ShowDocument?docid=274)
  - The redesign of some components in Simcon 3.1 can help to lower the noise in the analog input/output channels and increase the controller's bandwidth.
- The FNAL LLRF controller is an R&D project.
  - Simcon 3.1 was used as a starting point.
- The FNAL LLRF controller is expected to be developed in time to be used in most ILCTA test areas.

Example of Simcon 3.1 noise measurements

- **Noise in the output of the DC/DC converter**
  - The output of the 5v DC/DC converter shows spurs at ~-30dBm.





The DC/DC converters have ~60mV of ripple due to >3A of current required by the ADCs and DACs. Power supply ripple is converted to noise by the front-end amplifiers

Redesign strategy: Use lower power ADCs, avoid high current DC/DC converters. Replace differential amplifiers with pulse transformers.

FNAL LLRF controller

- Power management modifications with respect to Simcon 3.1:
  - New 14 bit ADCs draw 4 times less power and use +3V supply.
  - 3V are obtained by linear regulating the VME 3.3V down to 3V.
  - Analog inputs and outputs are AC coupled by pulse transformers.
- Clock distribution:
  - External clock jitter and internal clock jitter of ~200fs.
- FPGA size: 3x times bigger (Xilinx Virtex-4).
- PowerPC processor (instead of the one built into the FPGA).

- Schedule:
  - 1st hardware by end of November, 10 weeks debugging.
  - 5 board production and commissioning in early 07.

New IF frequency in the range of 10's of MHz

- Simpler than current 250KHz sampling method in Simcon
  - Less hardware required.
- Lower latency for the LLRF controller.
- Design is reported in ILC-docdb # 289: "IQ detector design", G.Cancelo, (https://docdb.fnal.gov/ILC-private/DocDB/ShowDocument?docid=289)
- Status: I-Q detector has been implemented in is being tested.

•Numerically controlled Oscillator (NCO) output:
120 dBc noise using a 12 bit table