Data Acquisition System Development Status

Applications on the CALICE AHCAL and ScECAL

- AHCAL DAQ Overview
- Status update
- To-Do

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AHCAL Testbeam Preparation
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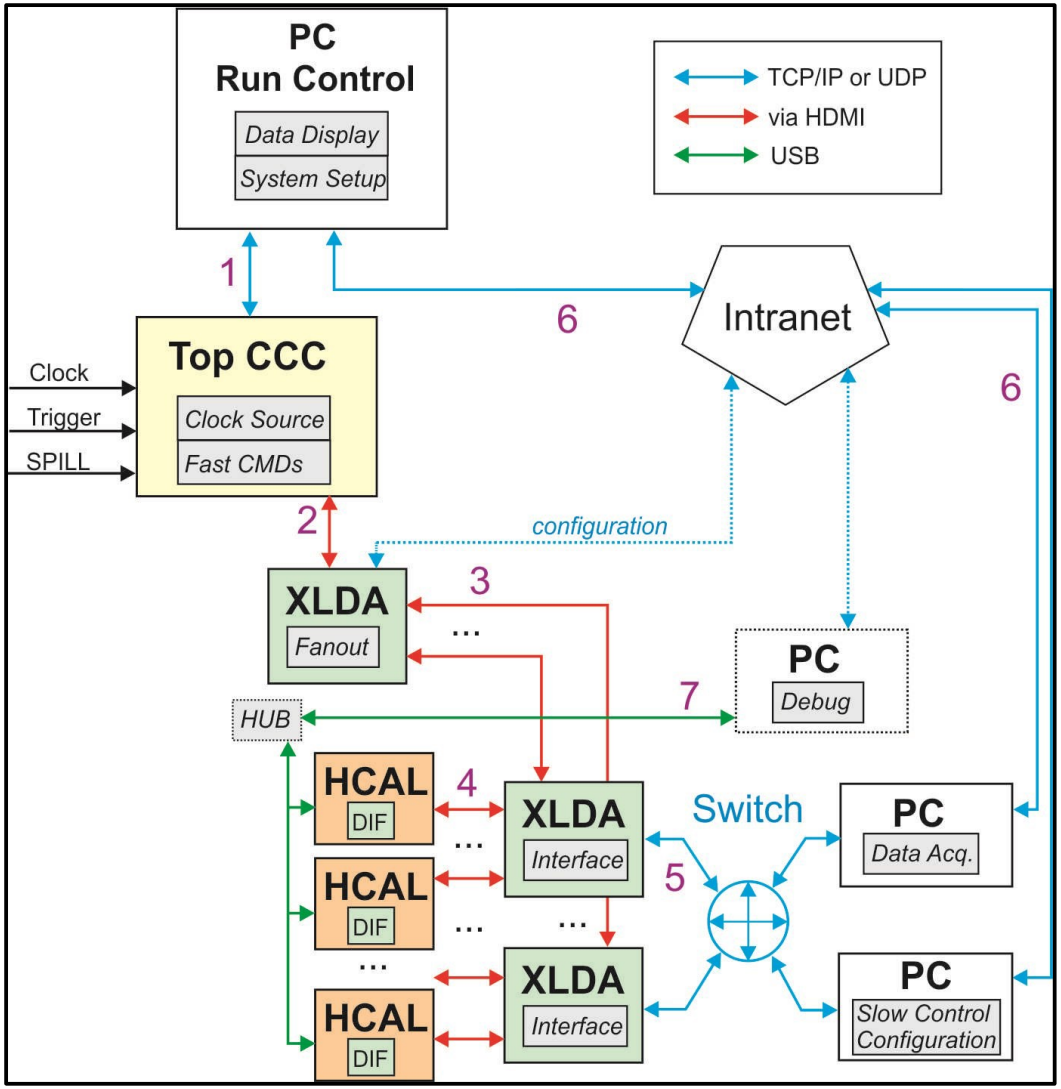
CALICE Calorimeter for ILC
DESY

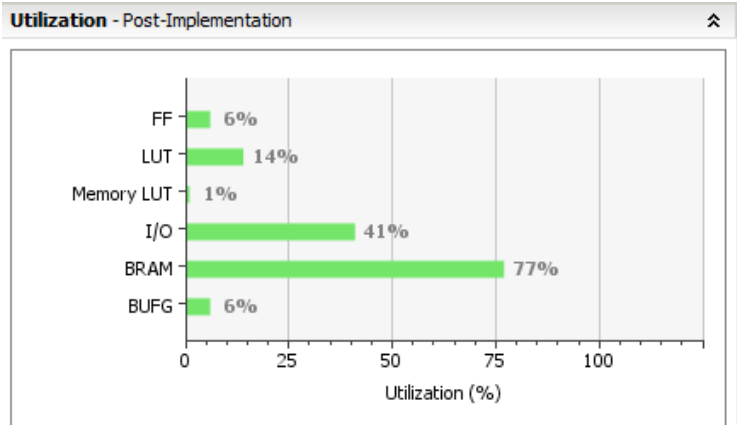
DAQ System Architecture

- Main DAQ subsystem:
  - PCs and Software Package
  - Clock and Control Card
  - Link and Data Aggregator
- Communicate over
  - Ethernet
  - HDMI
  - USB (debugging purposes)
- Master of operation is the Run Control PC
  - Initialization
  - Detector configuration
  - Data taking

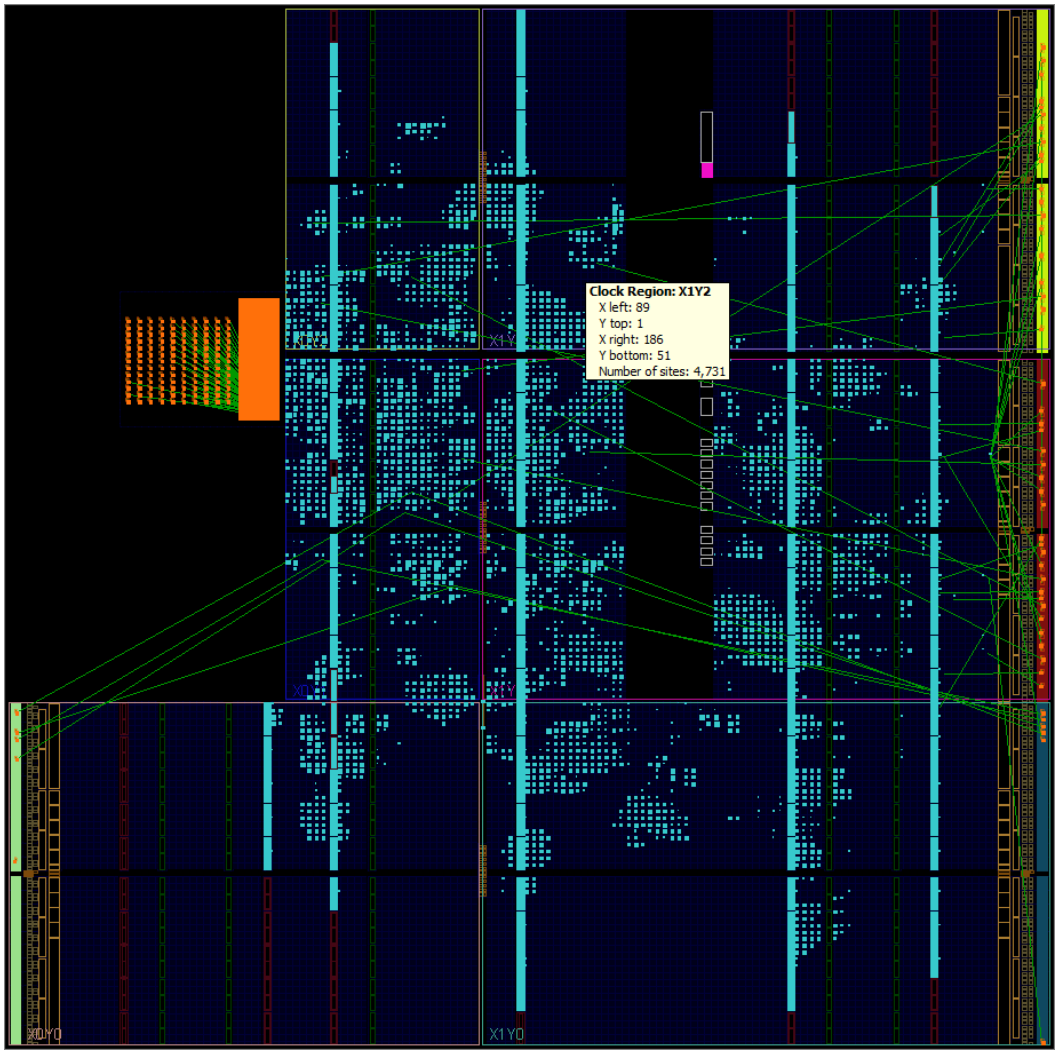


Mini-LDA Firmware

- All 10 ports are enabled and tested
  - 4 ports for 4-HBU layers
  - 6 ports for 1-HBU layers
  - Estimated total on-chip power: 2.1 W



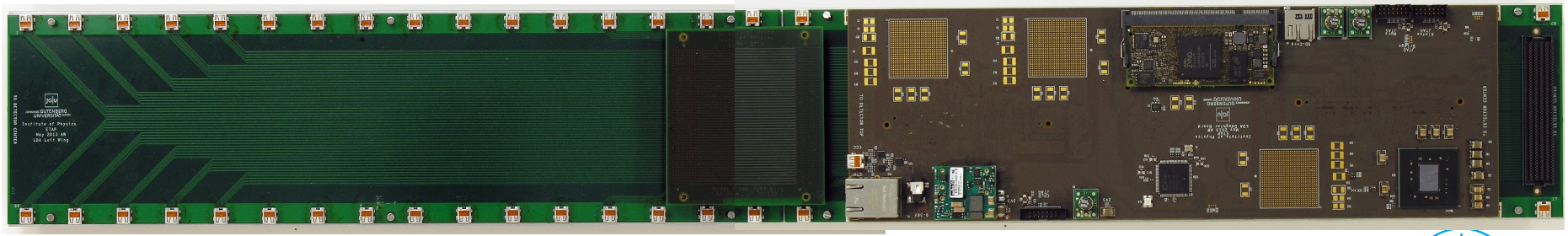
FPGA Resource Utilization



Mini-LDA implemented design on Zynq-7000

Wing-LDA

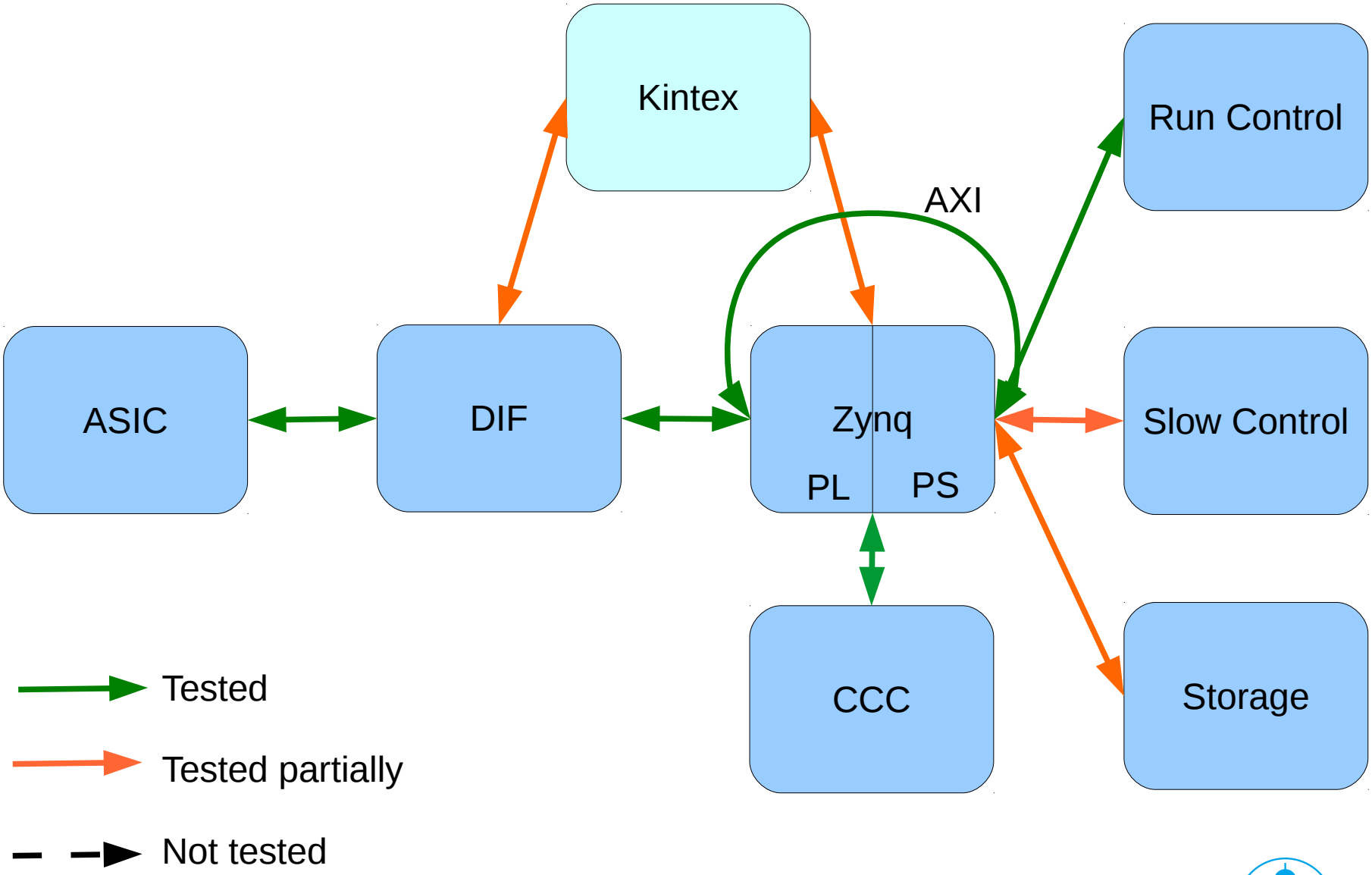
- Hardware Debug Completed
  - Problem with SD card is solved
  - Linux is up and running on the Wing-LDA
- Production of a new Wing-LDA in progress (Uni. Mainz)
  - Fixed bugs
  - Addition of a serial port for debugging
- To-Do
  - Zynq-Kintex firmware test
  - Configure input/output signal delays
  - Full system test



DIF and DAQ Software

- DAQ Interface (DIF)
  - Start/Stop acquisition implemented as fast command
    - Tested with USB
  - Fake trigger
  - Dynamic switching between HDMI and USB
    - No need to re-program the DIF
  - Final version to be tested
- Software
  - PiconfZ (Linux Driver) tested successfully
  - PL-PS data rate needs to be improved
  - Piconf Master/Slave can't be used
  - An application is developed to replace Piconf slave
  - Single layer USB LabView is changed to USB
    - Command and Acknowledge are tested
    - Slow control to be tested

DAQ test and commissioning chain (as of today)



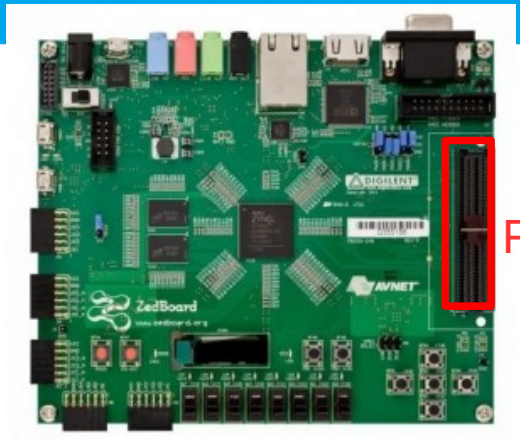
To-Do

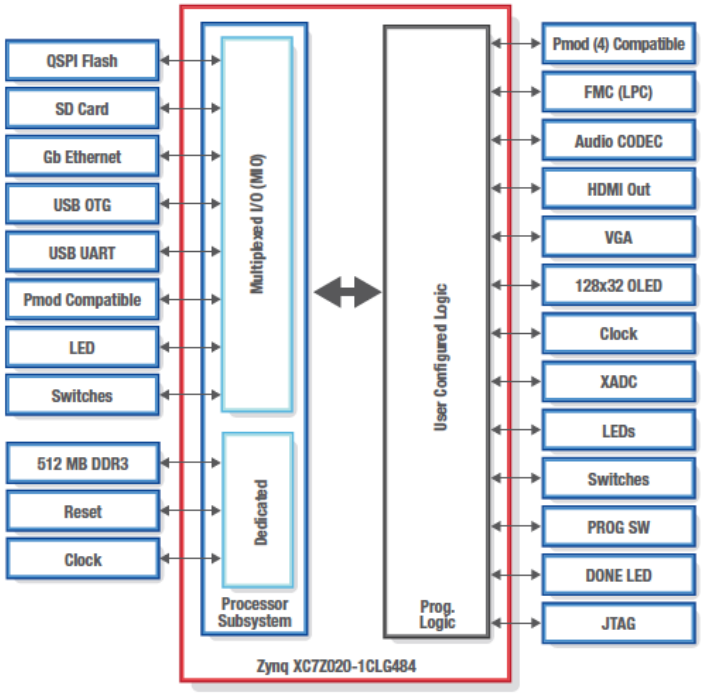
- Finalize DIF firmware
- Complete single layer LabView
- LED run using Mini-LDA
- Test/debug Kintex+Zynq on the Wing-LDA
- LED run using Wing-LDA
- Run Control Software
- Data Storage Software

Backup

ZedBoard

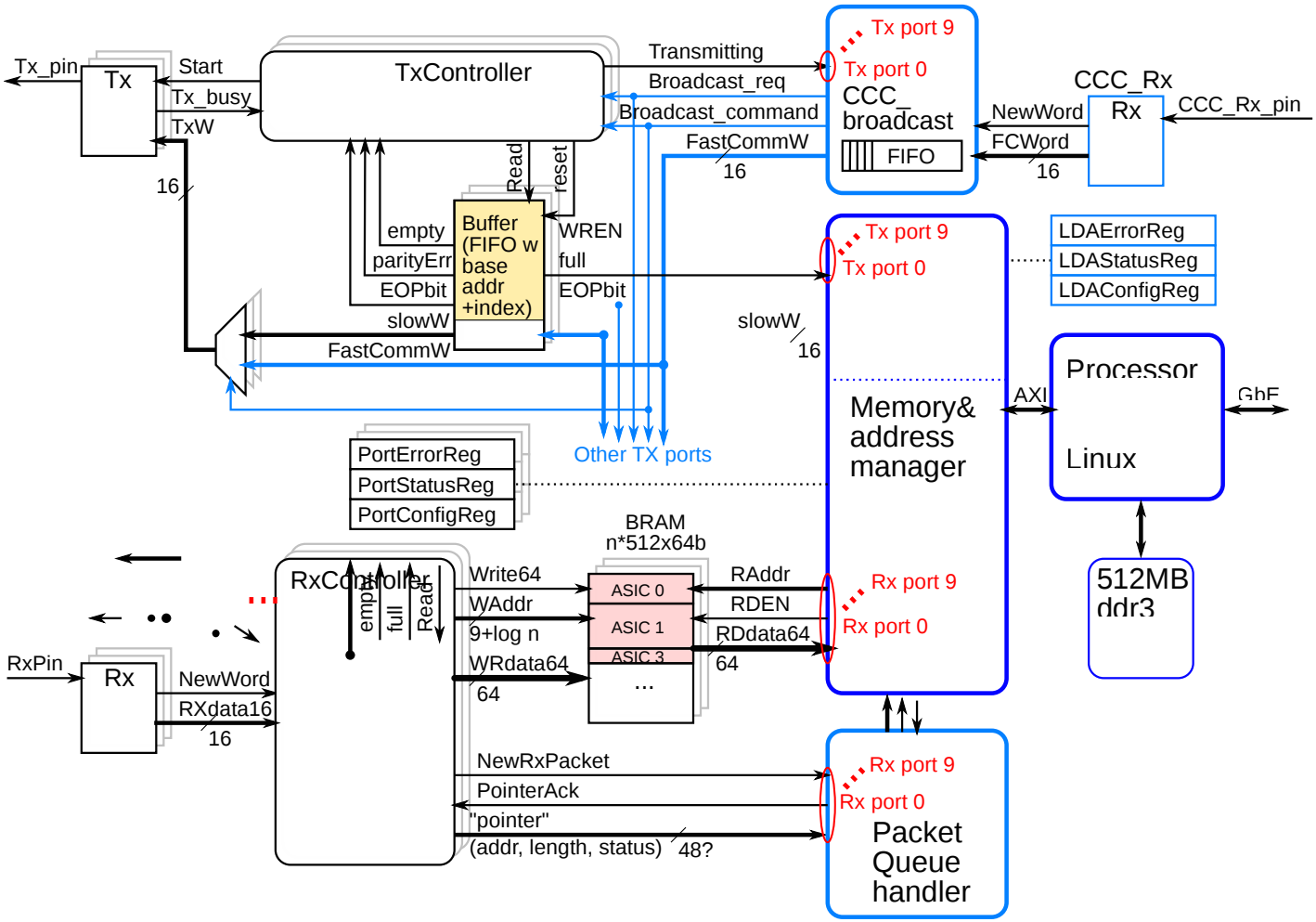
- Zynq Evaluation & Development Board
- Xilinx Zynq-7000 SoC
  - Processor Subsyst. (PS): Dual ARM Cortex-A9
  - Programmable Logic (PL): Xilinx 7 series FPGA
  - 100Gbps interconnect bandwidth
  - ARM programmability+FPGA flexibility
- On board memory
  - 512 MB DDR3 + 256 MB QUAD-SPI
- PS is able to run Linux
- FPG Mezzanine Connector (FMC)
  - Allows adding custom boards





LDA Firmware Block Diagram

LDA concept 2014-06-24



PortConfigurationReg
...: PortEnable
...: ClkEnable
...: BusyPropagationEnable
...: SaveAcknoledgments
...: SaveErrors
...: MergePackets
...: WaitForACK
...: Resends[1..0]

PortErrors (persistent)
...: RxPacketFormatError
...: RxPacketIDError
...: RxPacketOrder
...: RxTimeout0Error
...: RxTimeout1Error
...: RxLengthOverflow
...: RxPointerOverwritten
...: RxCRCerror
...: RxCRCok
...: RxPointerSaved]