Development and performance of bottom side readout ScECAL for ILC

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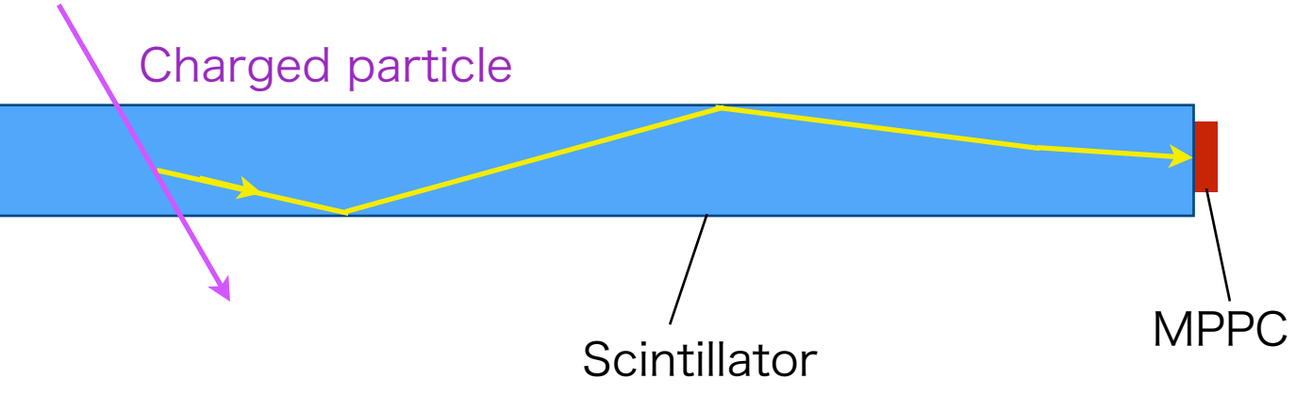
Outline

- Concept of bottom side readout design ScECAL
- Manufacturing of prototype EBU
- Performance of bottom side readout EBU in October test beam

Concept of bottom readout design

Baseline design



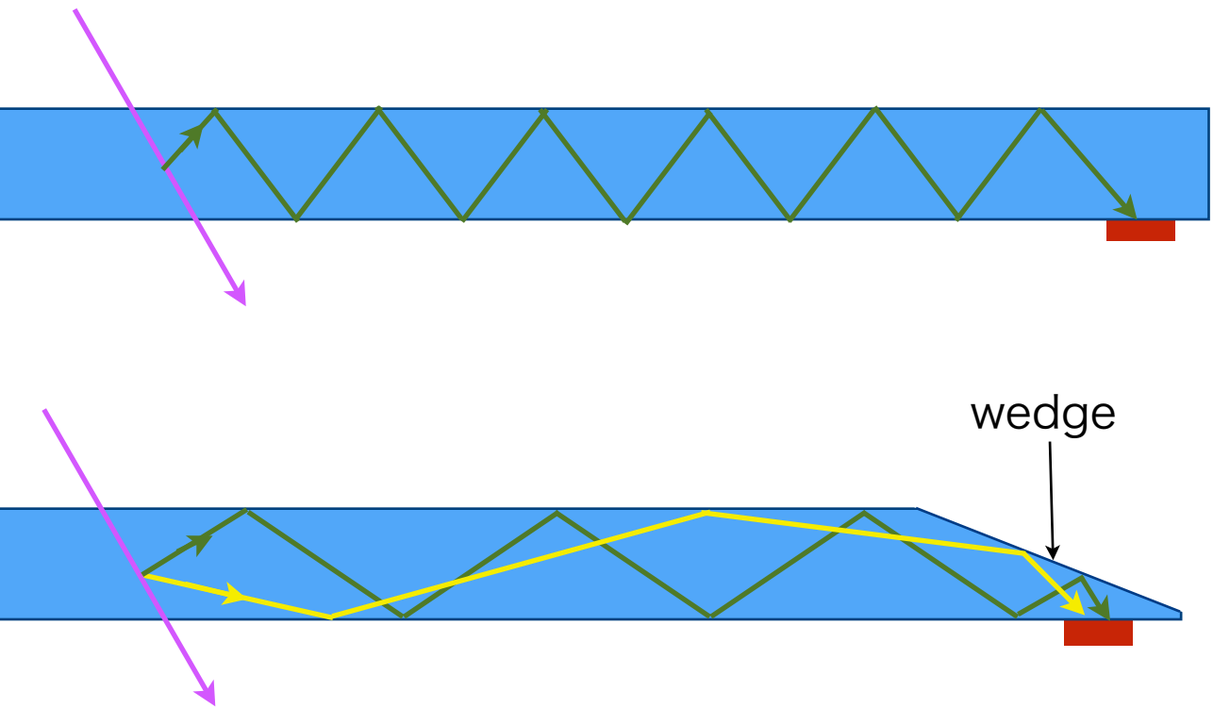
Baseline design shows good performance.

- Less number of reflection → high light yield
- Good uniformity

Technical problems exist.

- Dead gap due to MPPC installation
- Peaky response near MPPC

Bottom side readout design



Bottom side readout design was proposed.

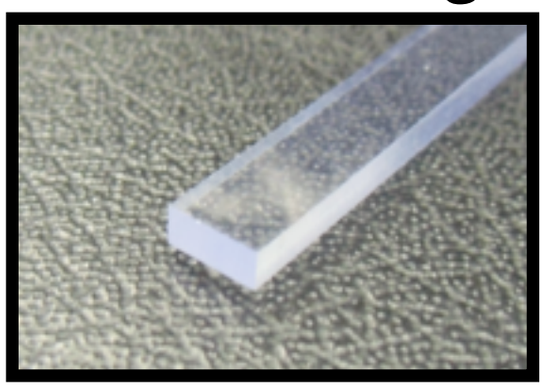
- Gap less layout is possible
- Easier MPPC installation → advantage of mass production
- Larger number of reflection → lower light yield
- Bad uniformity

Wedge shaped design was proposed.

- Wedge works as prism to guide scintillation light to MPPC → recover light yield
- Shorter pass length for particle going through near MPPC → good uniformity

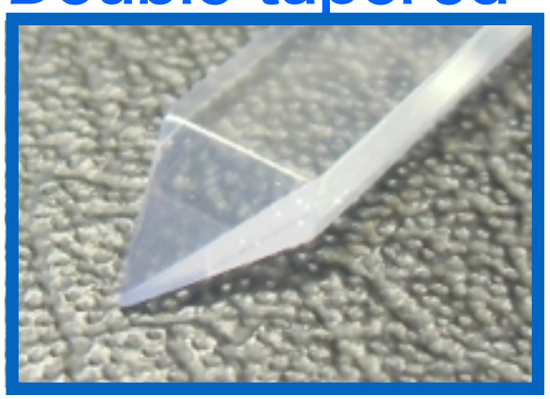
Effect of wedge

Baseline design

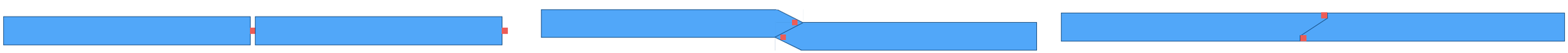


Simple wedge

Double tapered



Single tapered

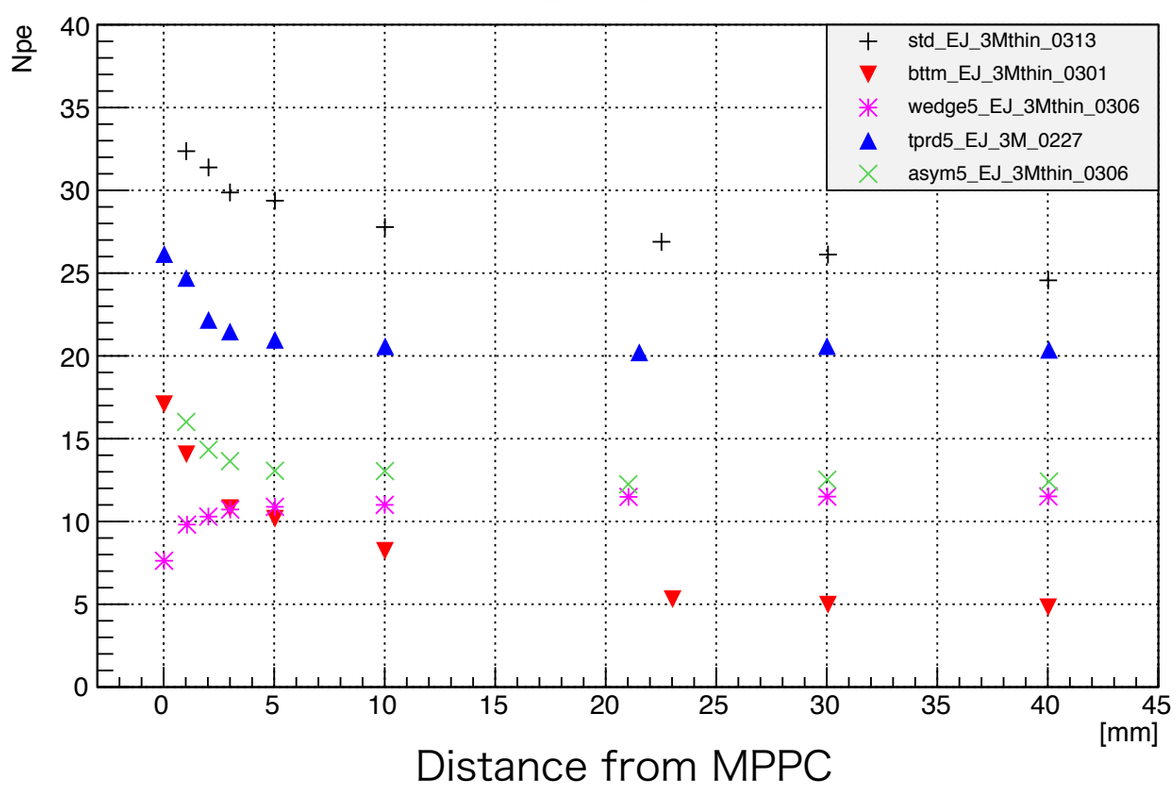


Wedge works to recover #p.e. and improve the uniformity.

Test beam in autumn 2014

- evaluate the performance of fine segment ScECAL with 3 layers.
- make one of prototype EBUs with bottom side readout design
- test 10k pix. MPPC

Light yield



Bottom side readout prototype

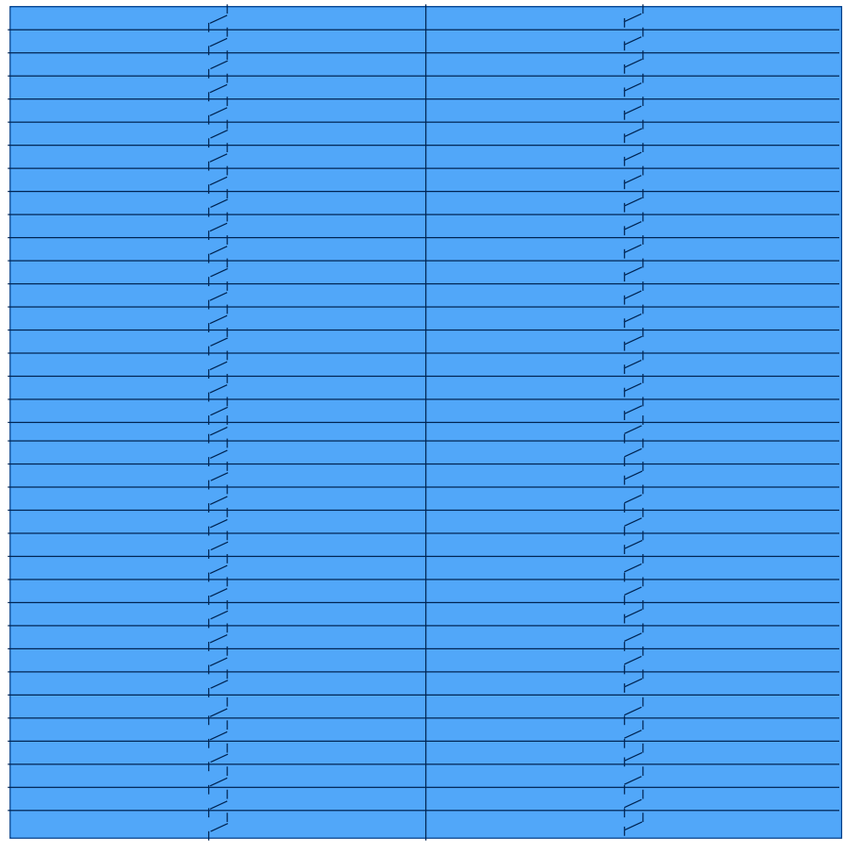
Configuration

MPPC : 10k pix. 1mm x 1mm
HAMAMATSU, S12571-010P

Scintillator : ELJEN EJ-204, 47.5mm x 5mm x 1.8mm

Reflector : 3M radiant mirror film

144 channels on 1 EBU

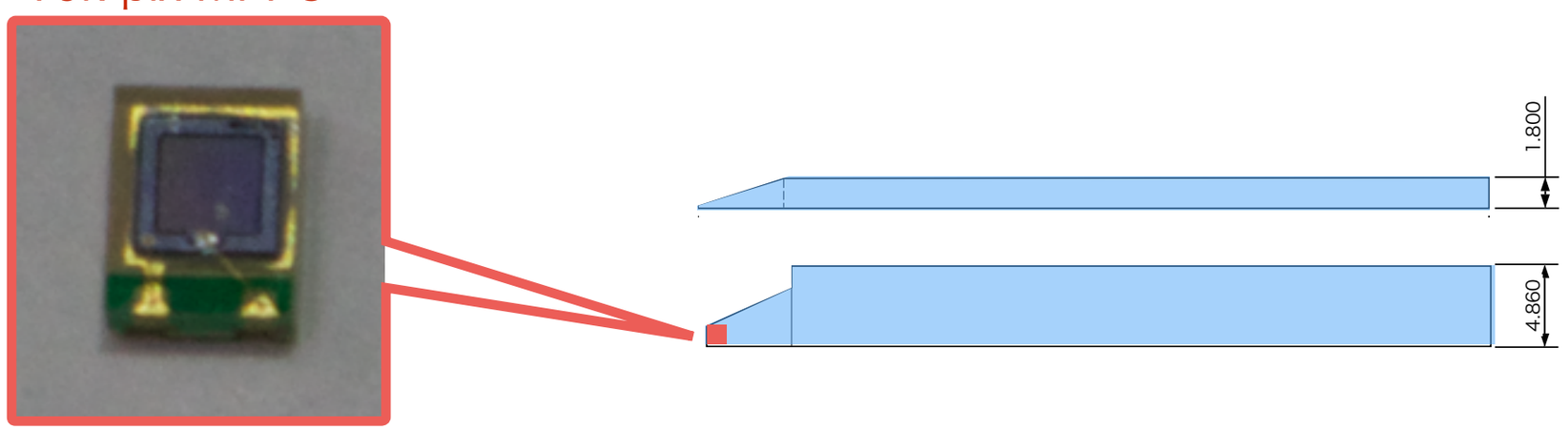


Tasks to be solved

- Current EBU is intended for baseline design.
  → some arrangements are needed for bottom readout

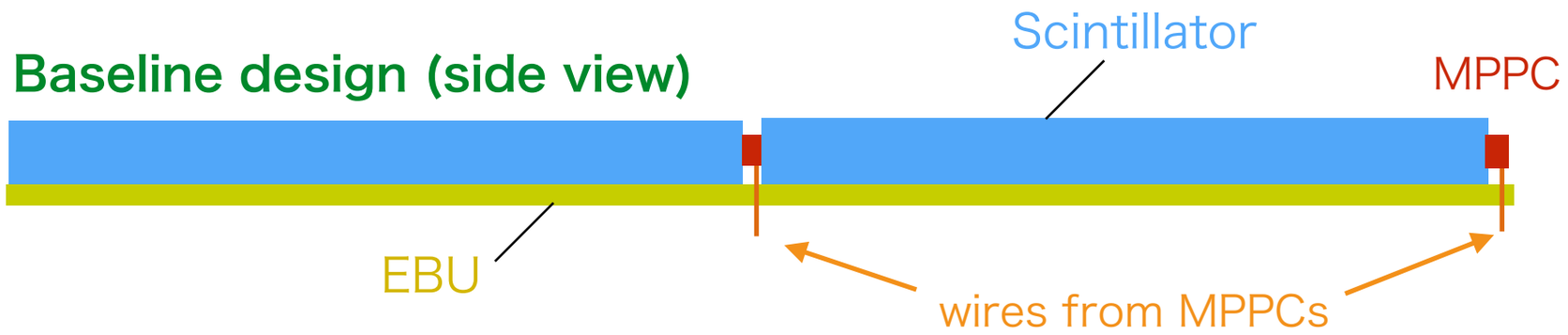
- The design of reflector is complicated.
  → the method of manufacturing reflector should be suitable for mass production

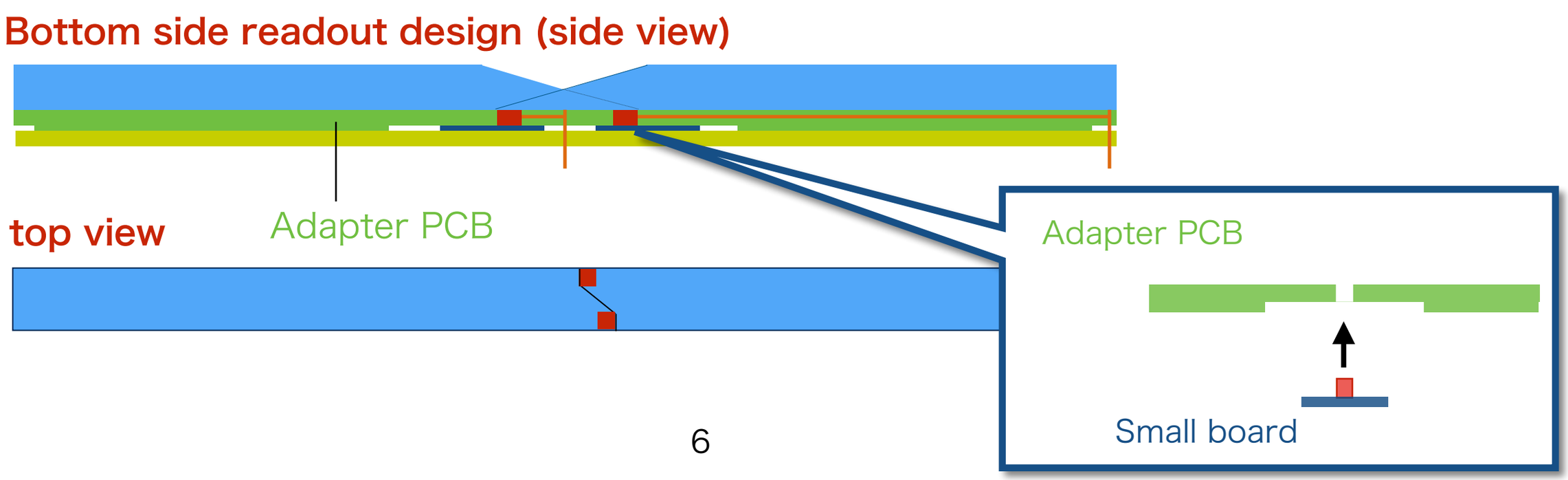
10k pix MPPC



Adapter PCB

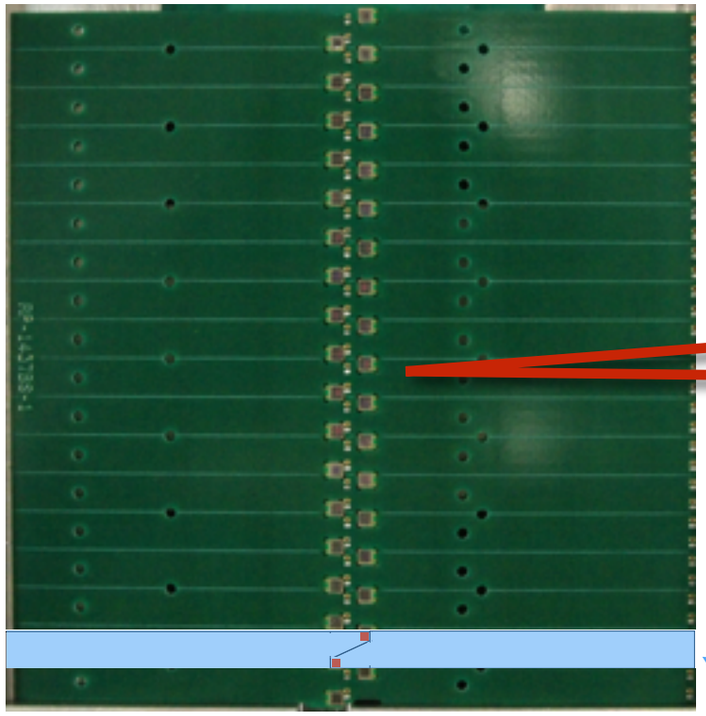
EBU has been designed for baseline design.
Adapter PCB is designed to change the wiring. This board also works as spacer.
This configuration is applicable to direct installation of MPPC to EBU.



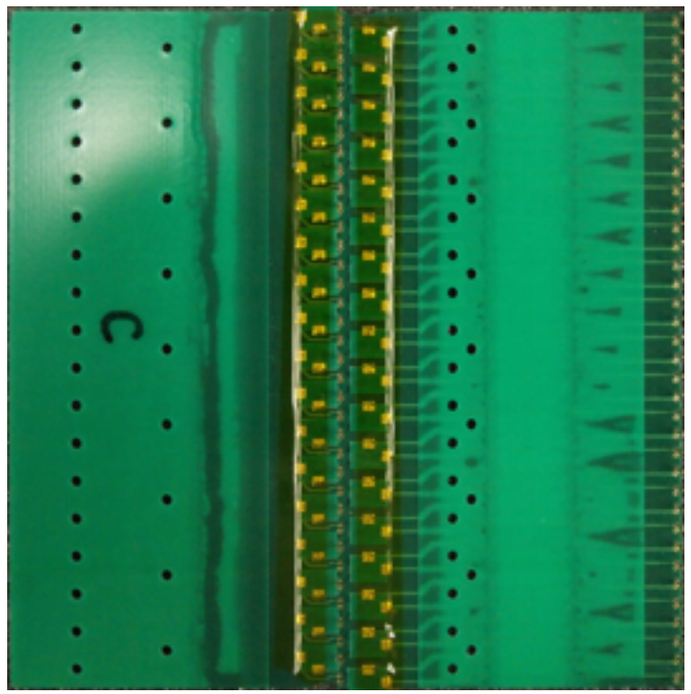


Adapter PCB

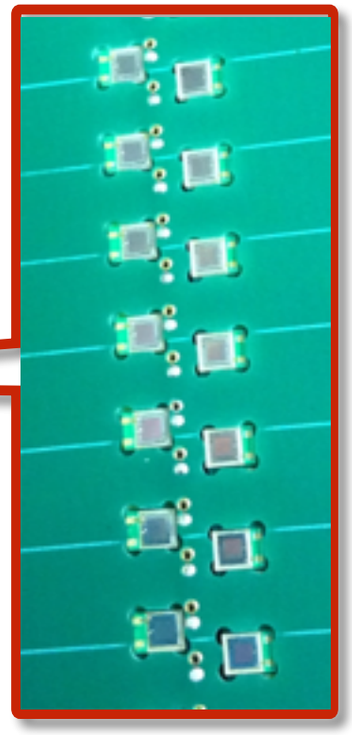
4 boards for 1 EBU



back side view

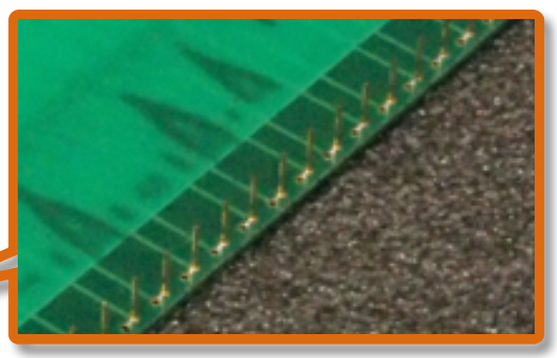


MPPCs

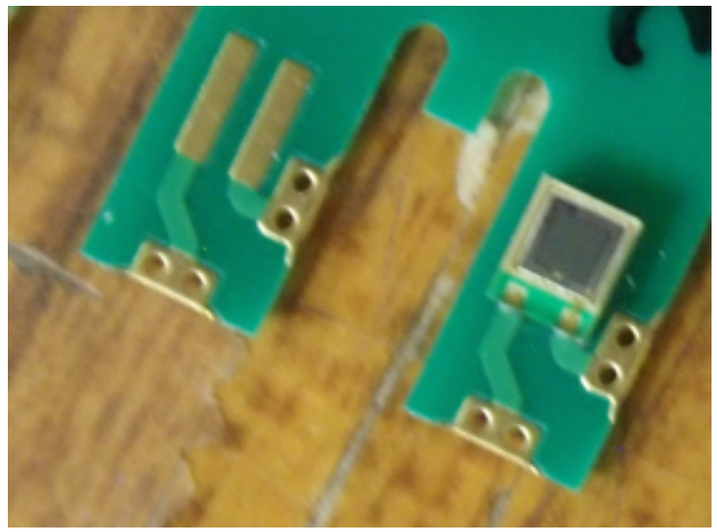


Scintillators

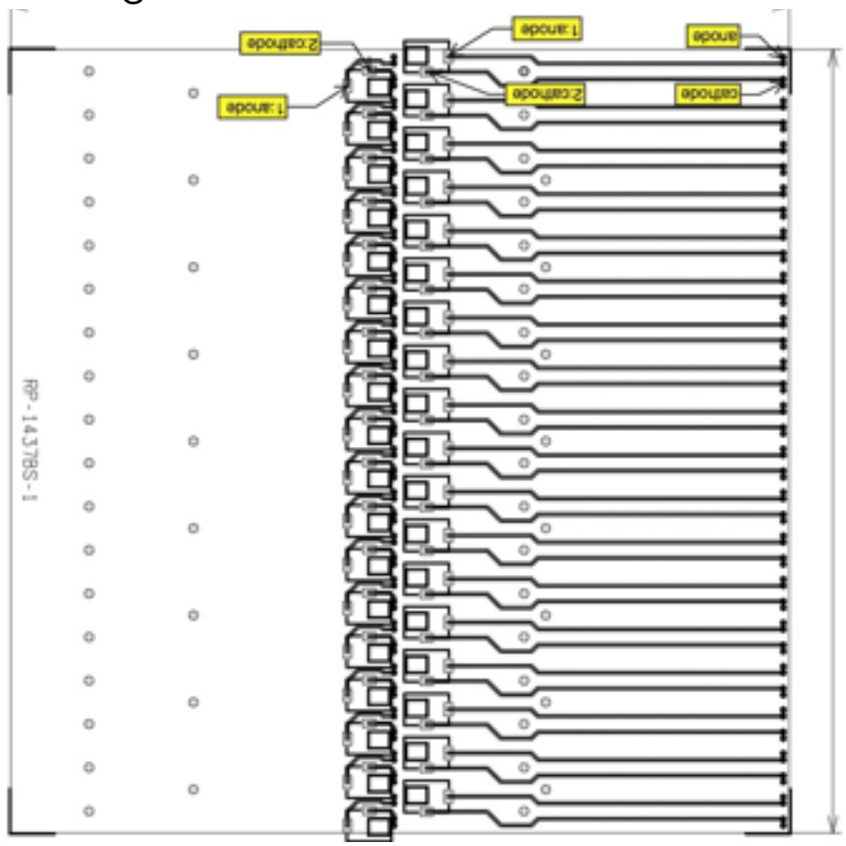
Pins



MPPC on small board



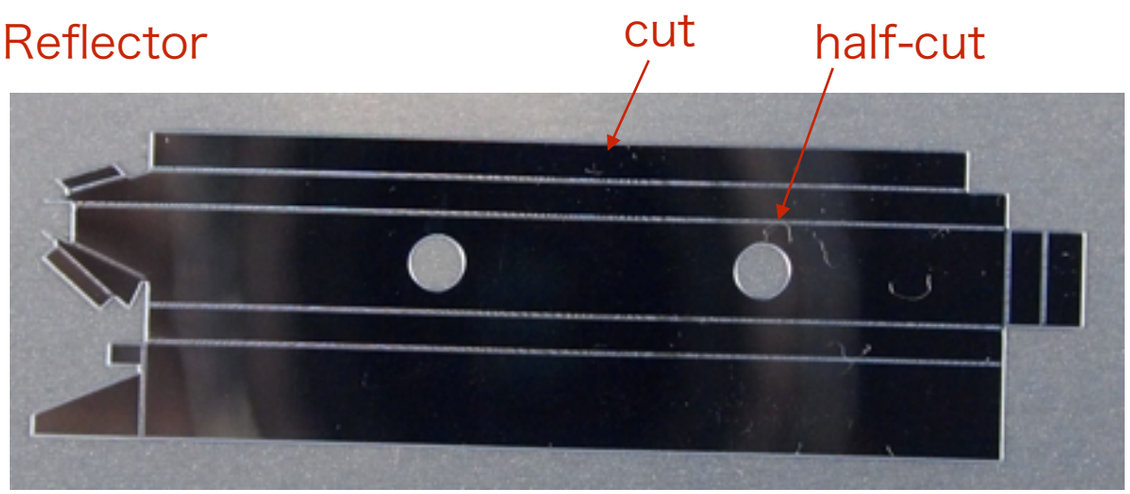
Wiring



Reflector

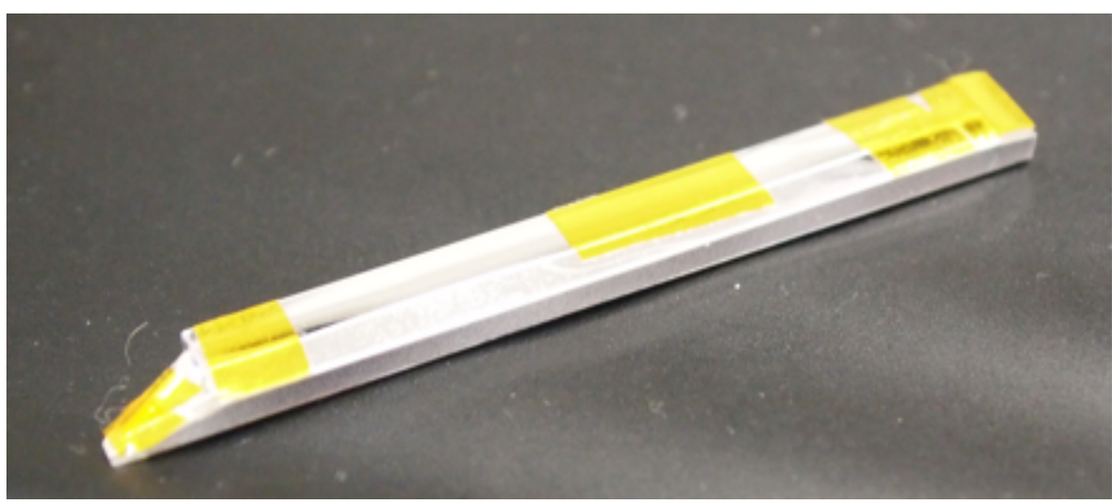
Laser cutting is manufacturable solution for mass product of reflector.
Half-cutting enable to make crease easily.

Reflector



Scintillator

Scintillator + reflector



Reflector is fixed with kapton tape.

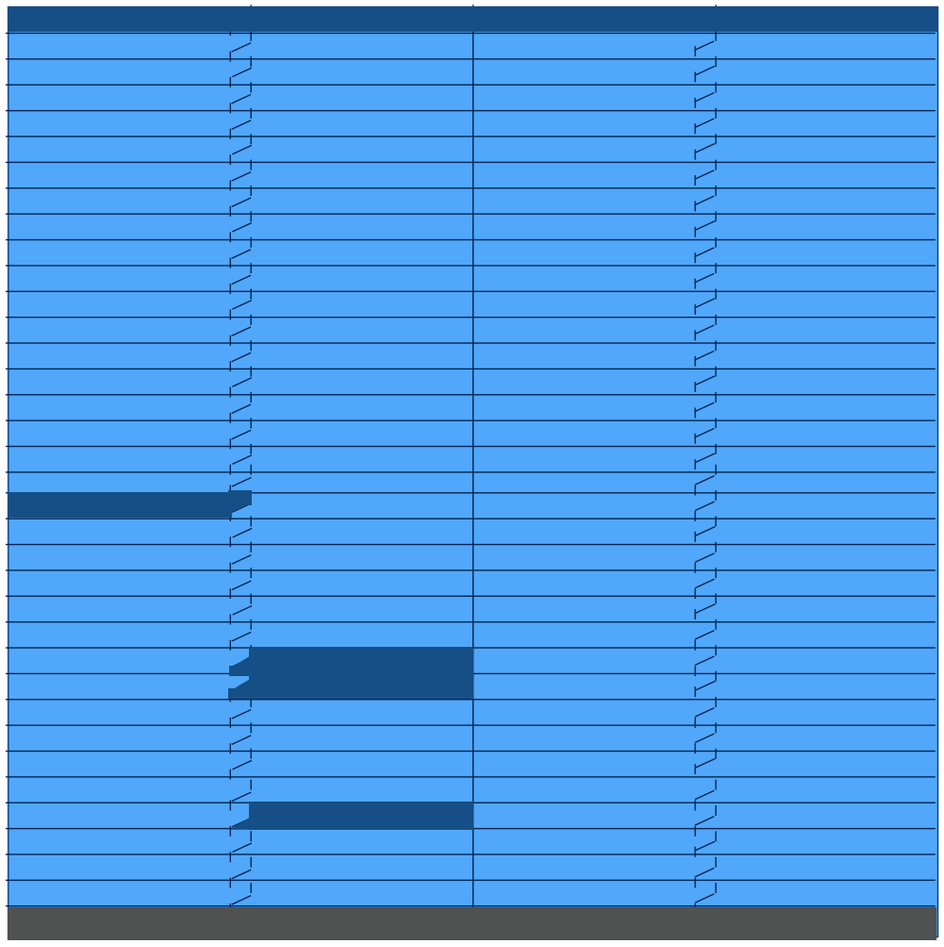
Status of EBU1

Status of channels

Dead : 0 channels

Low hit rate : 8 channels

Masked : 4 channels (because of light leakage)



Problems

Bad S/N

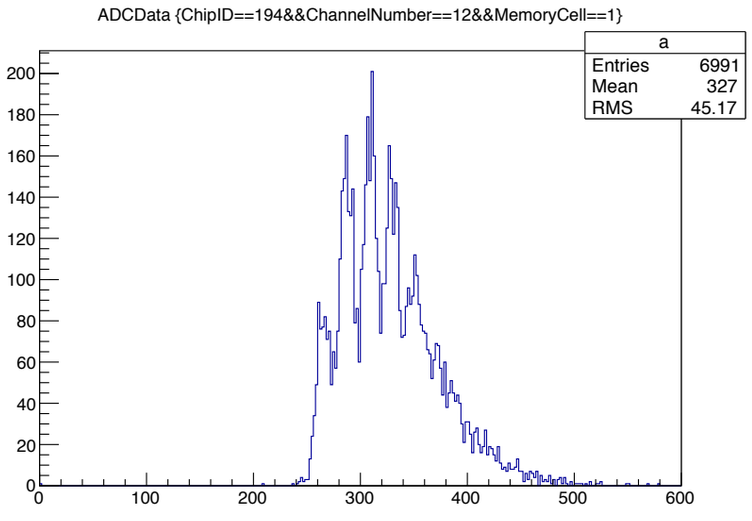
- Hard to see single photoelectron peak.
- High ADC thresholds were needed to suppress noise rate.

LED calibration

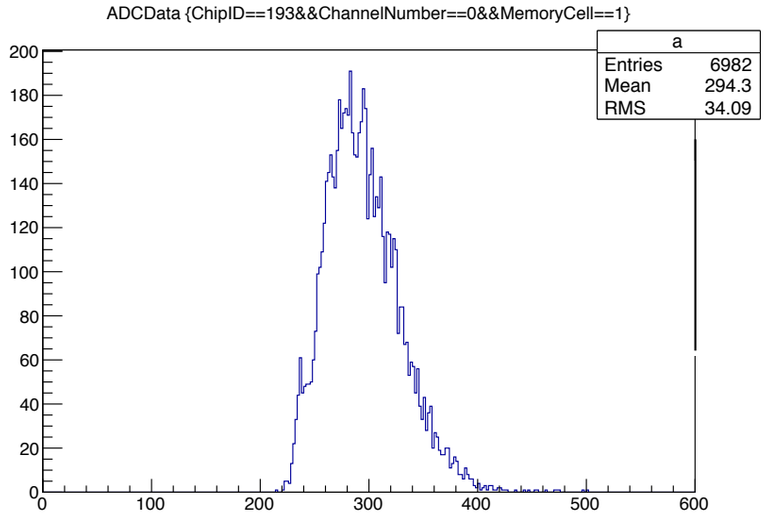
ADC dist. of 1ch.

- Good photoelectron separation with 1600 pix. MPPC.
- No obvious photoelectron separation with 10k pix. MPPC. This problem would be solved by optimizing SPIROC for 10k pix. MPPC.

Typical spectrum with 1600pix. MPPC



Spectrum of 10k pix. MPPC



Status of EBU1

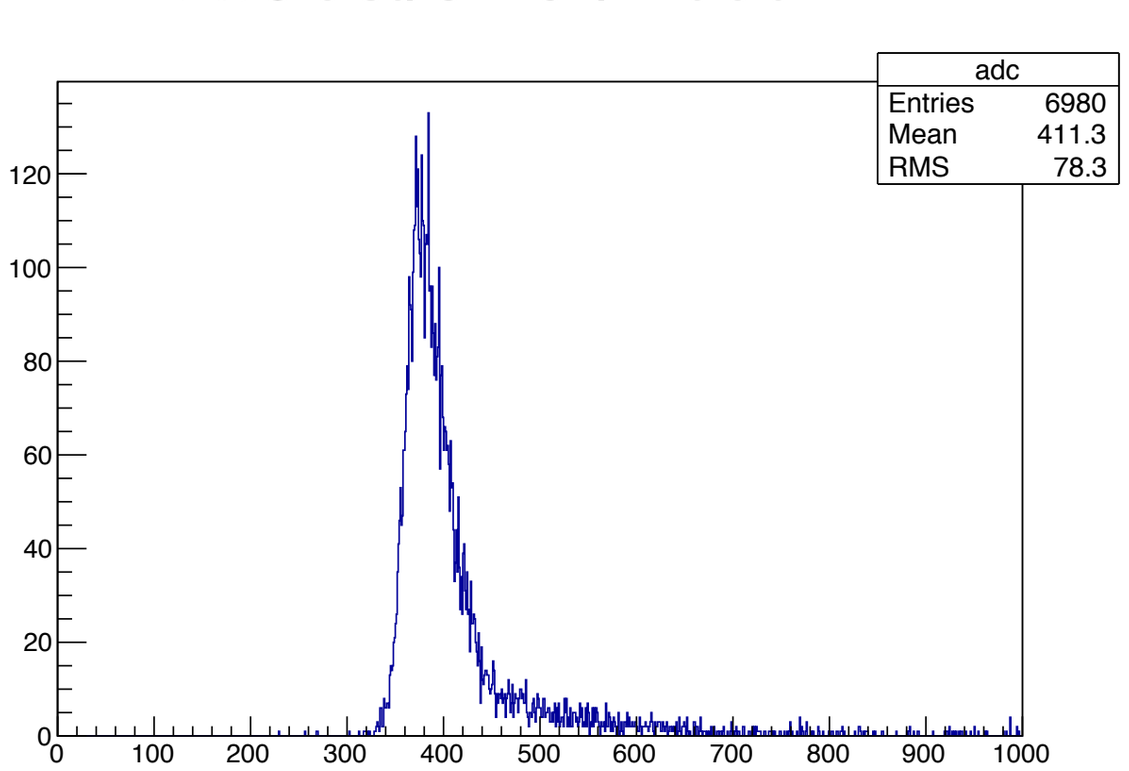
Hit bit

- Threshold can be set chip by chip. (not channel by channel)
- Hit bit is set when signal is over the threshold.
- Sometimes ADC of channels with hit bit=0 were affected by noise. (ADC was changed.)

Record data

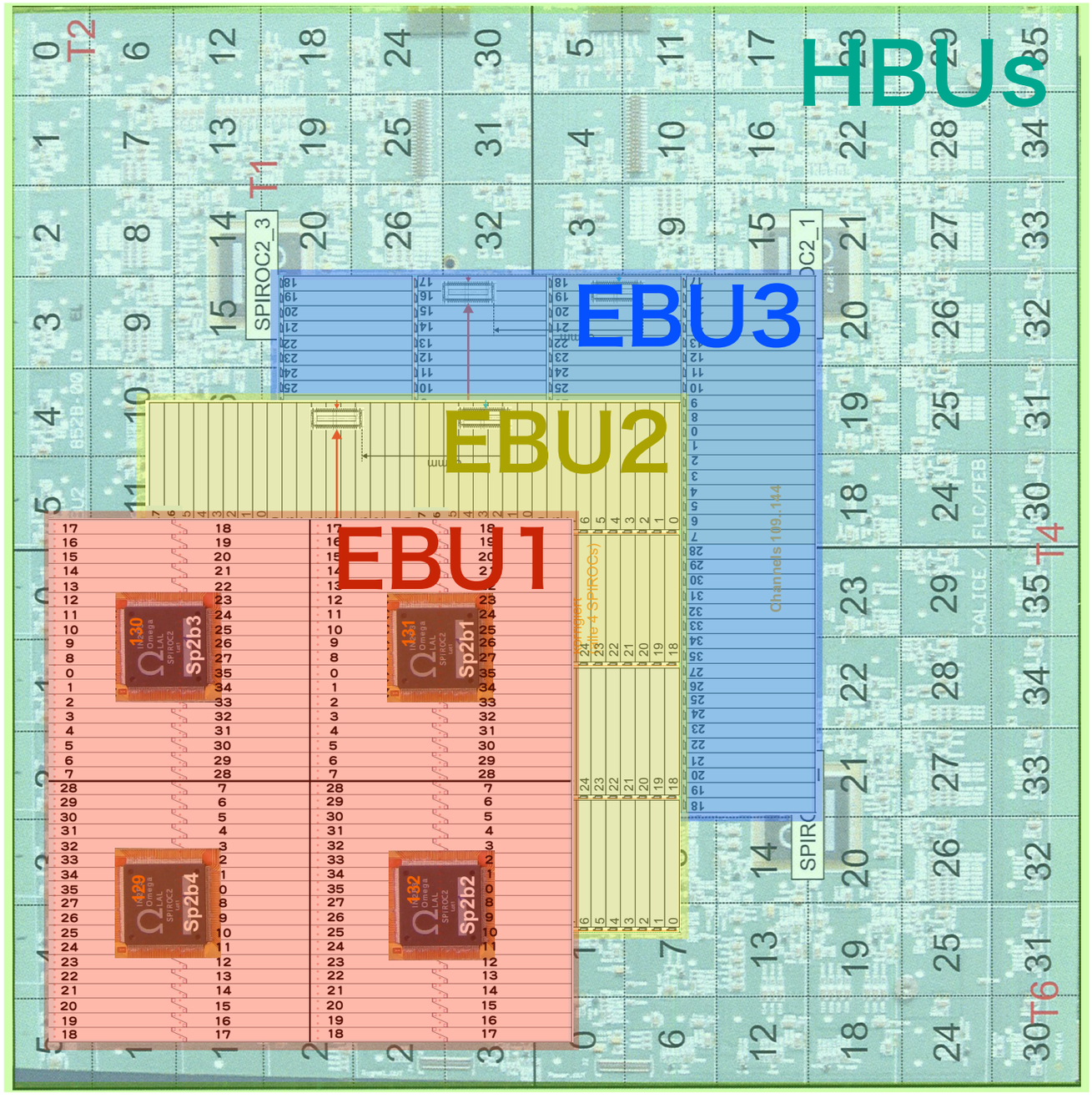
- 1 chip regulate 36 channels.
- If more than 1 of 36 channels set hit bit, all the channels belong to the chip are read out.
  If 36 channels are hit bit=0, no data is recorded.

Hits are dominated by noise in EBUs.
Additional rules of event selection are needed,

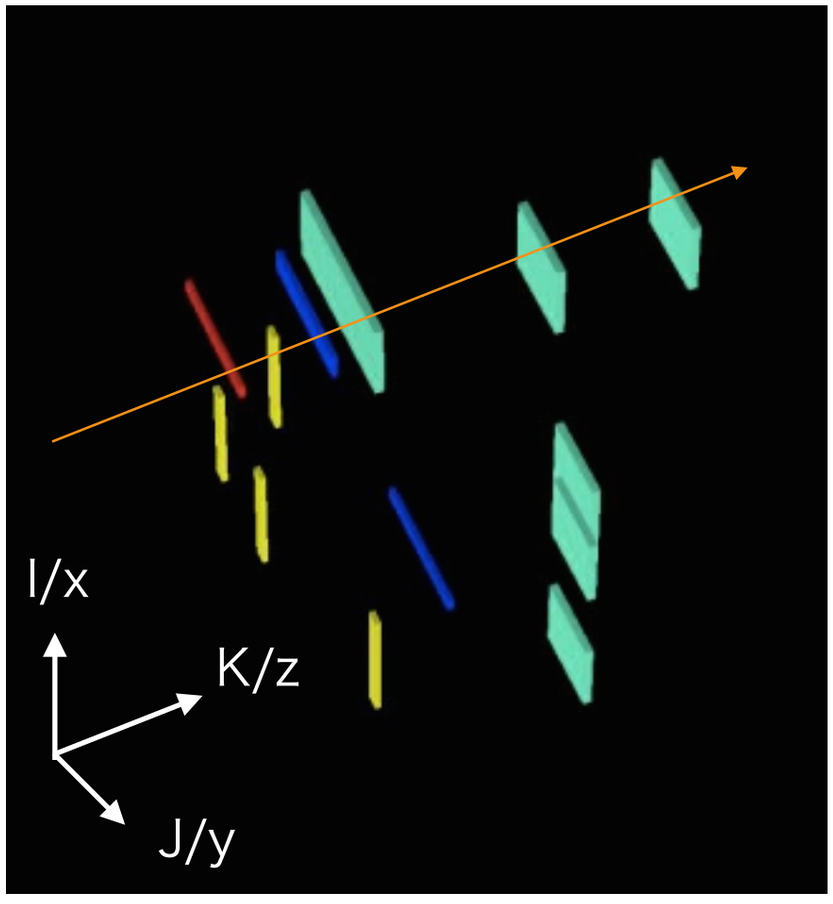


Event selection

HBUs and EBU3 are used as reference counter.
EBU1 and EBU3 have similar geometry.



Event display



EBU strip : 45mm x 5 mm
HBU tile : 30mm x 30 mm

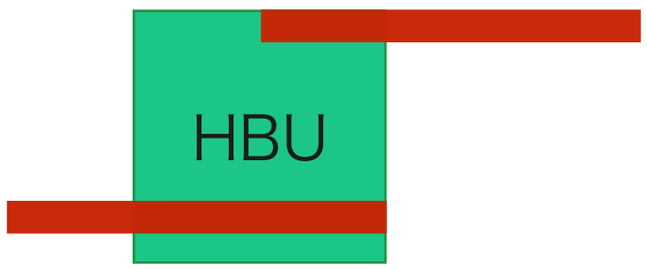
MIP

Muon run (2014. Oct)

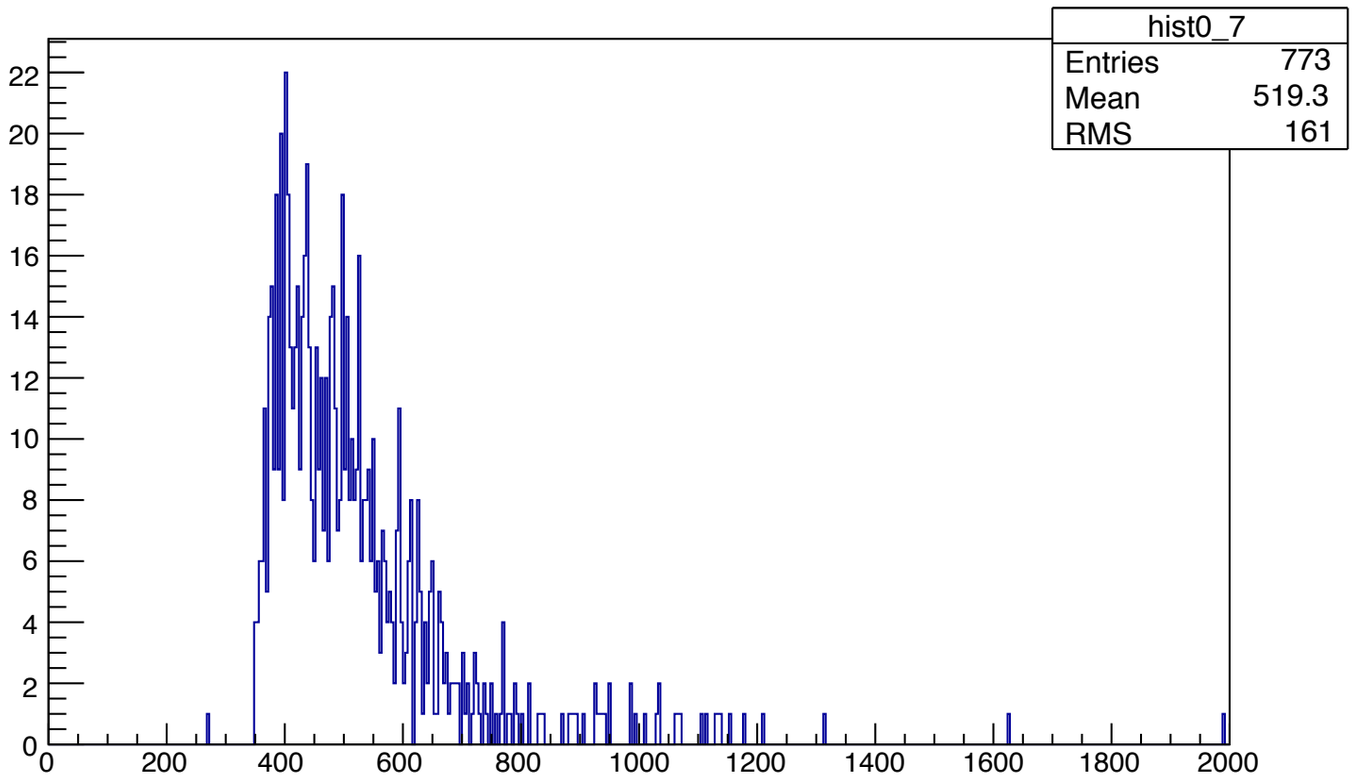
Condition of track finding : more than 3 HBU layers and EBU1 set hit bit

For most channels, whole picture of MIP peak can not be seen.
Threshold setting was higher than it should be.

Evaluate strips which have overlap with HBU tiles



ADC dist. of muon events (1ch.)



Efficiency

Muon run (2014. Oct)

Condition of track finding : “more than 3 HBU layers and EBU3 set hit bit” and “ADC of EBU3 > 350”

eg.) chip129, channel 7 (this channel locate at near the center of EBU.)

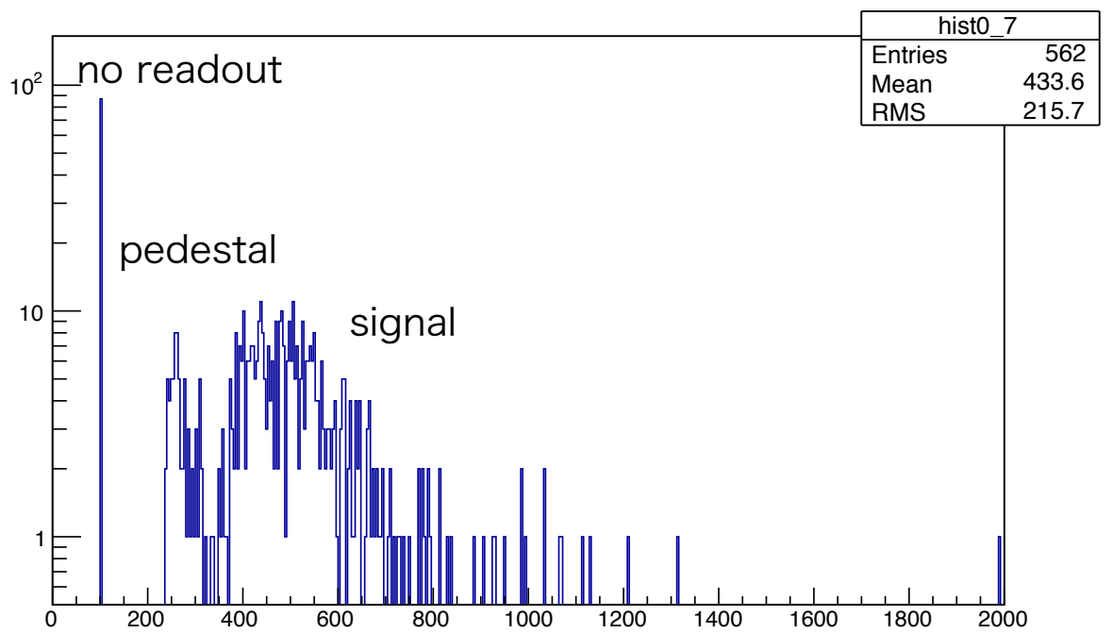
readout (hit bit 0 + hit bit1) = 475 events

no readout (nothing was recorded at the event) = 87 events

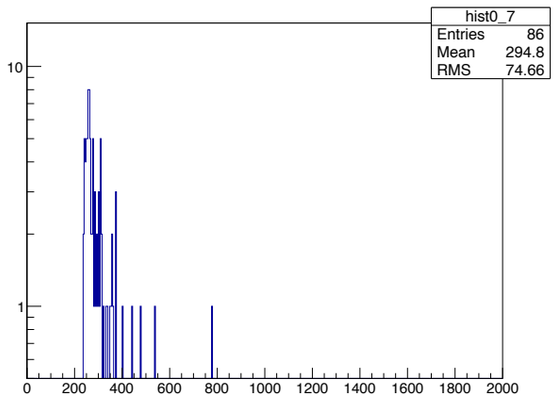
signal/(readout + no readout) ~ 72 %

→ Low efficiency because of too high threshold setting.

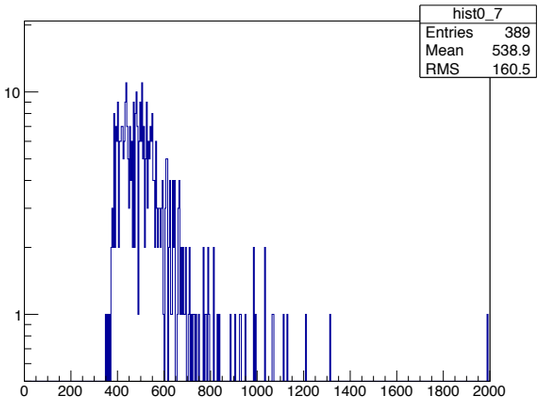
Actual efficiency would be better because it doesn’t include the effect of beam angular distribution and miss alignment.



EBU1 hit bit=0(mostly pedestal)



EBU1 hit bit=1(mostly signal)

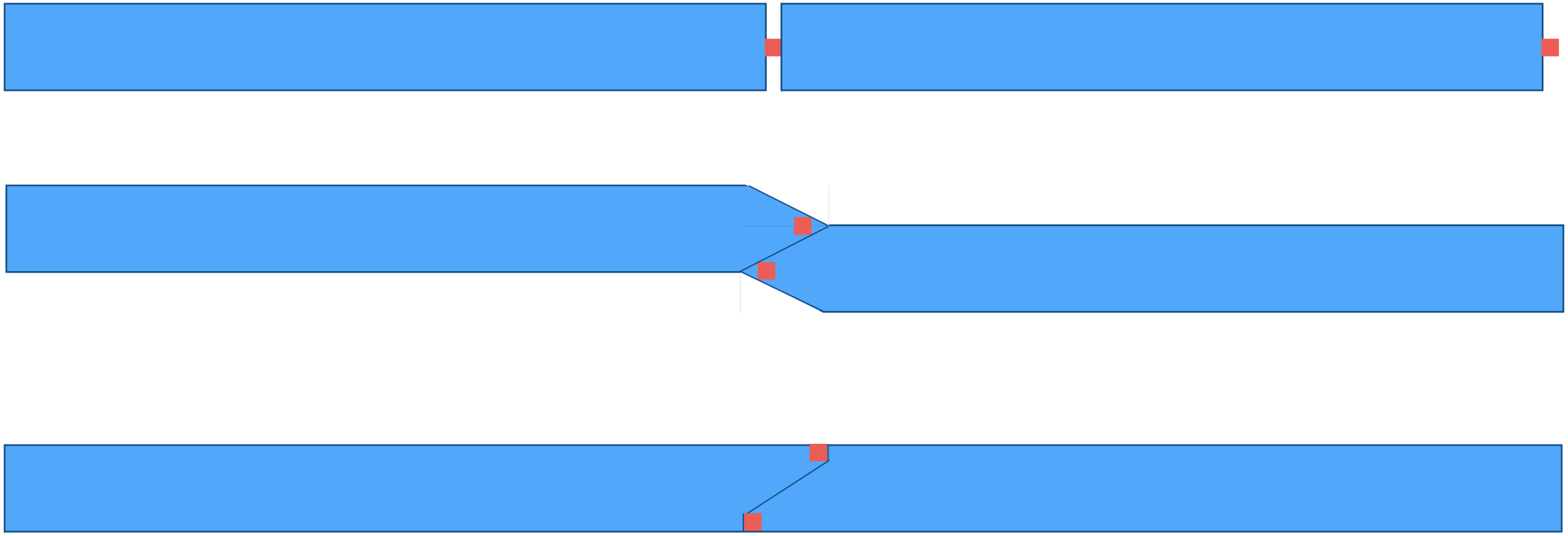


Summary

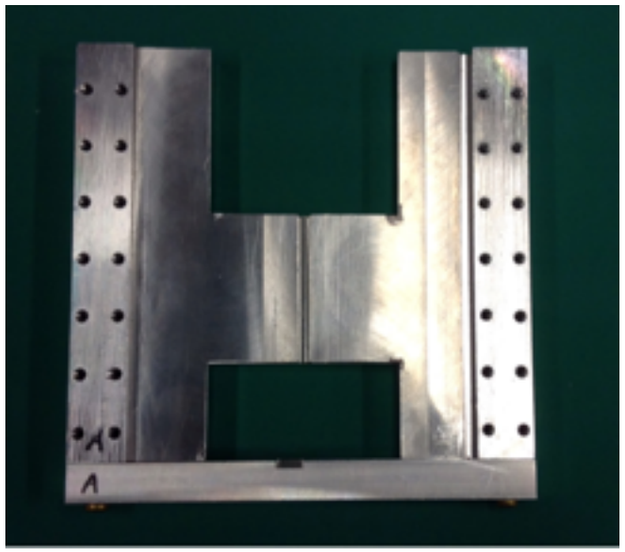
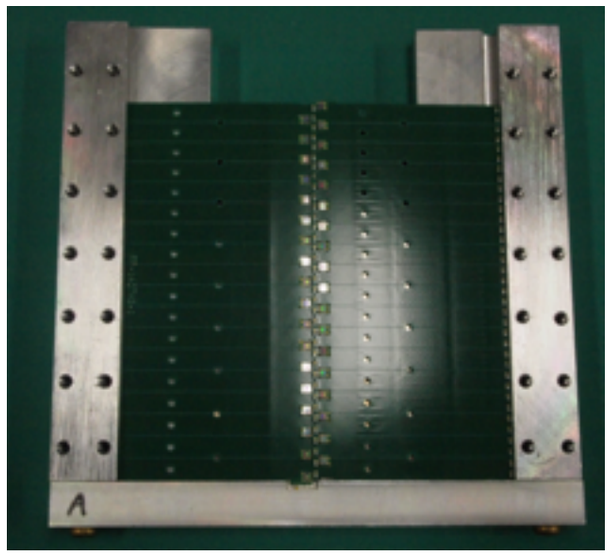
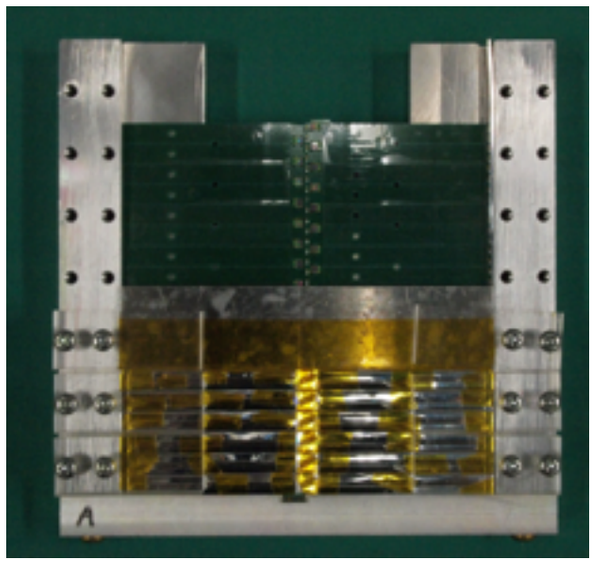
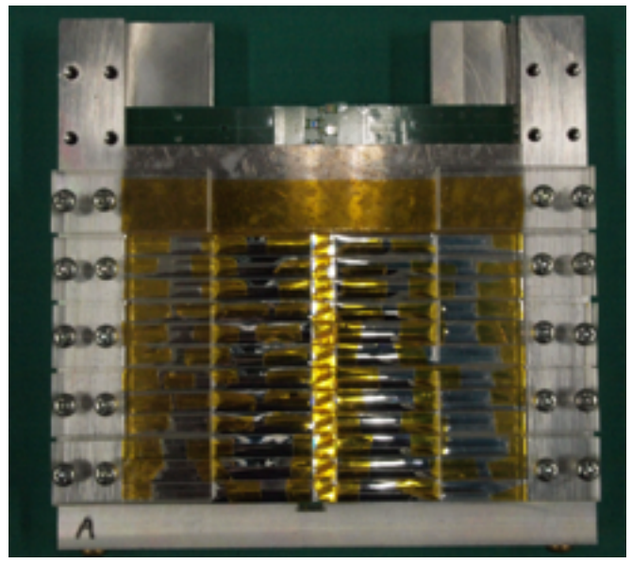
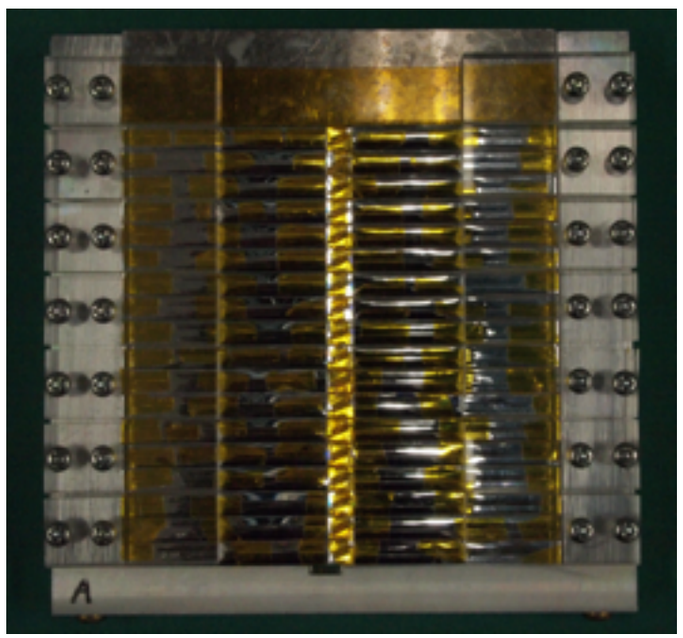
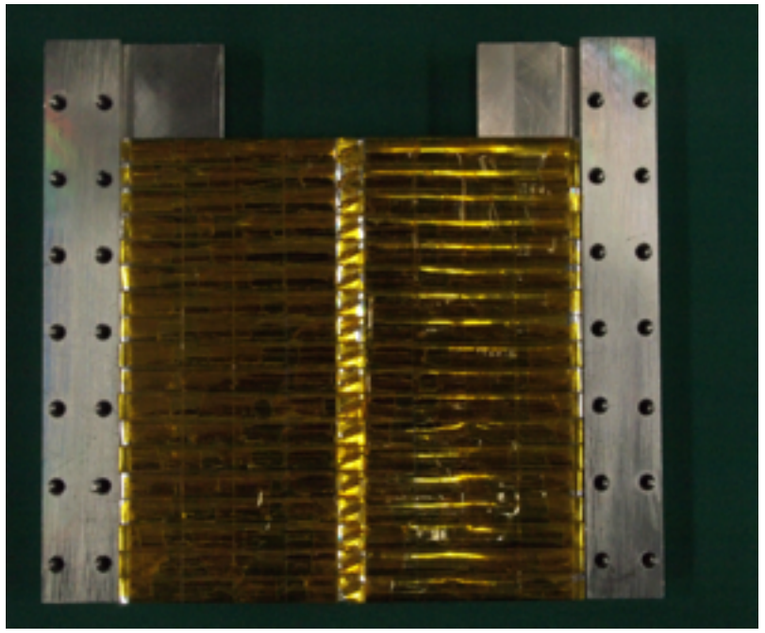
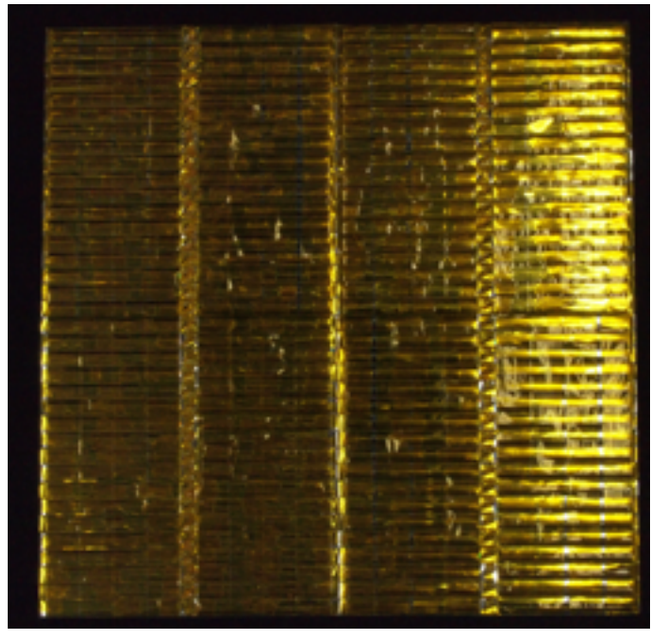
- Bottom side readout ScECAL prototype was developed.
- Prototype was tested at CERN PS beam line.
- Problem of noise arose from the combination of 10k pix. MPPC and SPIROC chip.
- High threshold setting for noise suppression affected to cut the MIP peak.
- Analysis is on going.

back up

Possible layout



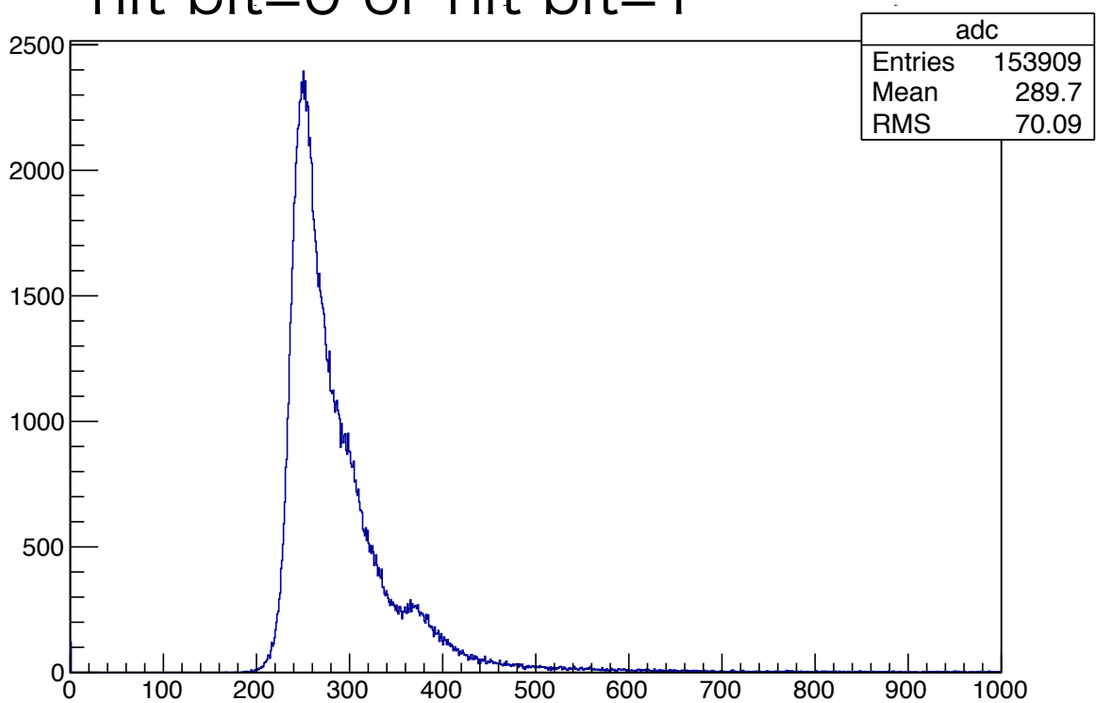
Assembly

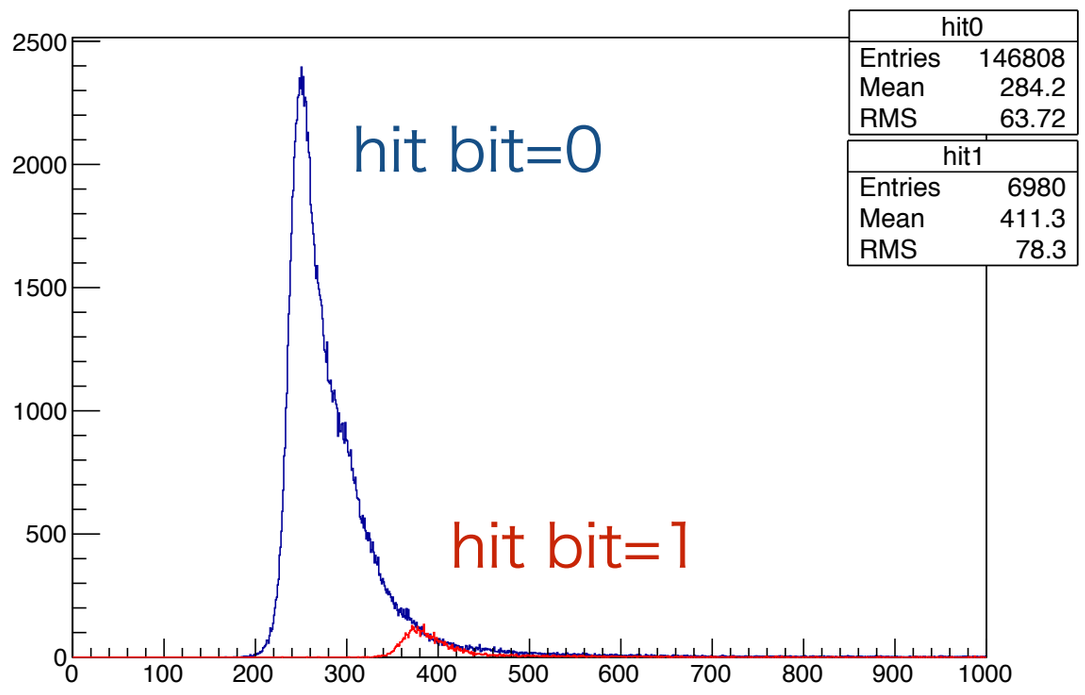








Status of EBU1

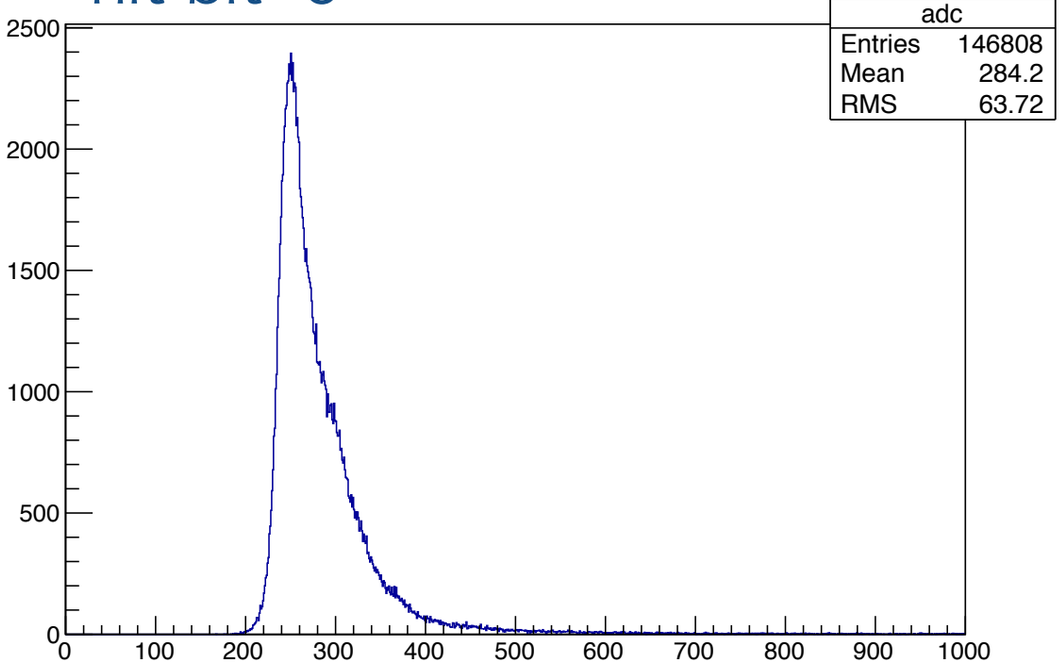
no event selection

hit bit=0 or hit bit=1

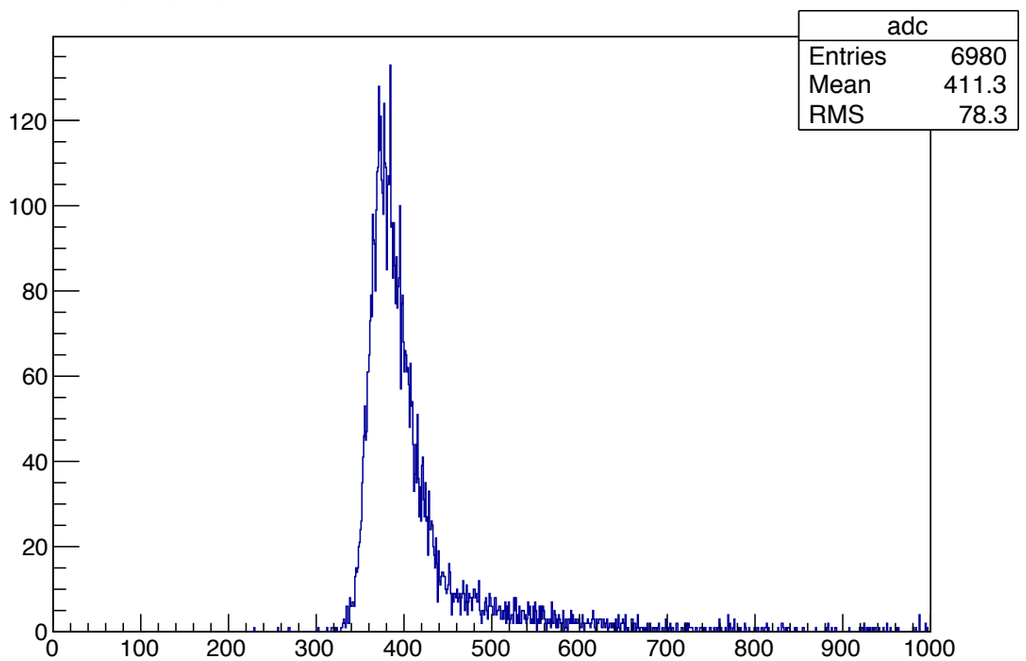


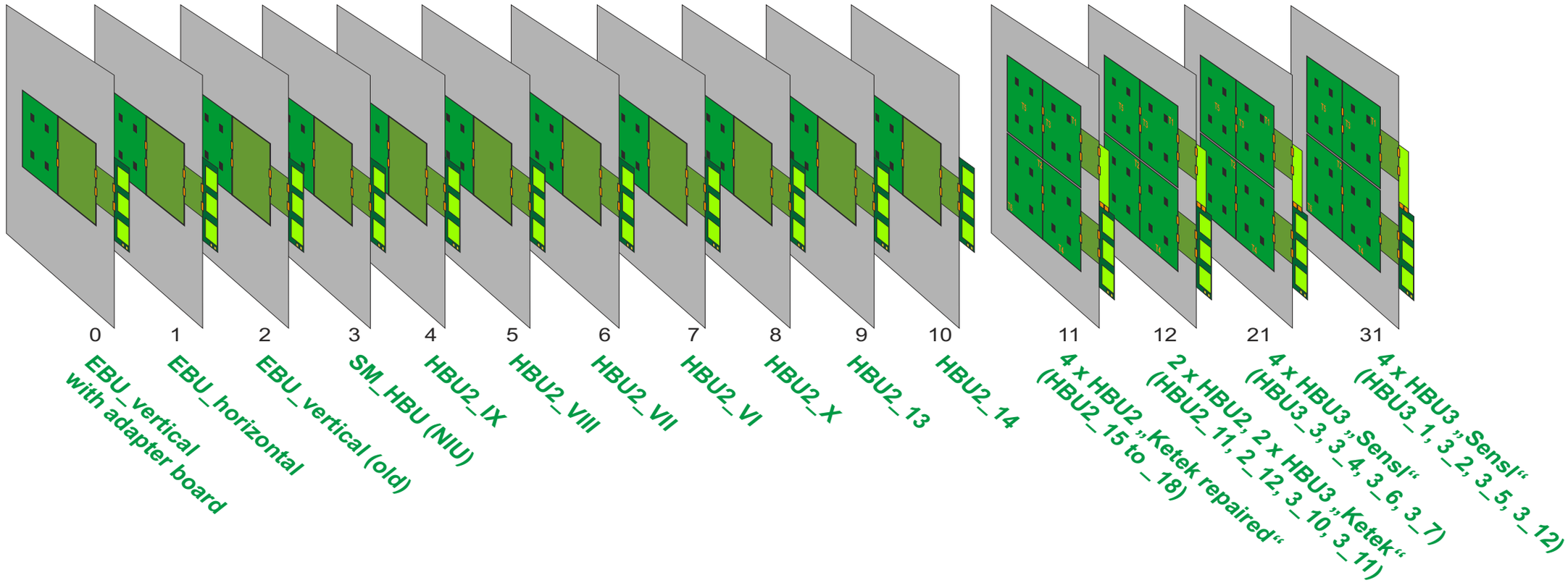


hit bit=0



hit bit=1



Layers

Position in stack	0	1	2	3	4	5	6	7	8	9	10	11	12	21	31
Layer (= DIF_ID)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Chip-IDs	129 -132	133 -136	137 -140	125 -128	141 -144	145 -148	149 -152	153 -156	157 -160	161 -164	165 -168	169 -184	185 -200	201 -216	217 -232