

# Development Status of Electronics and Cooling for ILC TPC

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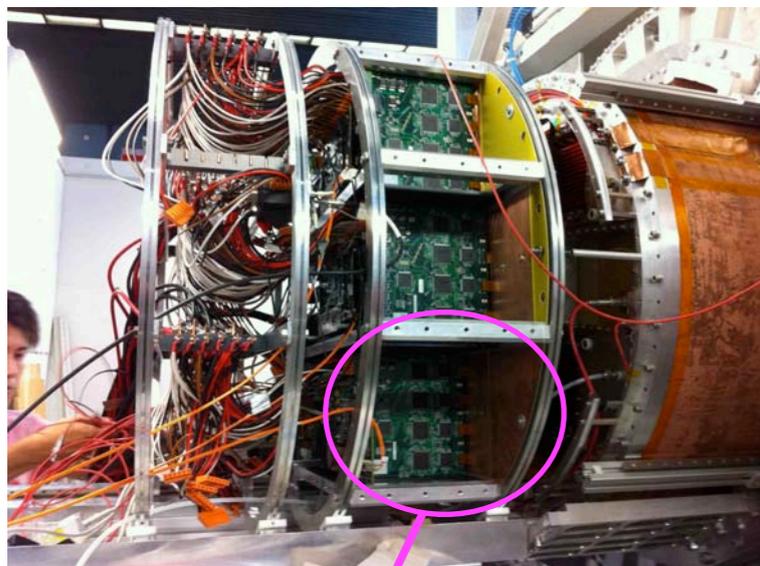
2014.12.17 ILC Tokusui Workshop @ KEK

# 1. Introduction

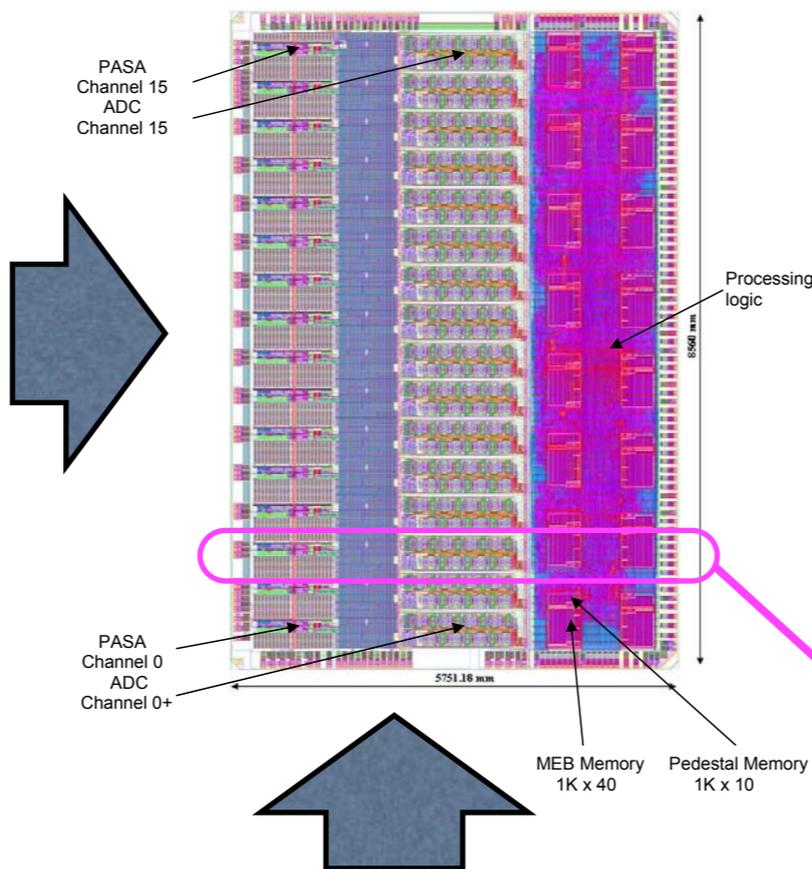
# Introduction:

## LCTPC Electronics Development for Pad Readout

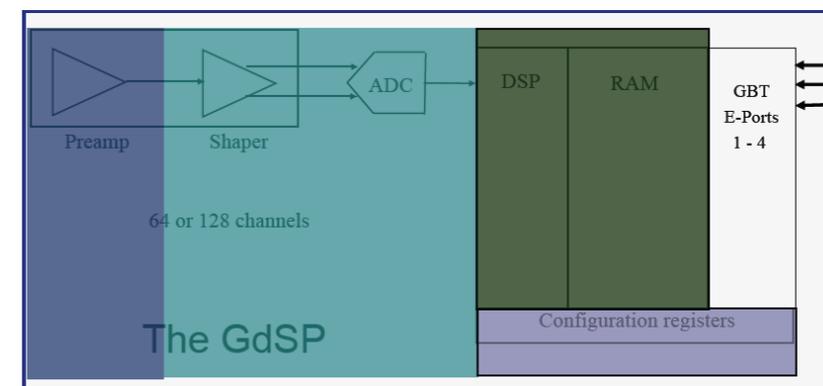
Large Prototype  
test so far



Next step  
S-ALTRO16 (fabricated)



Future GdSP

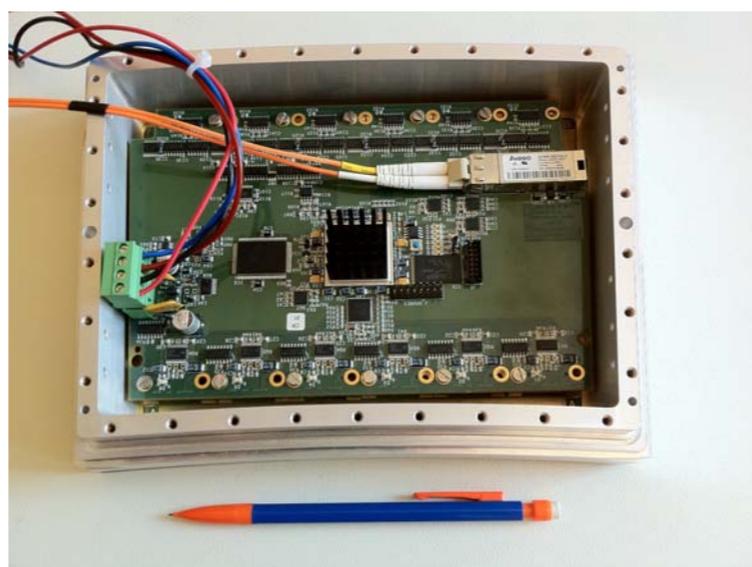


- 64 or 128 channels in a chip.
- Low power consumption (7-8mW/ch).

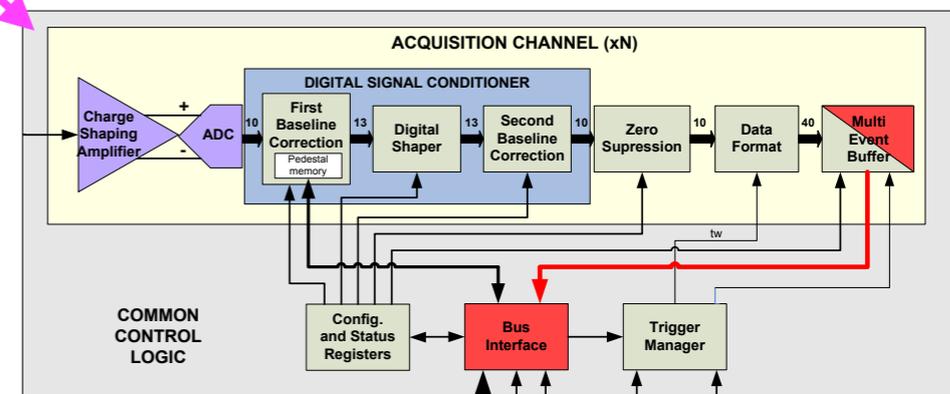
Front End Card



PCA16 (programmable) ALTRO



MicroMegas module with AFTER-based electronics



- Runs with Sampling Clock
- Runs with Readout Clock

- 16 channels in a chip.
- 59(42)mW per channel @ 40(20)MSPs.

# Outline

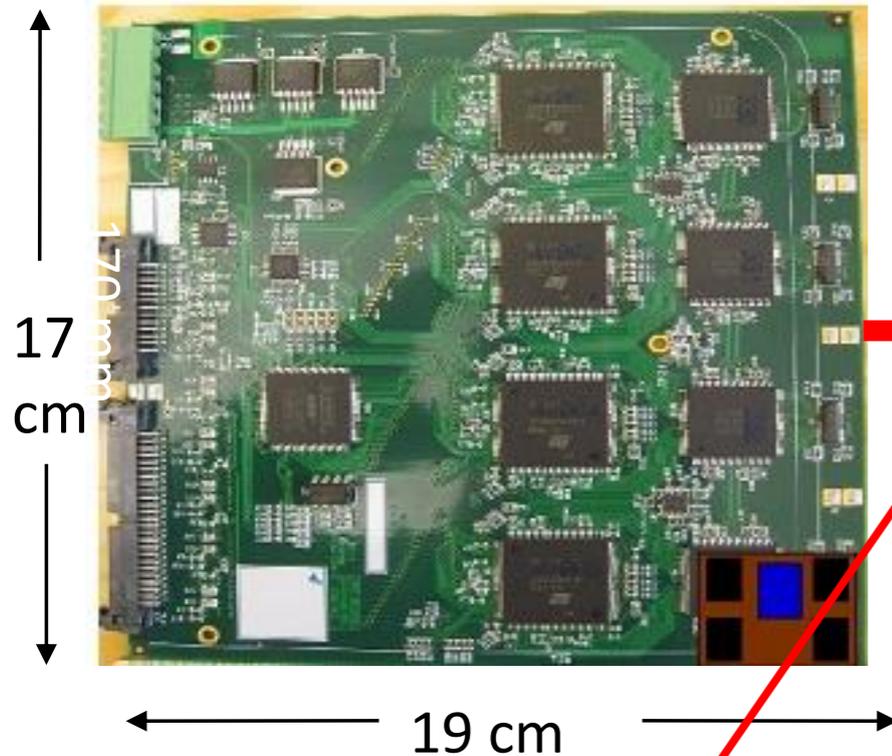
1. Introduction
2. Next module development
  - Evaluation of heat conducting plate
  - Evaluation of module cooling
3. Towards the final electronics
  - Readout chip specification
4. Summary

## 2. Next Module Development

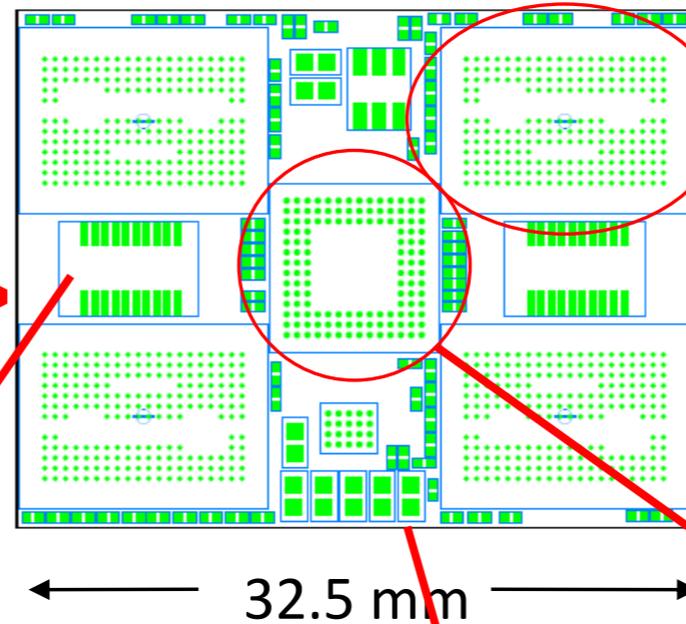
# From ALTRO to SALTRO16

A decrease in size by a factor 40 of the front end electronics

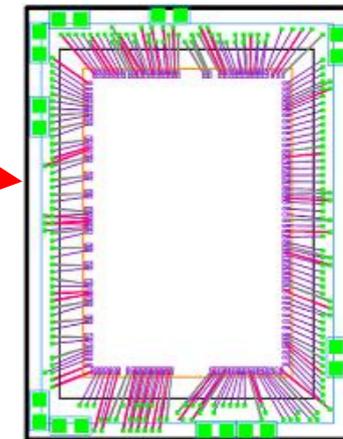
FEC with 8 ALTRO



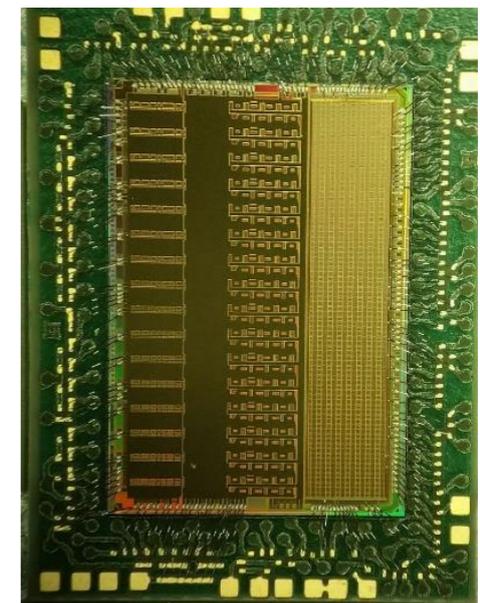
MCM with 8 SALTRO on carrier boards



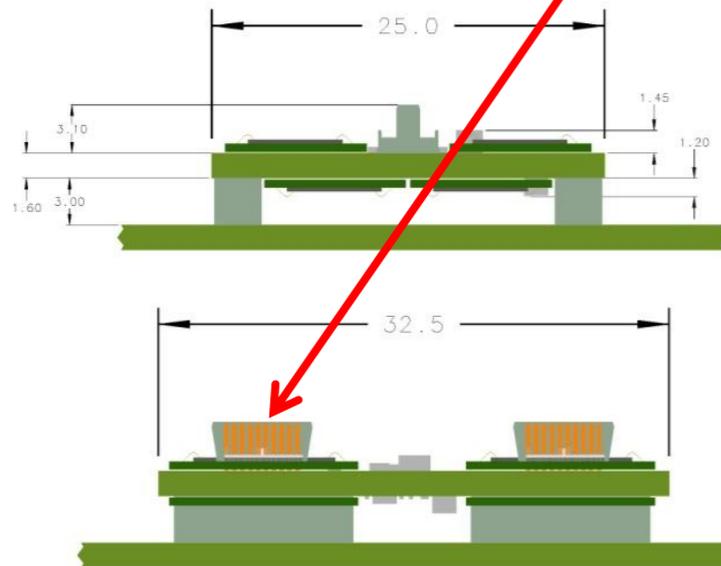
Carrier Board



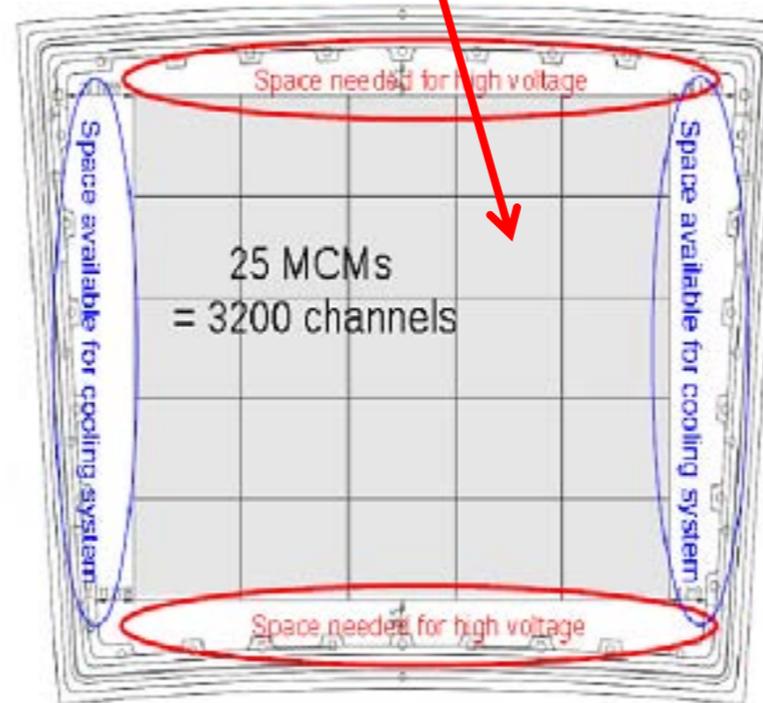
Carrier Board with SALTRO



Side views of an MCM

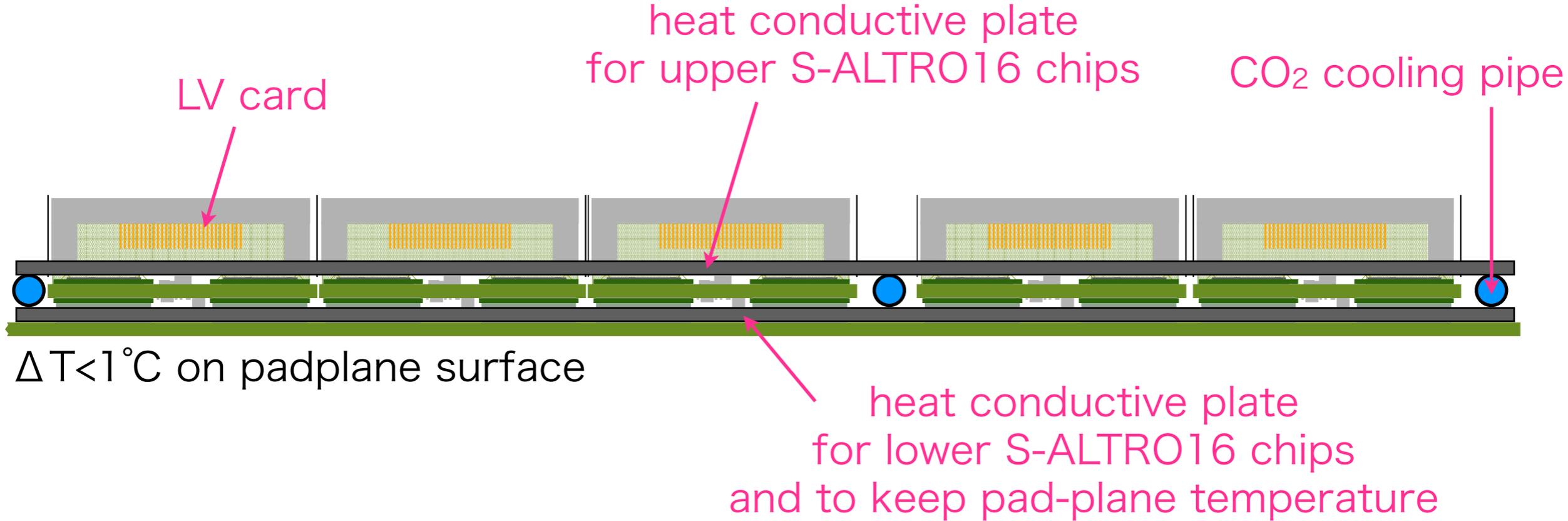
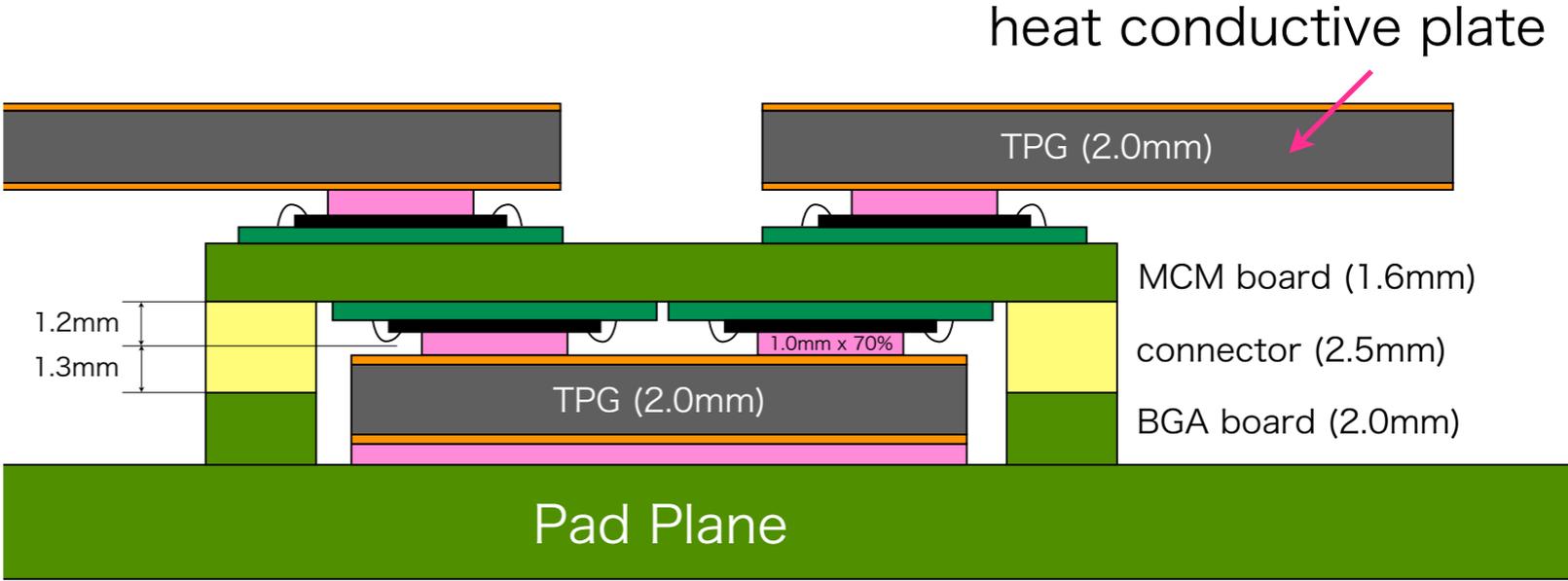
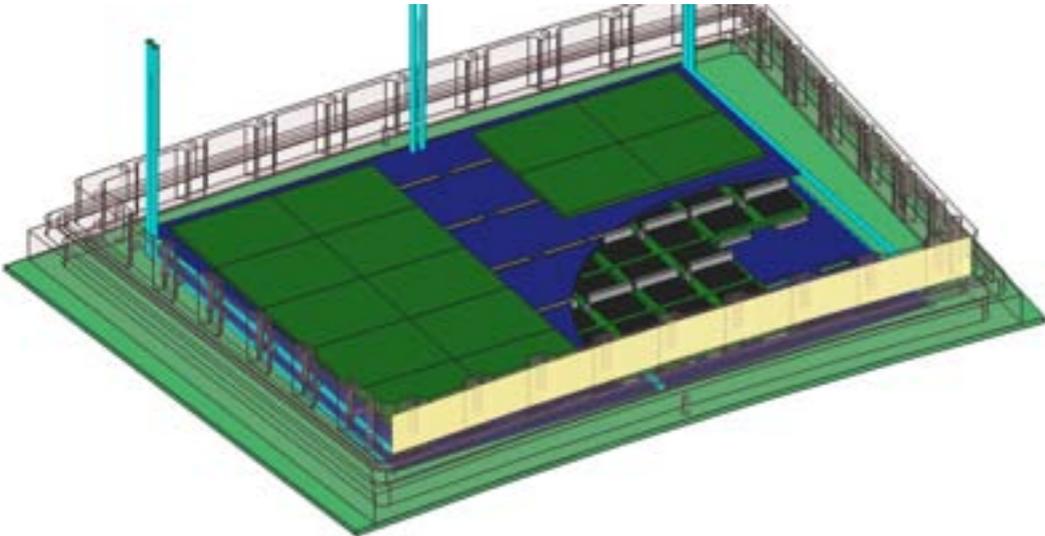


Pad Module



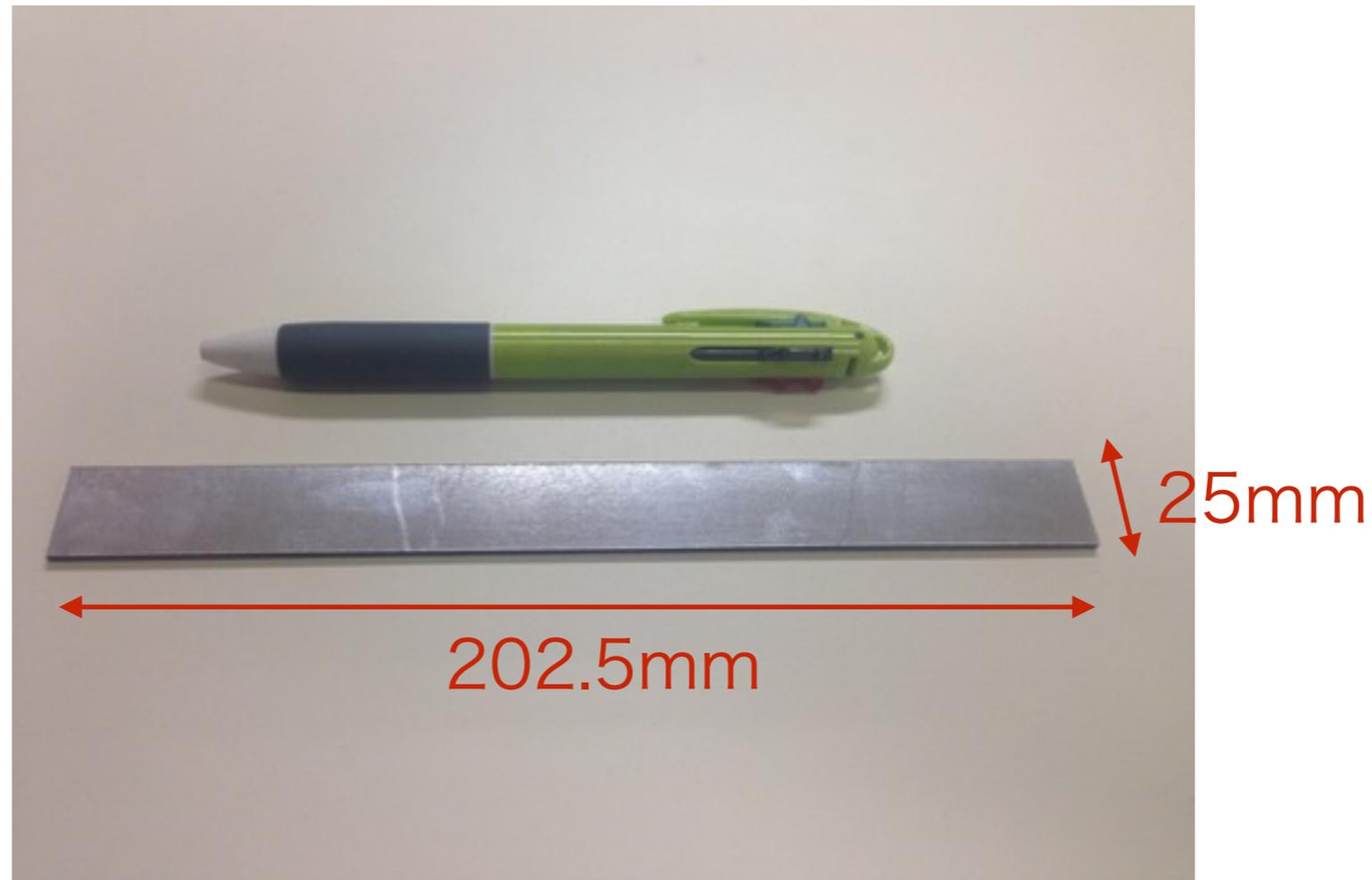
# Proposed Cooling for our next module

CO<sub>2</sub> cooling pipe



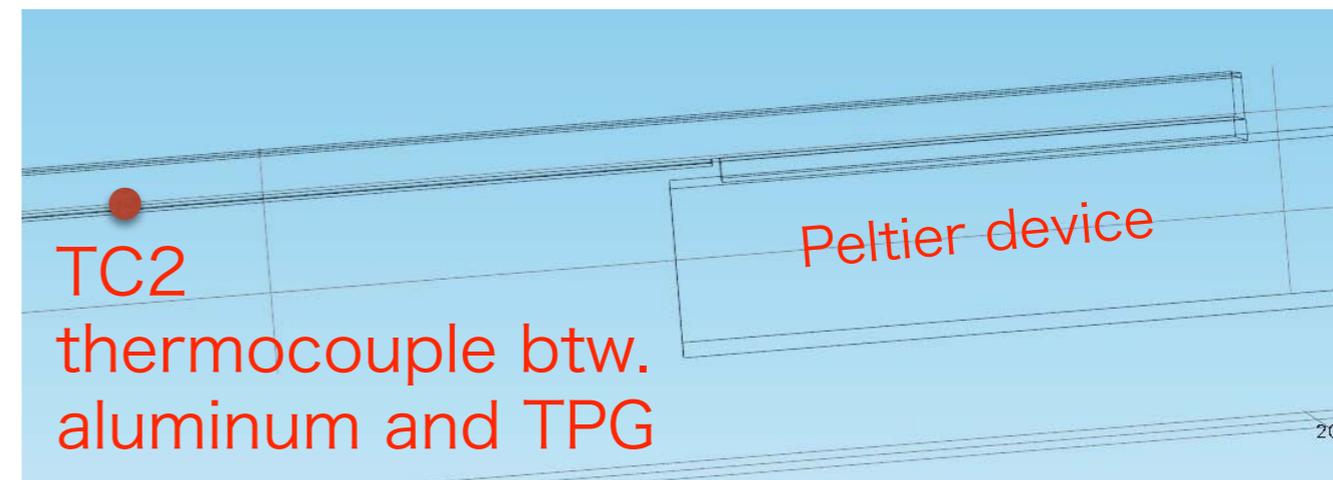
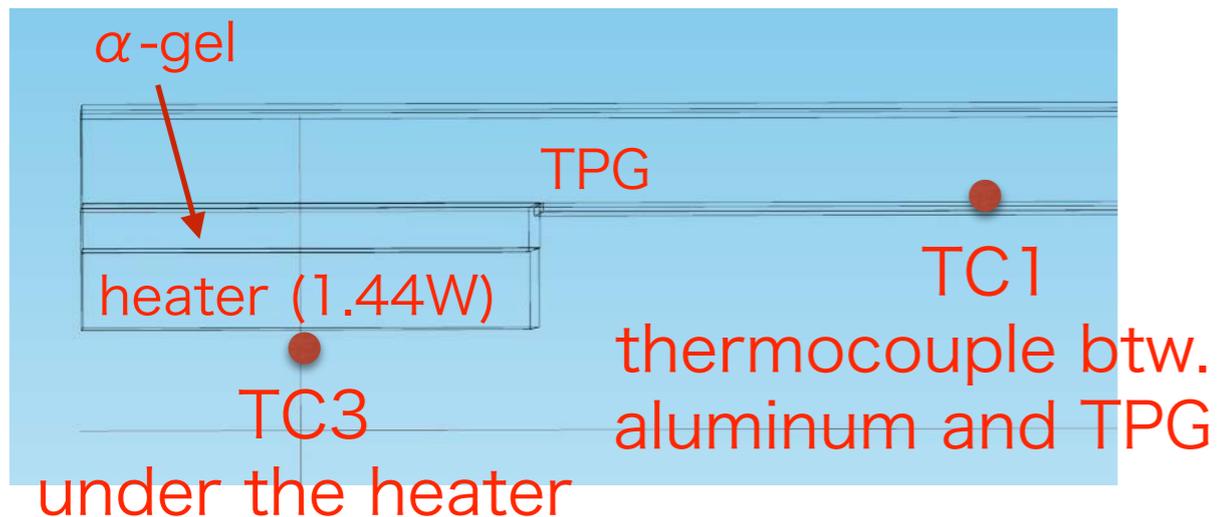
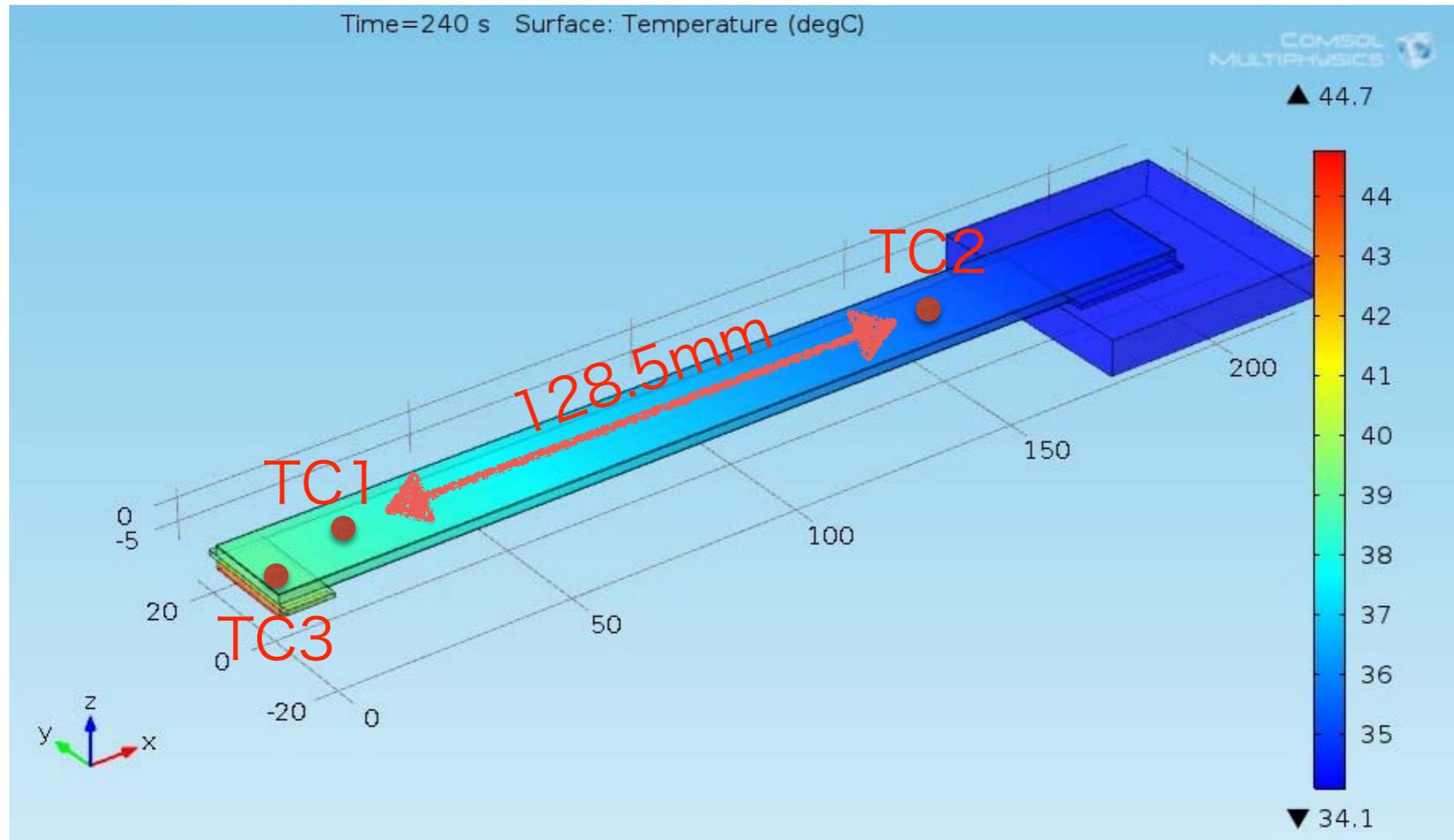
# Evaluation of Heat Conductive Plate, TPG

TPG (Thermal pyrolytic graphite) — high heat conductive plate by **MOMENTIVE™**  
 $\lambda \sim 1500 \text{ W}/(\text{m} \cdot \text{K})$  in plane and  $20 \text{ W}/(\text{m} \cdot \text{K})$  vertically

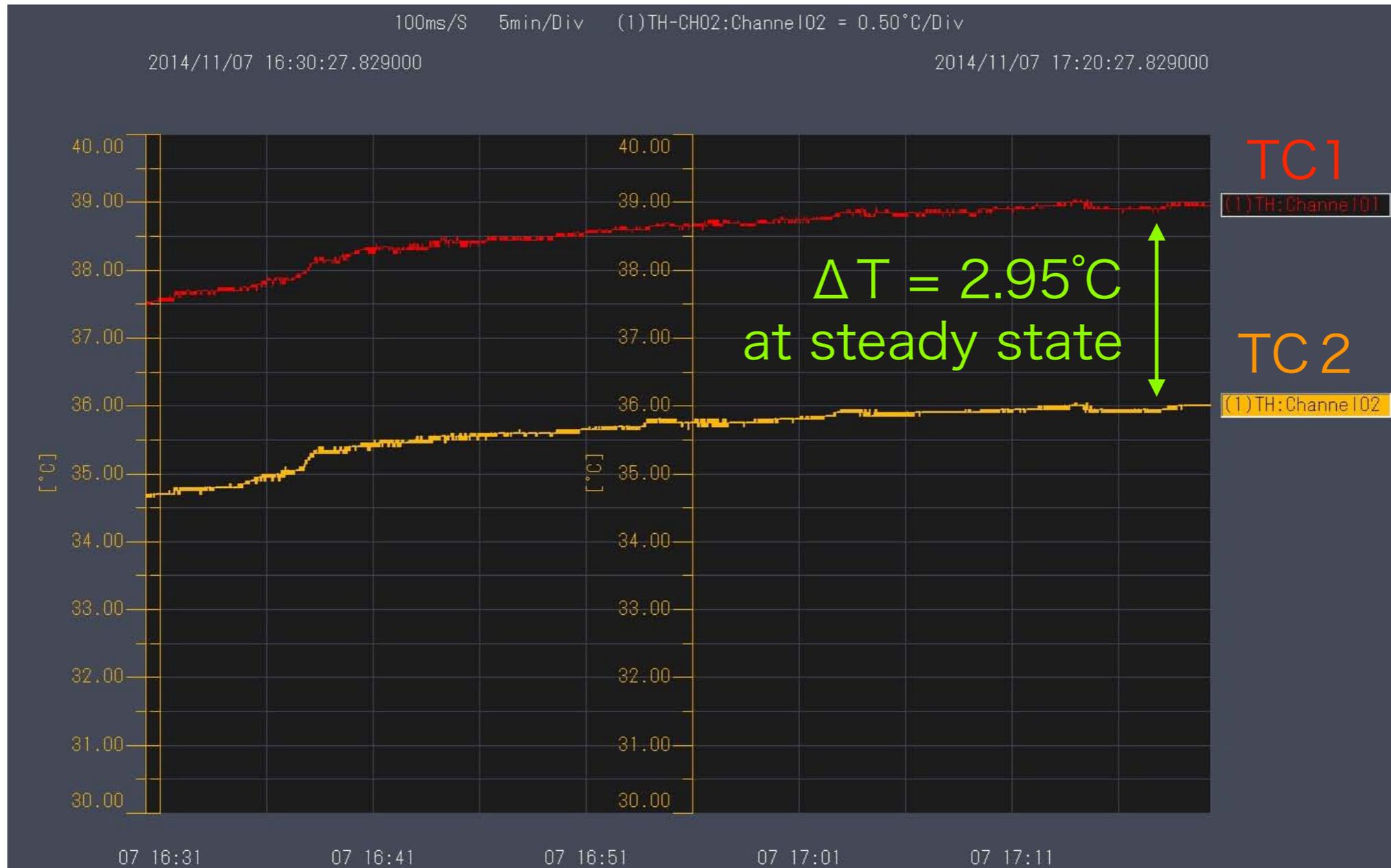


# TPG Measurement Setup

A ceramic heater as a heat source, a Peltier device as a heat sink.

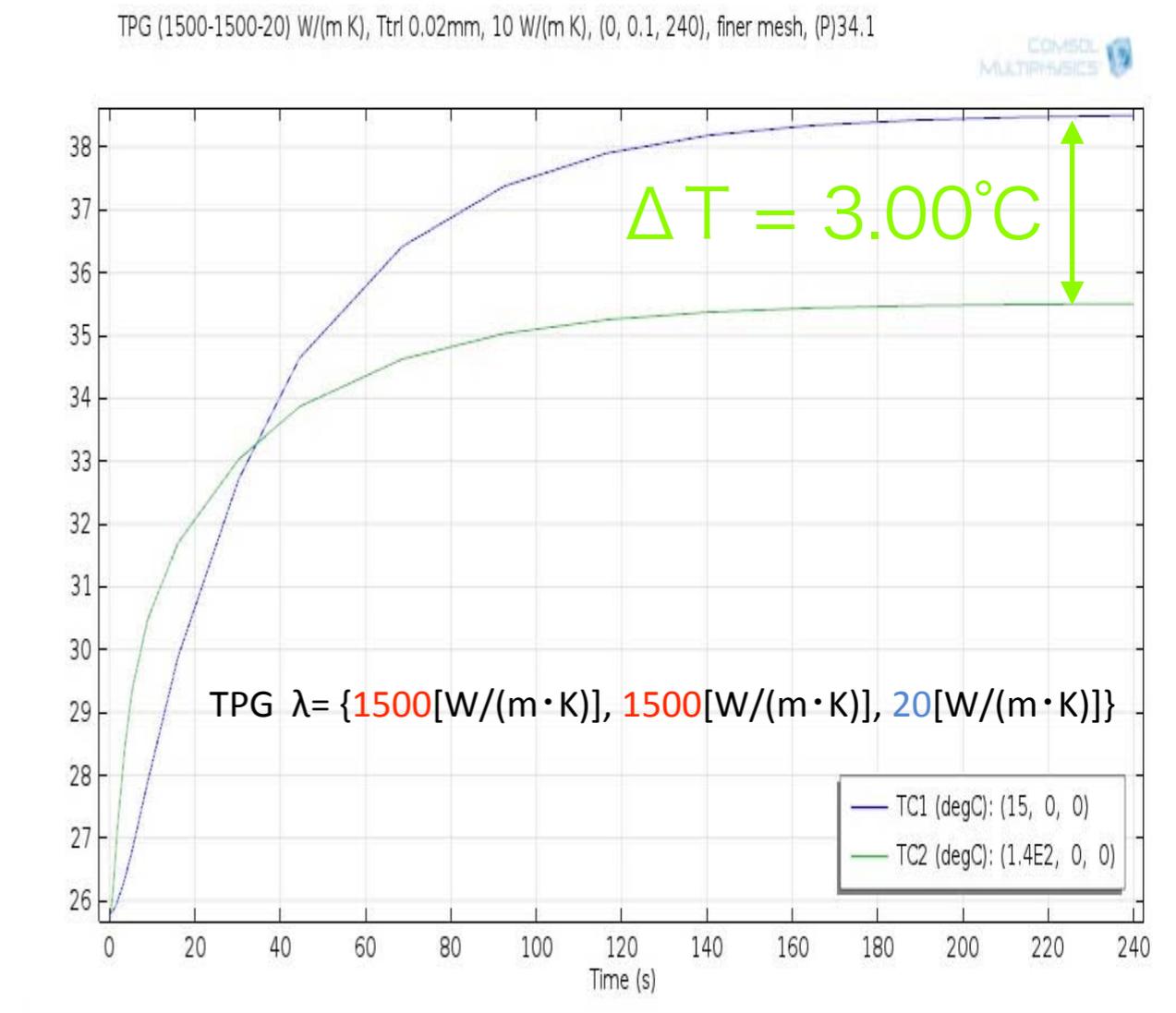
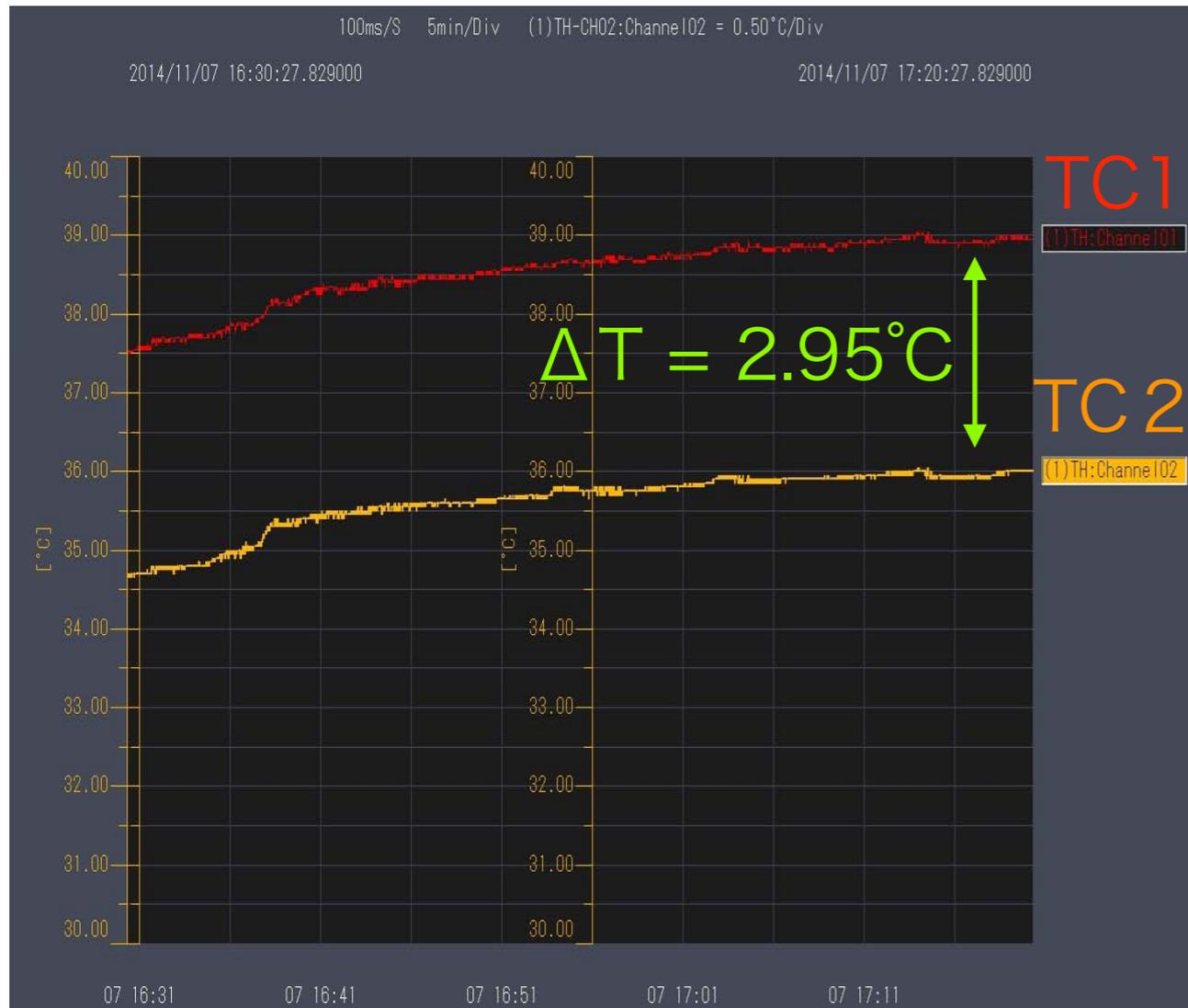


# TPG Measurement Results

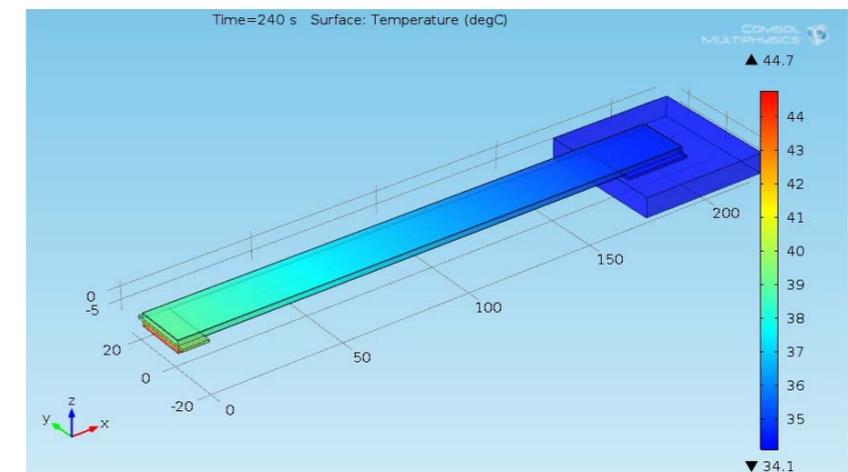


The steady state measurement gives thermal conductivity  $\lambda = 1526\text{W}/(\text{m} \cdot \text{K})$ , after subtracting the effect of aluminum laminate. The result is well consistent with the specification.

# Comparison with Simulation

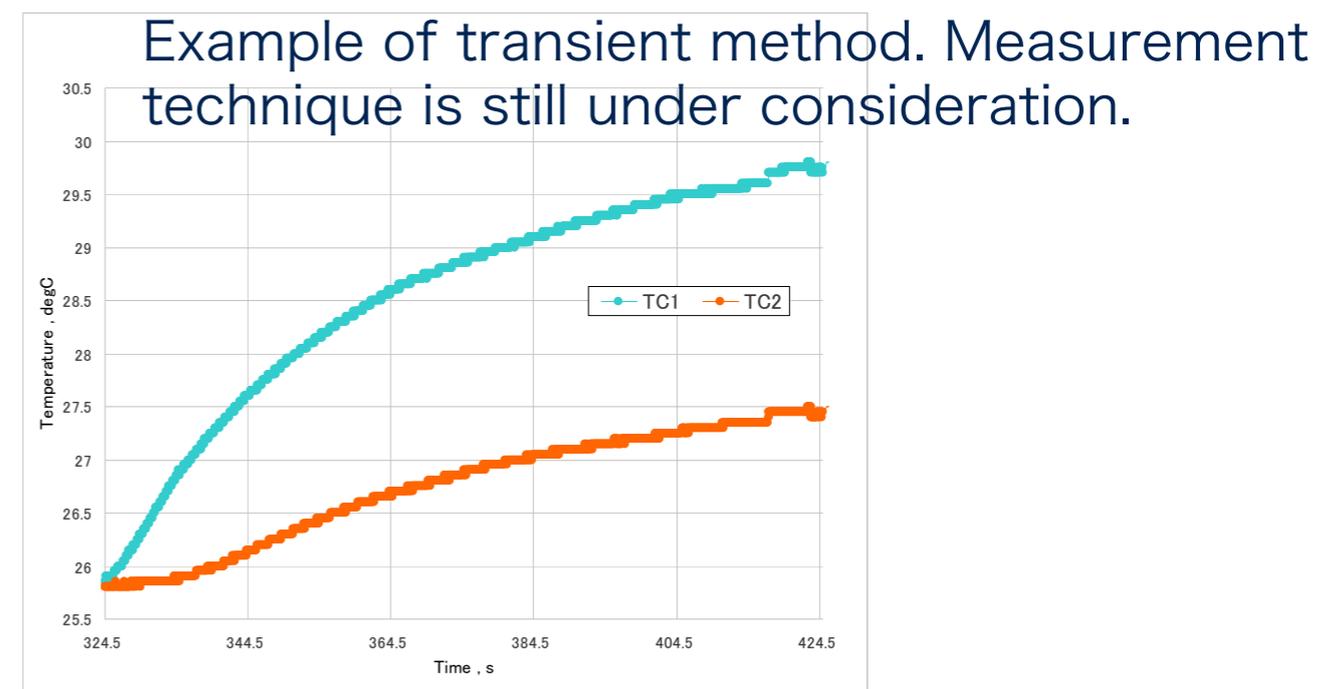
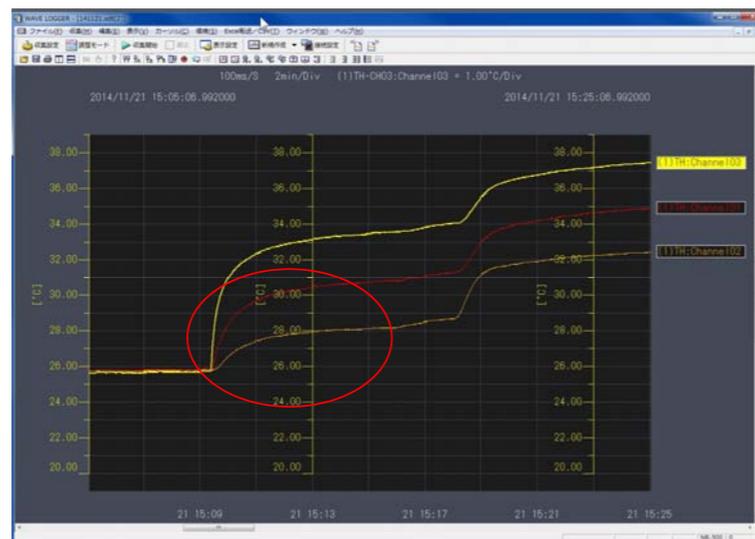


- Well explained by the simulation.



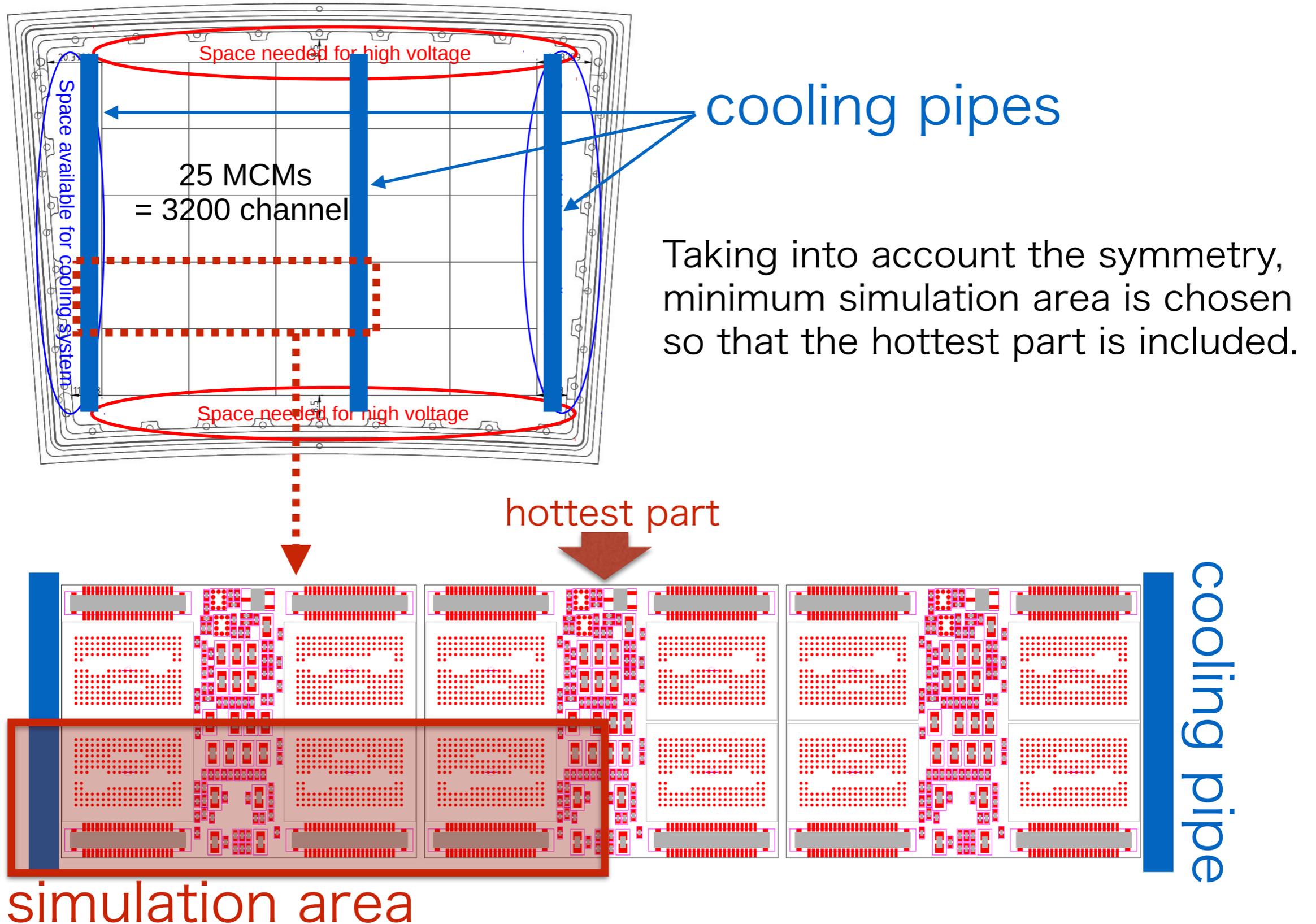
# TPG Evaluation Summary and Plan

- Thermal conductivity of TPG was measured with the steady state method. The value can be an input to the module simulation.
- Heat conductivity through the Al, glue and TPG is also important but not given by the specification sheet. It will be measured next.
- Instead of the steady state method, the transient method is also being tried, which is faster to obtain measurement results. This will be valuable to evaluate various alternative materials.



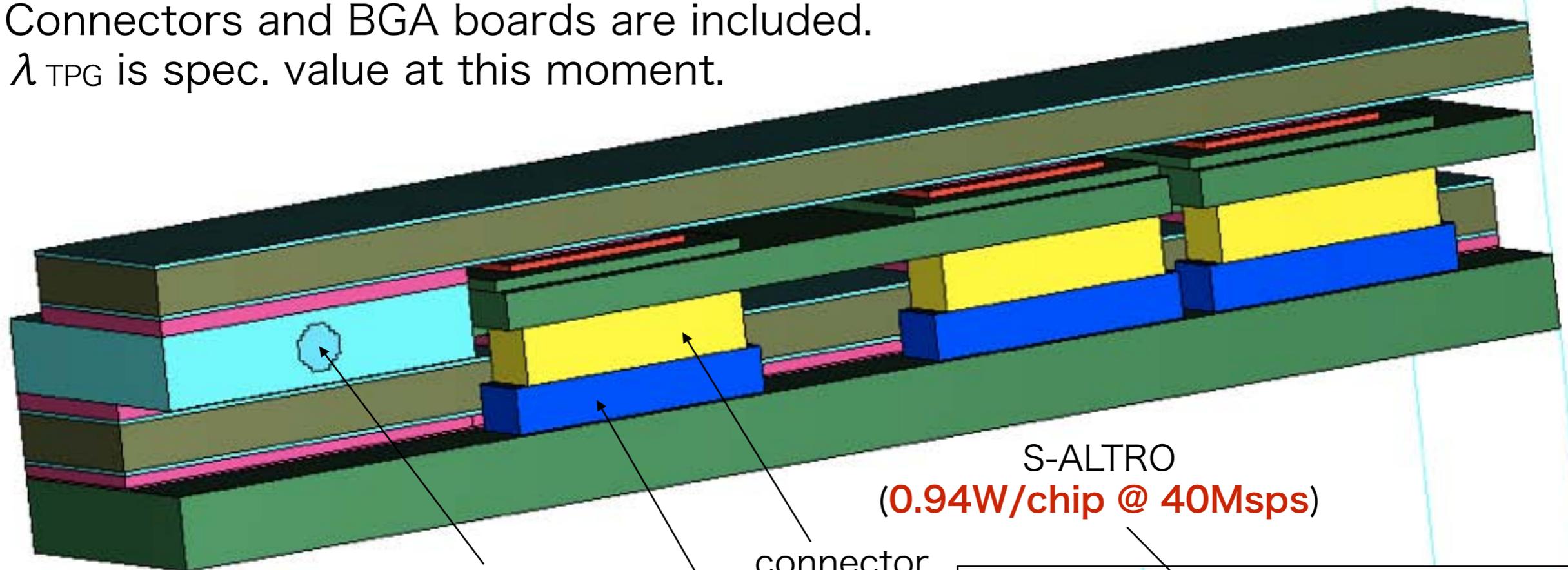
# 3D Thermal Modeling of the Readout Module

Two cooling pipes at the module sides and one near the middle.



# 3D Thermal Modeling of the Readout Module

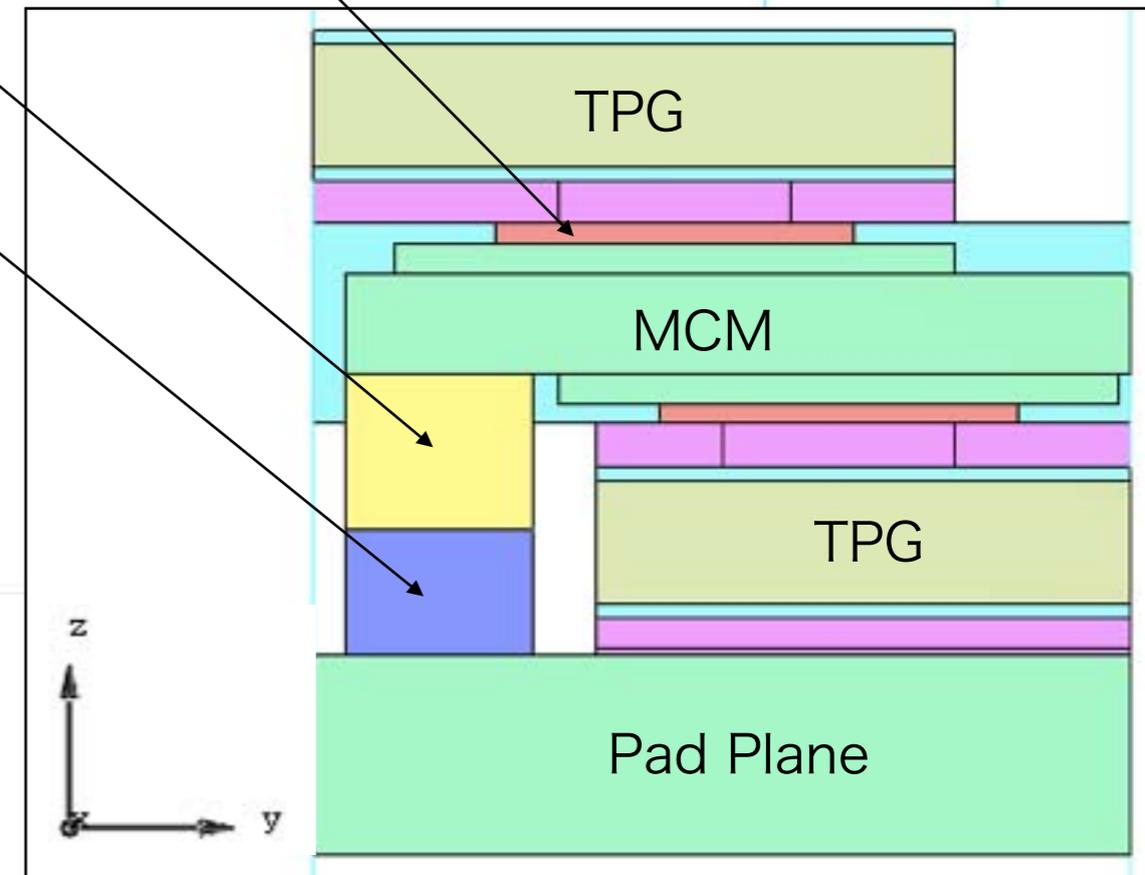
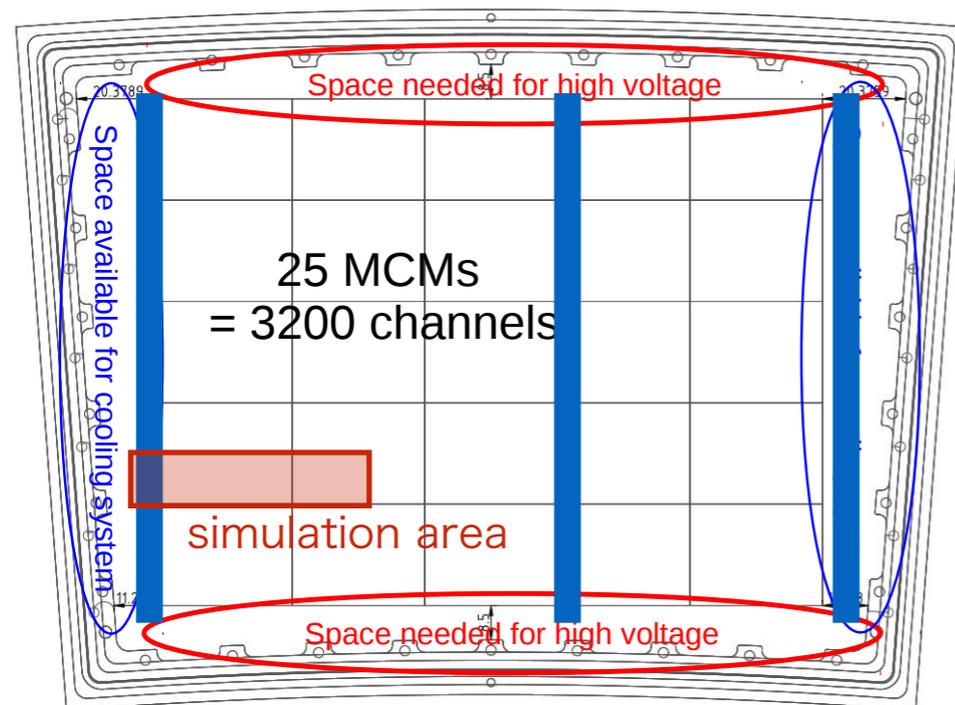
More precise modeling than before.  
Connectors and BGA boards are included.  
 $\lambda_{\text{TPG}}$  is spec. value at this moment.



cooling pipe  
(fixed to 20°C)

connector  
BGA board

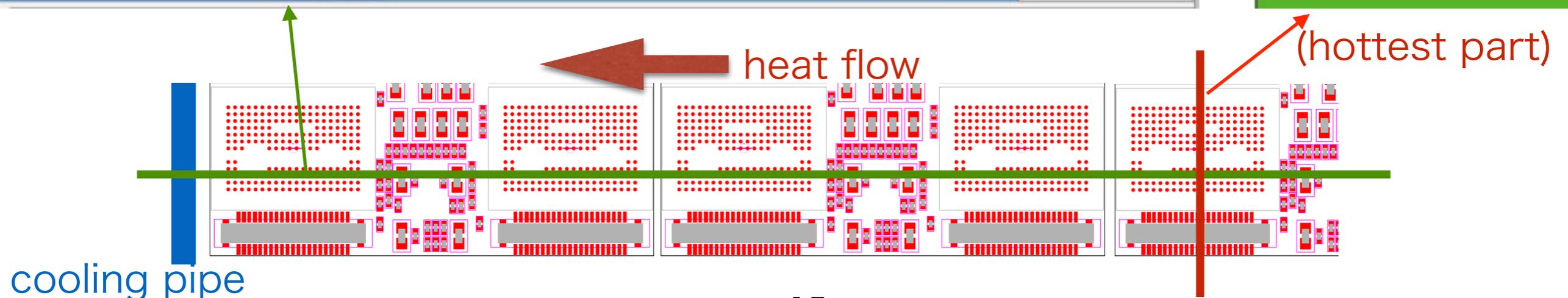
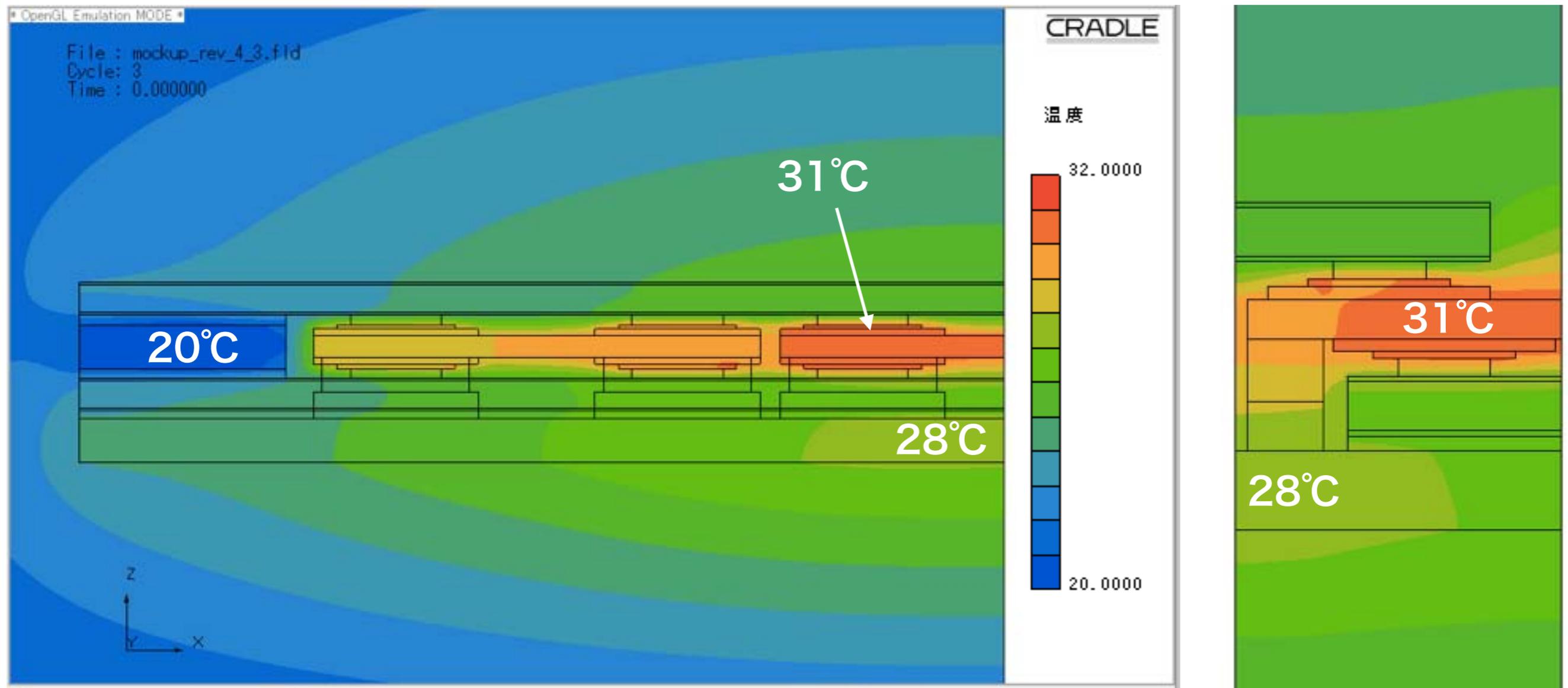
S-ALTRO  
(0.94W/chip @ 40Msps)



# Heat Simulation of the Next Module

$T(\text{S-ALTRO}) \sim 31^\circ\text{C} \rightarrow$  acceptable for the chip operation

$T_{\text{max}}(\text{Pad Plane}) \sim 28^\circ\text{C} = T(\text{pipe}) + 8^\circ\text{C} \rightarrow$  NOT acceptable for the final LCTPC



# What we know from the module simulation

- For the proposed design, temperature gradient will be about  $8^{\circ}\text{C}$  in the case of 40Msps operation w/o power pulsing.
- If the operation is at 20Msps,  $P(\text{chip})$  is 0.67W and the temperature gradient will be  $\sim 6^{\circ}\text{C}$ .
- Heat flow through the connector is not small. Because of this, pad plane temperature is near the chip temperature. Therefore, the chip at the “operational” temperature is not enough and should be relatively near to the room temperature.
- Via of the BGA board should be as thin as possible. Thermal contact between TPG and chips and the one between TPG and pad plane should be better.
- (mockup test will be performed)

# 3. Towards the final electronics

# Discussions on final ILC-TPC electronics

- Electronics meeting was held at Bonn on 18/Sep/2014.  
Materials can be obtained at  
<https://agenda.linearcollider.org/event/6507/>
- Exchanged information with ASIC experts.
- Options:  
ASIC process — keep IBM 130nm? move to TSMC 65nm?  
Digital filtering rather than analog shaping for baseline correction?  
Common Front End (CFE) project for analog part?  
Stack two or more different chips?
- Need to determine parameters by the physics aspects  
—> temporary values are listed in the next slide.  
—> These numbers have to be verified.

## Parameters of final ILD TPC

### 1.) List: Parameters driven by physics

Preamplifier: input capacitance (5-20 pF)

shaping peaking time (60-200 ns) Martin Ljunggren MSc

sensitivity (1-10 mV/fC)

polarity (negative)

dynamic range (SALTRO: 150 fC, AFTER: 120, 240,?,600fC) dE/dx

linearity error <1% for full dynamic range dE/dx

noise (<600 electrons)

Shaper: restoring to baseline in units of counts

at least 1  $\mu$ s for Micromegas (not to lose the signal on side pads)

ADC: number bits (8-10) Wenxin's thesis (Saclay), Liangliang's thesis (Lund) for spatial resolution

sampling frequency (20 - 40 MHz)

Time of continuous readout:  $\sim$ 800  $\mu$ s (full bunch train)

### 2.) List system driven by other considerations

Input leakage current compensation (if too high -> noise, but may be necessary, e.g. for protection diodes)

pad density (1/4 of smallest pad size per channel)

Power consumption: 4 mW/channel (without power pulsing) -> 20 W per Module (5000 channels) -> 1 kW per endcap with power pulsing (+ at least a factor of 5 in power reduction by power pulsing)

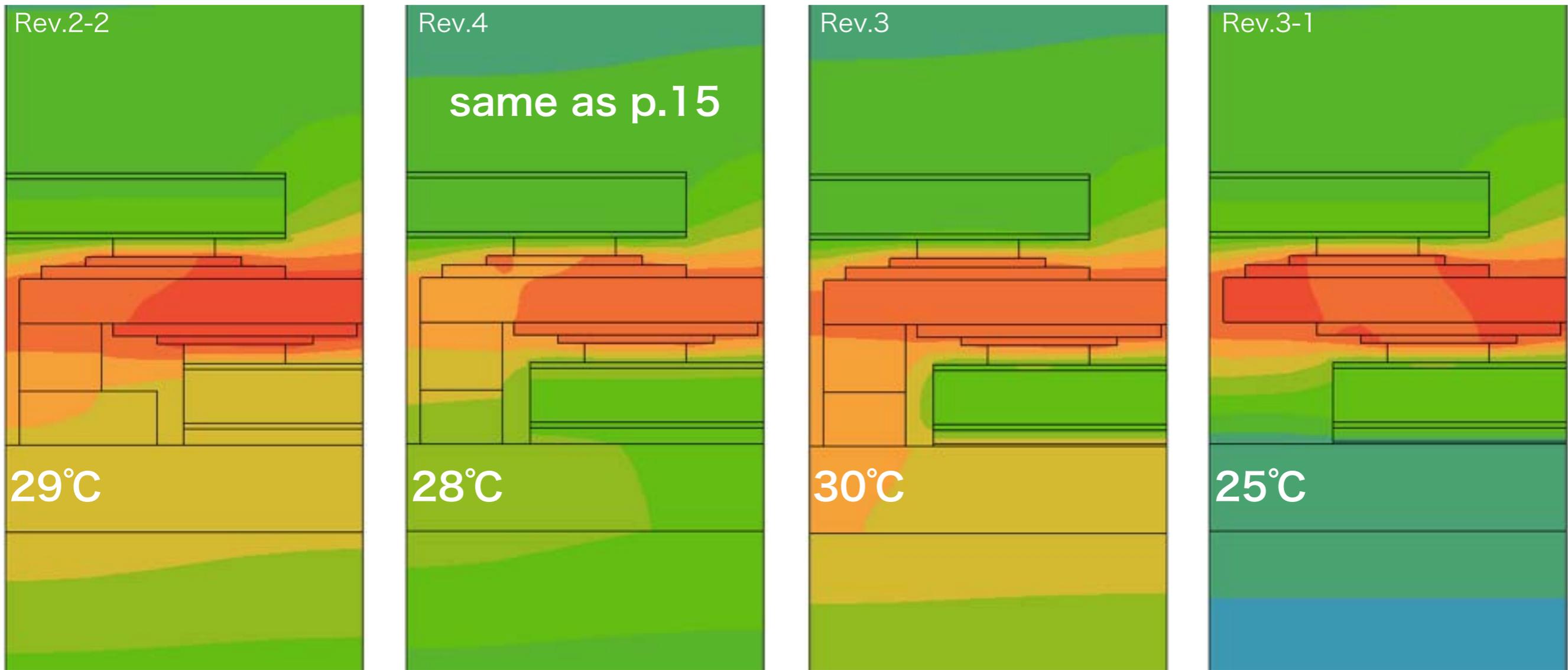
from <https://agenda.linearcollider.org/event/6507/>

# Summary

- For the next module development,
  - thermal conductivity of the TPG was measured, which is consistent with specification and well explained by simulation. The result will be a good input to the module simulation. Further study will be performed for improved measurements and for various alternative devices.
  - Thermal simulation of the next module was performed. The result shows rather large temperature gradient. More detailed study and mockup test will be performed.
- For the future final electronics,
  - a discussion group was formed and the first meeting was held. We listed specifications of the readout chip. Verification of the given spec. numbers is the next step.

Backup Slides

# Comparison btw. different cases



Wider BGA board,  
hence narrower TPG

Insulator to block heat  
from TPG to pad plane.  
This doesn't work at all  
because of heat flow  
through the connector.

Remove the connector  
to show that the  
insulator works well  
only when thermal  
contact btw. MCM and  
pad plane is small.