Overview of SiECAL and related DAQ development

Taikan Suehara
(Kyushu University, Japan)

Contents

- Current situation
- Combined DAQ
- Plans

ILD SiECAL Group

- Japan
  - Kyushu
    (Kawagoe, Yoshioka, Suehara, Sudo,
    Miyazaki, Ueno, Tomita, Hirai, Sumida, Takada)
  - Tokyo
    (Kamiya, Daniel, Kozakai, Chen, Nakanishi)
- France
  - LLR (Vladik, Vincent, Remi, Frederic,
    Jean-Claude, Henri, …)
  - LAL (Roman, …)
  - LPNHE
  - OMEGA (Christophe, Stephane, …)

History

- -2008: Physics prototype (external chip)
- 2012-13: First TB of Tech. prototype
  - SKIROC2 embedded, FEB8 assembly
  - HDMI/LDA/ethernet DAQ
- 2011: Kyushu joined
  - Sensor study, hybrid, attend TB
  - DAQ study (from 2013)
- 2013: Tokyo joined
  - Software, optimization, radiation study

General strategy in Japan

- Attendee → Core institute
  - Physics, Software and Analysis: OK
  - Sensor study: OK
  - Electronics and DAQ: in progress
    - LLR is the mainstream, LAL option
      We chose LLR to collaborate now
    - Necessary resource is gradually coming (eg. Slab)
- Small detector vs. Hybrid (cheaper ILD)
  - LLR prefers silicon-only small
    - Small degradation in performance, large gain in cost
  - We prefers to keep performance

ECAL and HCAL

Silicon ECAL

Scintillator ECAL

Shinshu

Kyushu

France

Same techno logy & DAQ

DESY

SDHCAL

AHCAL

Progress in this year

- Sensor study (Takada, Kozakai)
  - Stable temperature measurement
  - Crosstalk study with laser
    - Guard ring and edge
    - Inter pixel
  - MIP peak and RI source
- DAQ (Hirai, Suehara)
  - Injection study, RI, TB, combined DAQ
- Optimization & Software (Sumida, Daniel)
  - Garlic, layer optimization

Combined DAQ

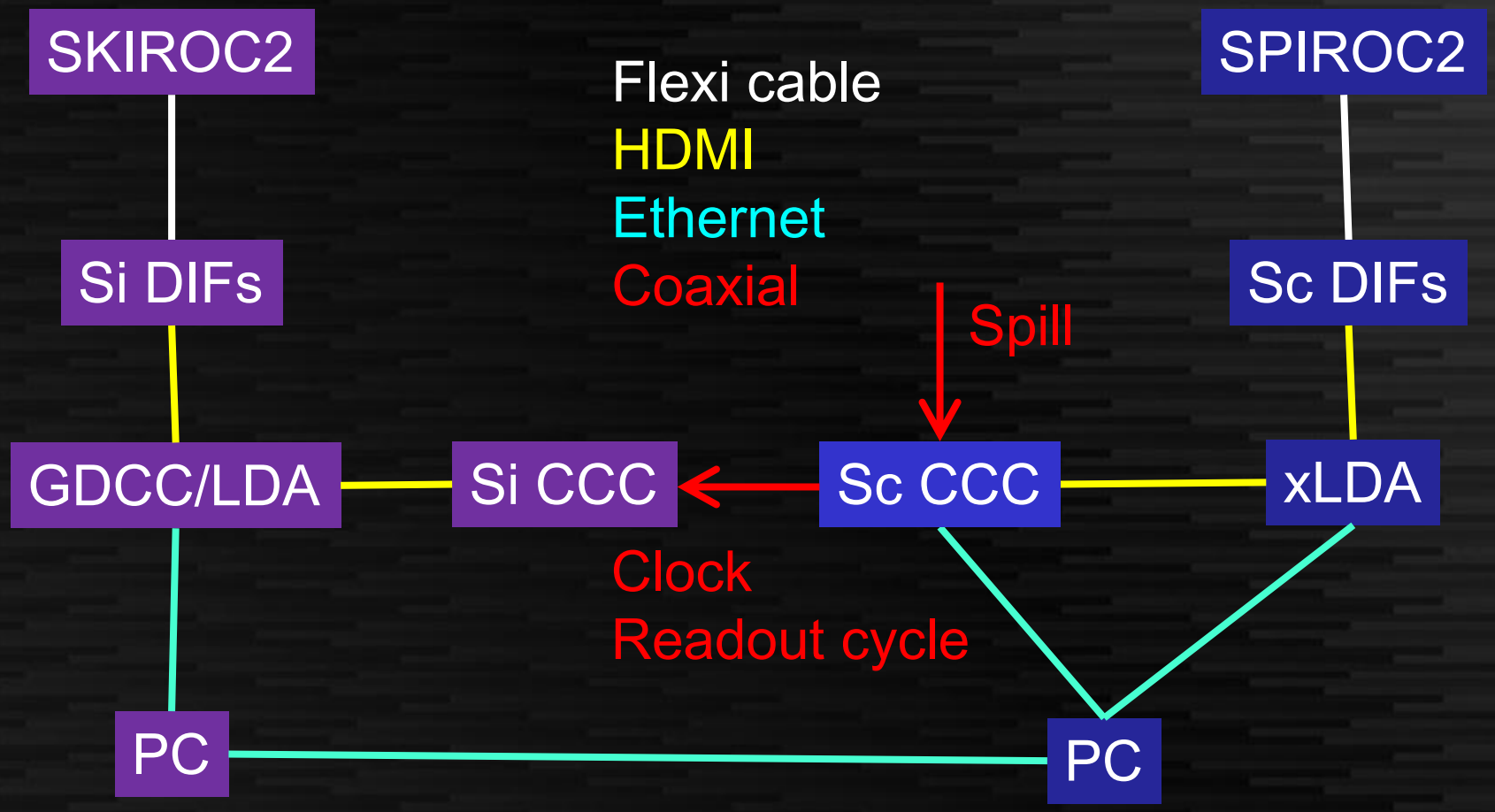
Combined DAQ: overview

- All CALICE Tech. proto. are based on the same chip family – ROC chips by Omega
- There existed a common DAQ elec. by UK
- Needs for common DAQ
  - Minimal effort in total
  - Common TB (towards real experiment)
  - Hybrid (Si + Sc)
- Groups are rival as well as collaborators
  - Need ‘neutral’ common system – difficult
  - Kyushu is at the good position for neutrality

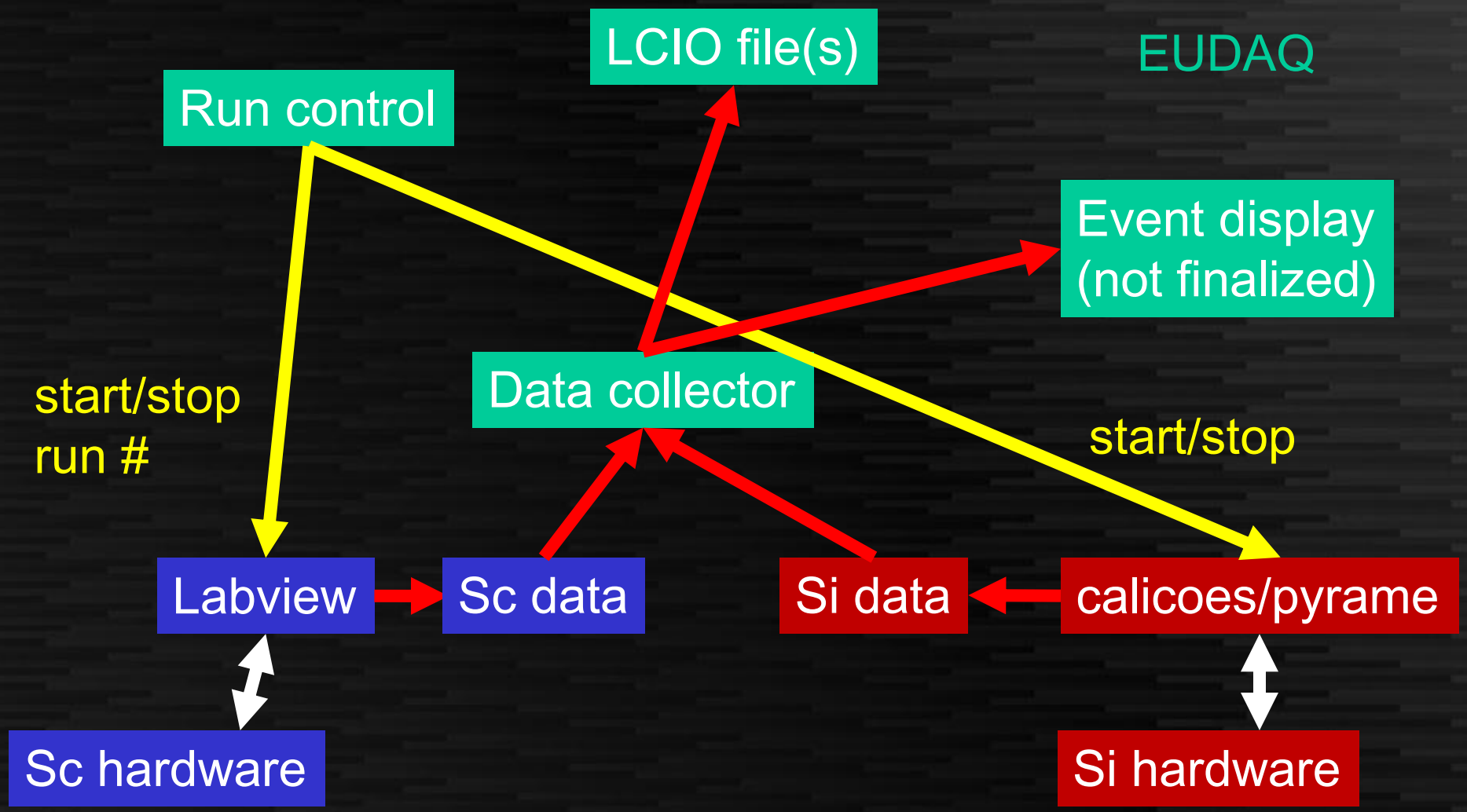
Sc + Si TB at CERN

- Nov. 26 – Dec. 8, 2014, CERN PS
  - 2nd period of Scintillator testbeam
- 15 Sc layers (3 EBU + 12 HBU)
- 1 Si layer (FEB8, from Kyushu)

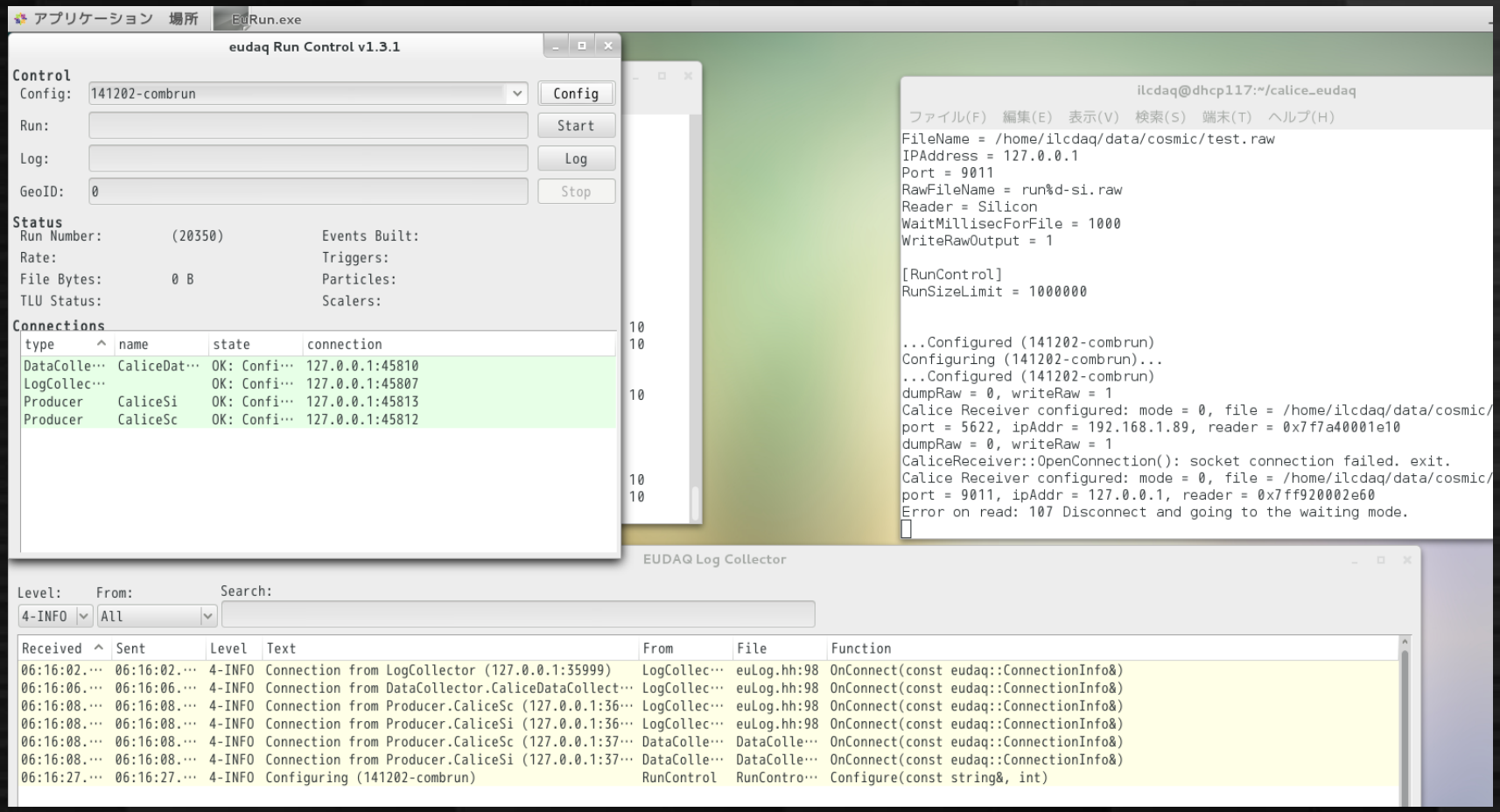
Si and Sc DAQ in TB 2014



Combined DAQ for Si + Sc



Screenshot of EUDAQ



Master PC (Linux): EUDAQ + CALICOES (Silicon)
Slave PC (Windows): LabView (Scintillator)
Successfully took data for more than a week

Next step: CALICE DAQ TF

- The first trial is successful, but many adhocs
  - Independent CCC
  - No busy synchronization
- Task force for CALICE-wide DAQ formed
  - Silicon: Remi, Frederic, TS (coordinator)
  - Scintillator: Mathias, Jiri
  - SDHCAL: Laurent
- Next TB: Si+SDHCAL next year (probably)

Personal comparison

	SiECAL	ScE/AHCAL	SDHCAL
Manpower	**	***	*
Strategy	Minimal mod	Full replace	Minimal mod
CCC	UK original	ZedBoard	DCC
CCC clock	50 MHz	40 MHz	50 MHz
8b/10b encode	yes	No	yes
BX clock (TB)	2.5 MHz	250 kHz	
DIF-LDA	HDMI	HDMI	USB+HDMI?
LDA	GDCC	ZedBoard	Raspberry+DCC
LDA-PC	Ethernet raw	TCP	TCP
Software	Calicoes	Labview (tentative)	DIM (from DELPHI)

Things to be considered

- Common master clock frequency
  - To assure simultaneous BX counting
- Common BX clock frequency
- BUSY treatment
- → Common CCC? or just clock synchronization?
- High level DAQ software (EUDAQ?)
  - Run control, event building, run number, monitoring,…
- Common data format (LCIO class)

- Partial or optional sharing of firmware and software
- etc.

Plans

Plans towards the “final” slab

- 2015: FEB11 long slab, TB
  - Design: LLR, we may try to produce
- 2015 or 16: SKIROC3 production
  - Our contribution: SKIROC test board
- 2015: Sensor specification finalized
  - Thickness, guard ring, radiation
- 2016 - 17: production of full layers
  - Test facility will be at Kyushu
- 2017 - 18: Full layer TB
  - SPS? J-PARC?

Plans of optimization

- Two candidates (my personal opinion)
- Small, fewer layers, Si+SDHCAL
  - Solid, less effort on calibration
  - Performance degraded
- Large, Si (ECAL) +Sc (M+HCAL)
  - Keep DBD performance
  - More careful calibration needed
  - We will optimize this option in detailed study
    - # layers, thickness, pixel size
    - Ration of Si/Sc, Strip/tile
    - How to calibrate