Strip AHCAL performance and test beam results

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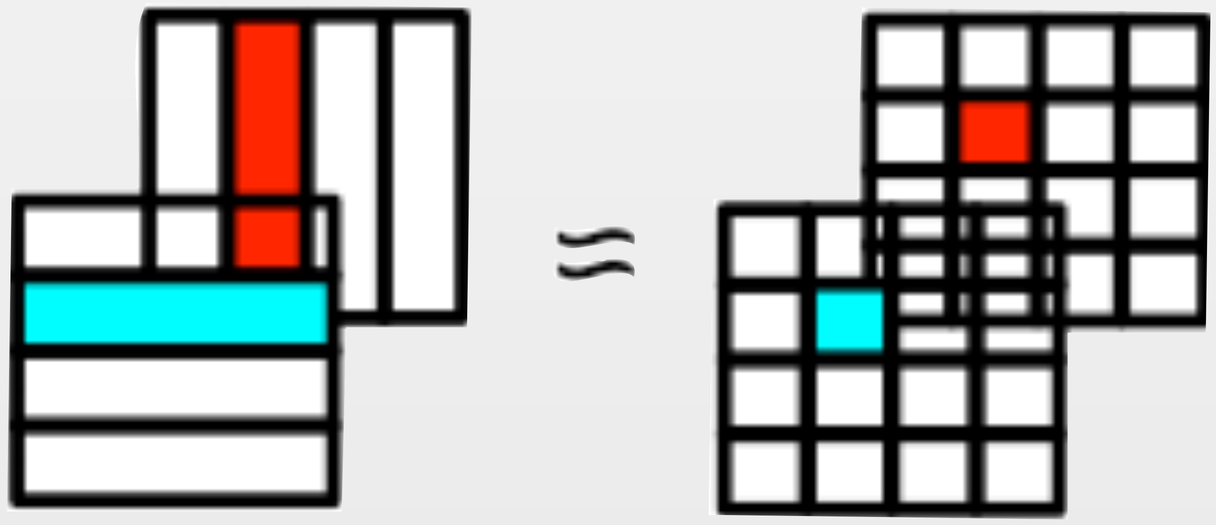
Motivation

- Pixel size of Digital HCAL is 10mm x10mm so far.
- Digital HCAL has good capability for position measurement.
- Analog HCAL has good performance on energy resolution.
- and Semi-digital HCAL is being developed.
- We think another way to make 10mm x 10mm segmented “full analog” HCAL by using scintillator strip technology.
- potentially good performance is expected.
- Challenge is to apply the strip splitting algorithm to the MIP like tracks close in hadron and EM cluster.

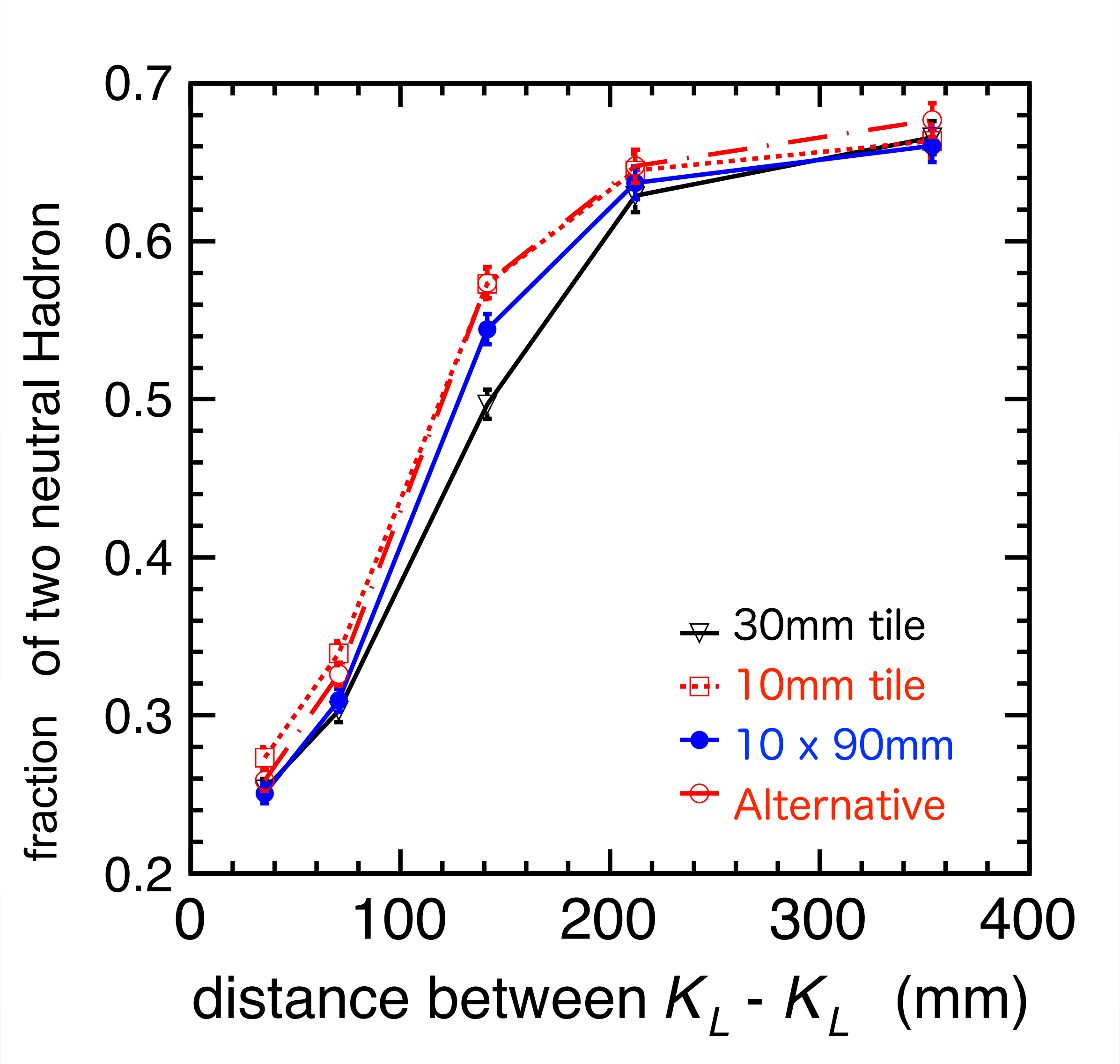
Strip AHCAL

- We choose 90mm x 10mm scintillator because it covers the same area 9cm^2 as 30mm x 30mm tile AHCAL.
- Strip directions are orthogonal to those in the neighboring layers.
- Effective segmentation is 10mm x 10mm.
- Further improvement is expected with tile layers between strip layers. (alternative)

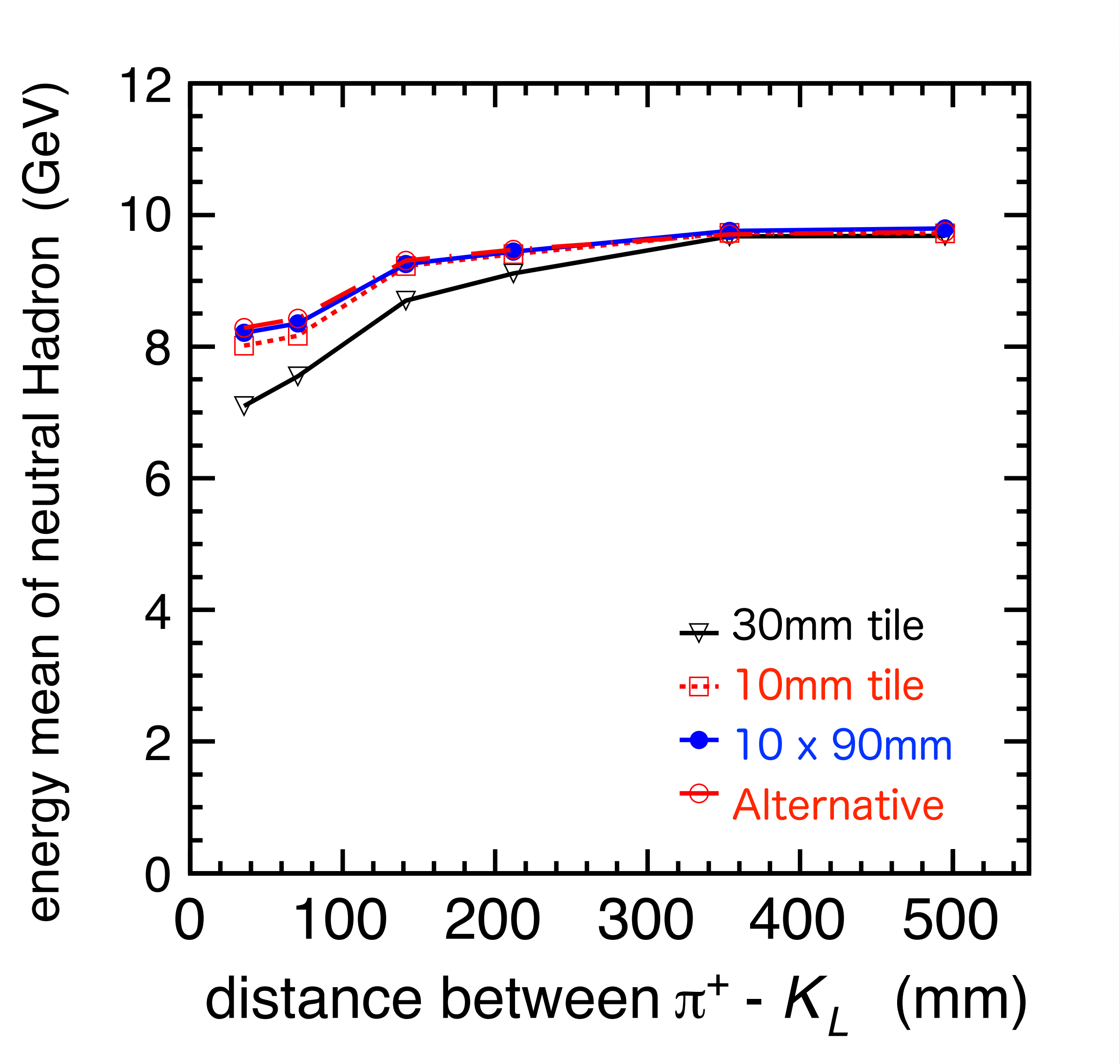


Particle separation

Fraction of events successfully reconstructed as two K_L events v.s. particle distance.



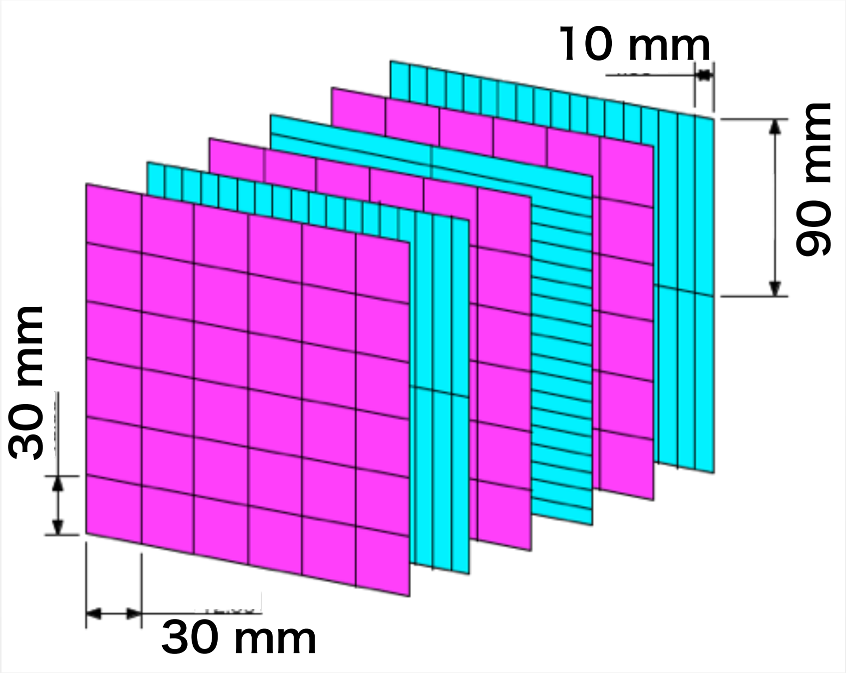
Reconstructed energy of 10 GeV K_L injected together 30 GeV π^+ v.s. particle distance.



less than 200mm distance, 10mm x 10mm segmentation makes better separation than 30mm x 30mm.

uds jet simulation and other

- uds Jet simulation on going
- need Optimize Parameter
  - detector parameter
    - calibration
    - time window
    - etc.
  - Sc size
    - $10x10mm^2$, $15x15mm^2$ tile
    - $90x10mm^2$, $180x10mm^2$ strip
    - altanative option ($90x10mm^2$ with $30x30mm^2$)
  - PFA parameter



altanative

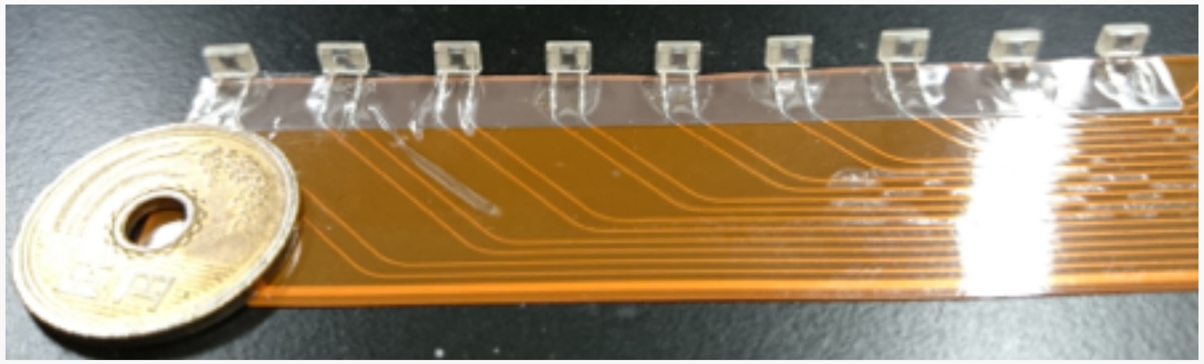
Test Beam

- CERN PS TB at Oct. 2014
- 4 Layers
- DAQ system
  EASIROC-NIM MODULE
- Run stand alone

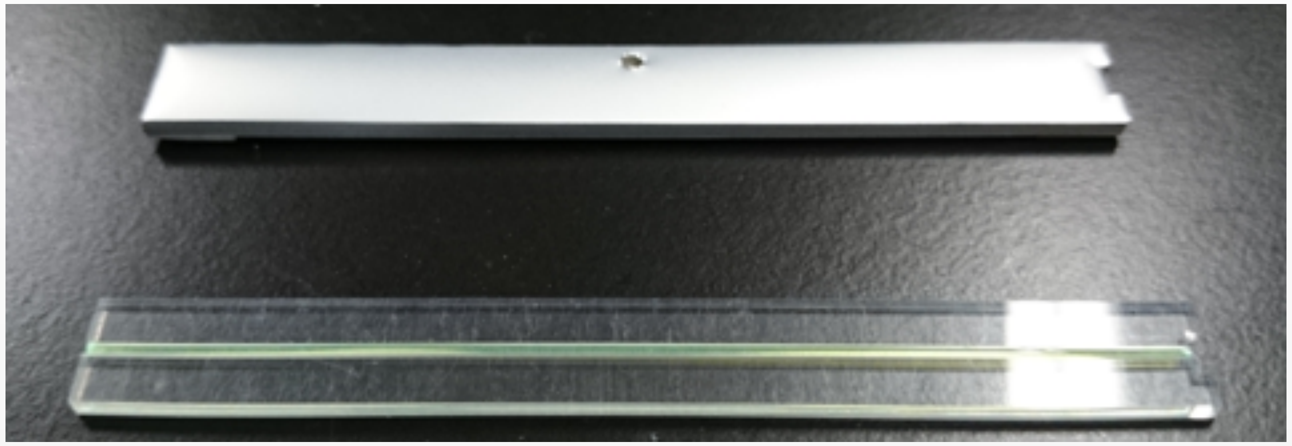
Strip AHCAL

SET UP

MPPC and scintillator

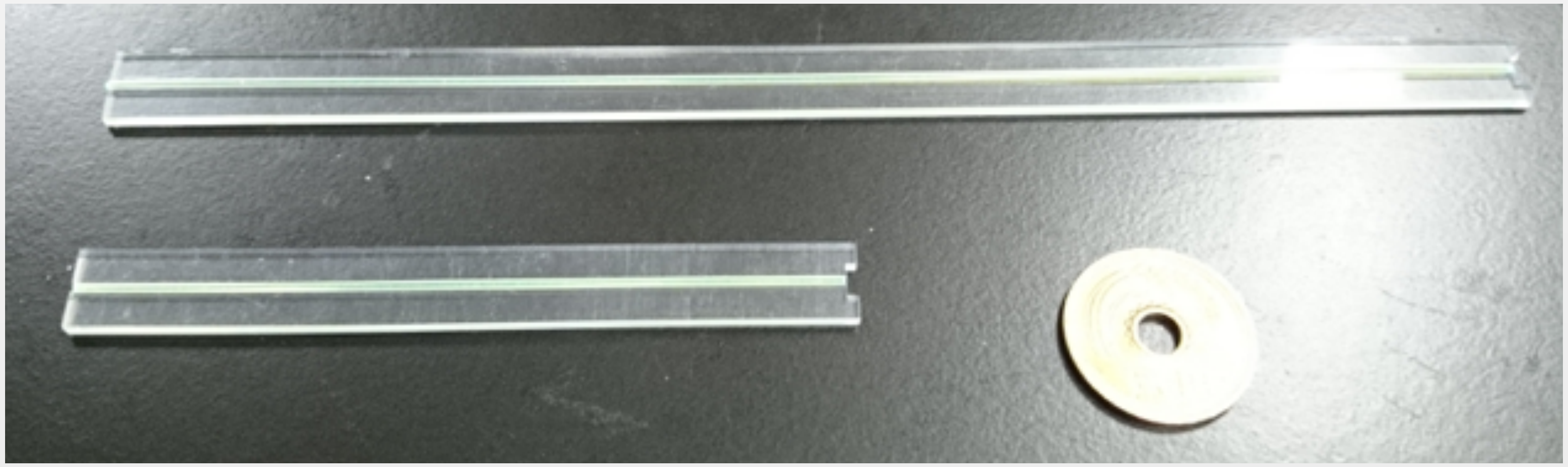


1600pixel MPPC
1cable has 9ch



enveloped in
Kimoto reflector film

length 180mm



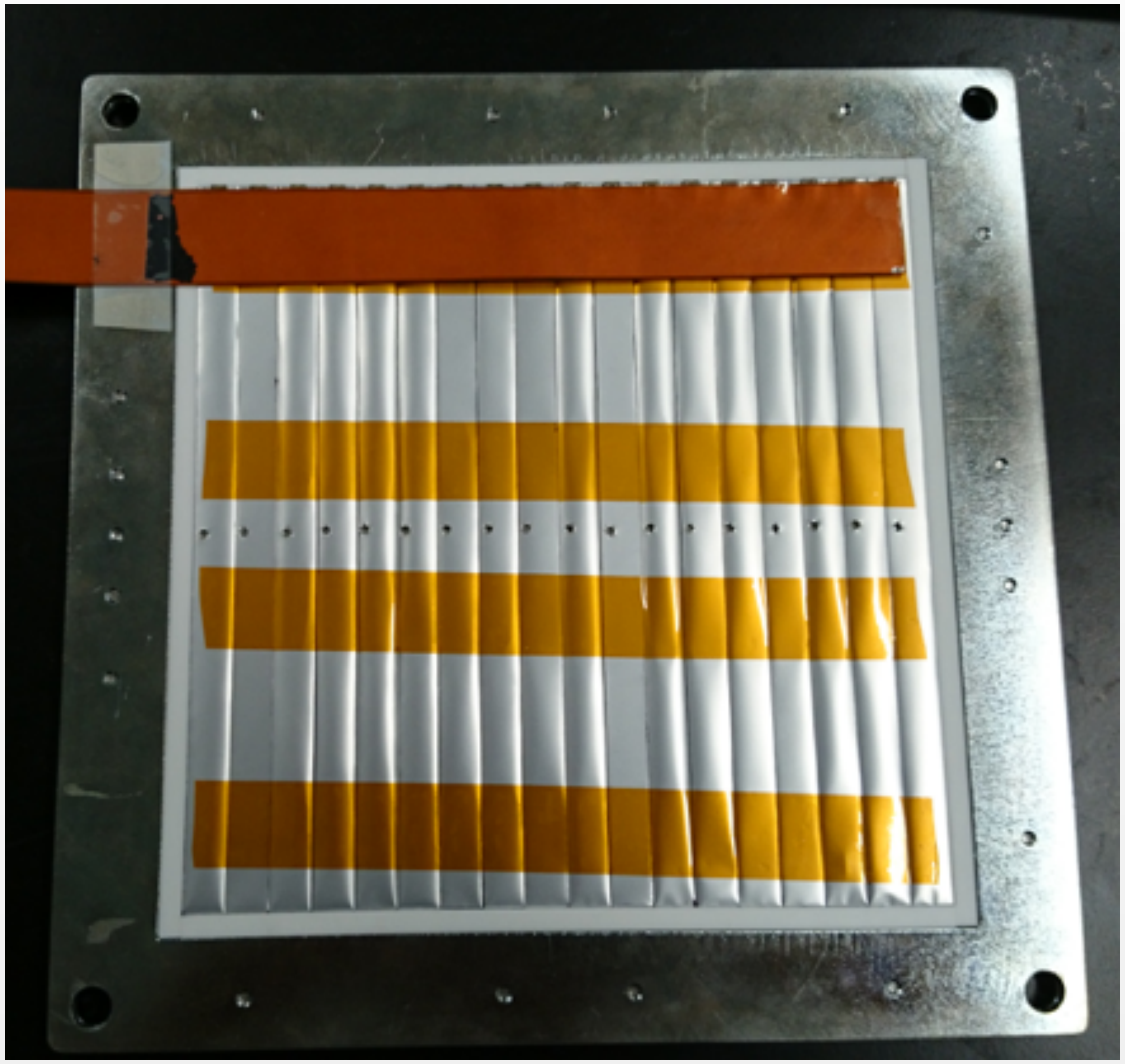
length 90mm

width 10mm
thickness 2mm
with WLSF

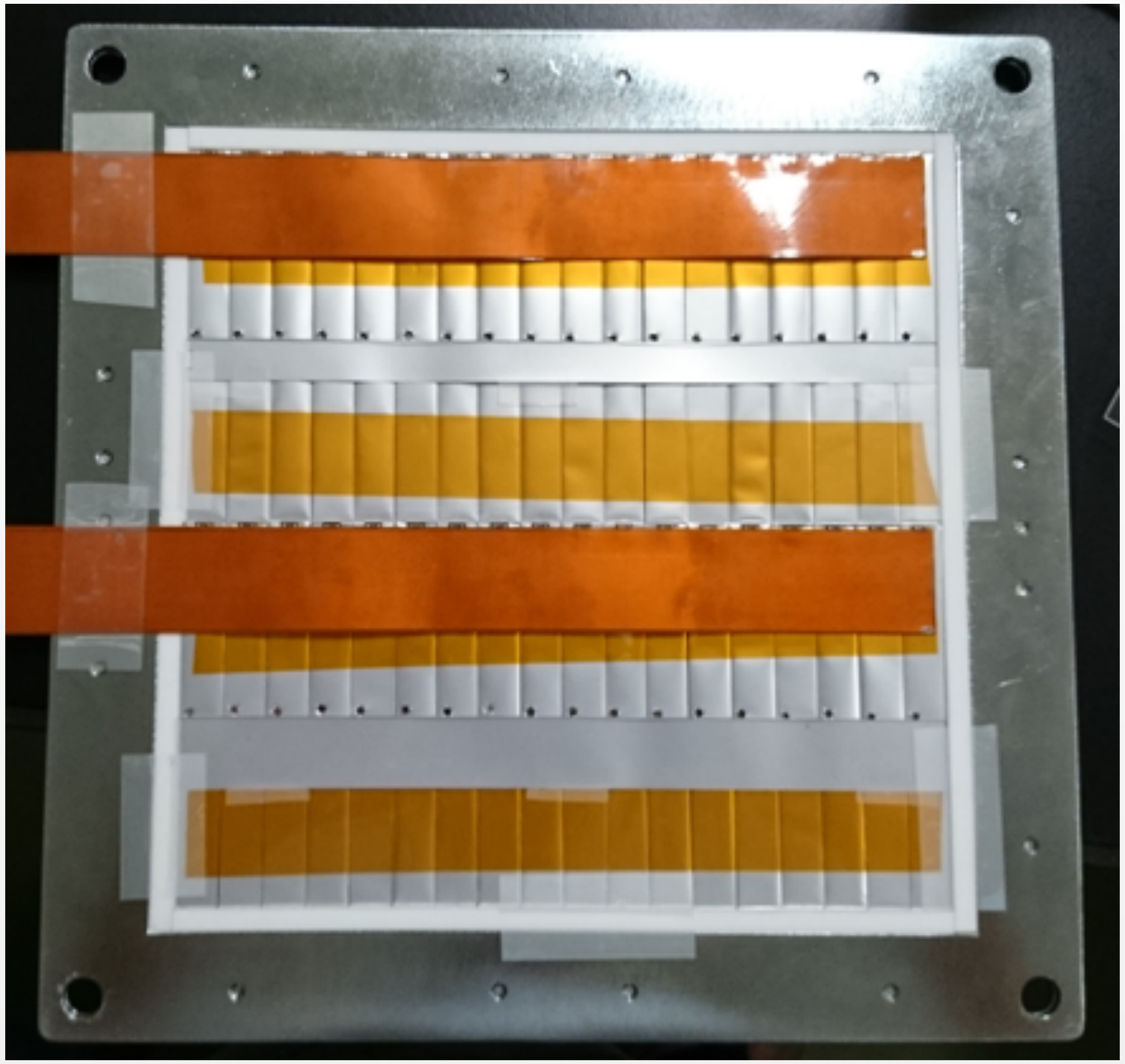
Scintillator Layer

180mm strip layer x2

90mm strip layer x2



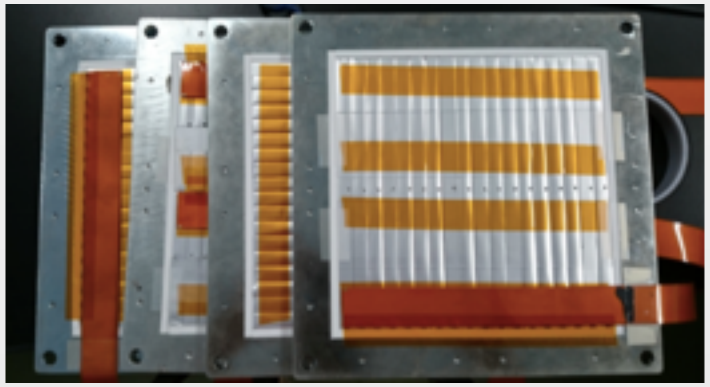
18ch

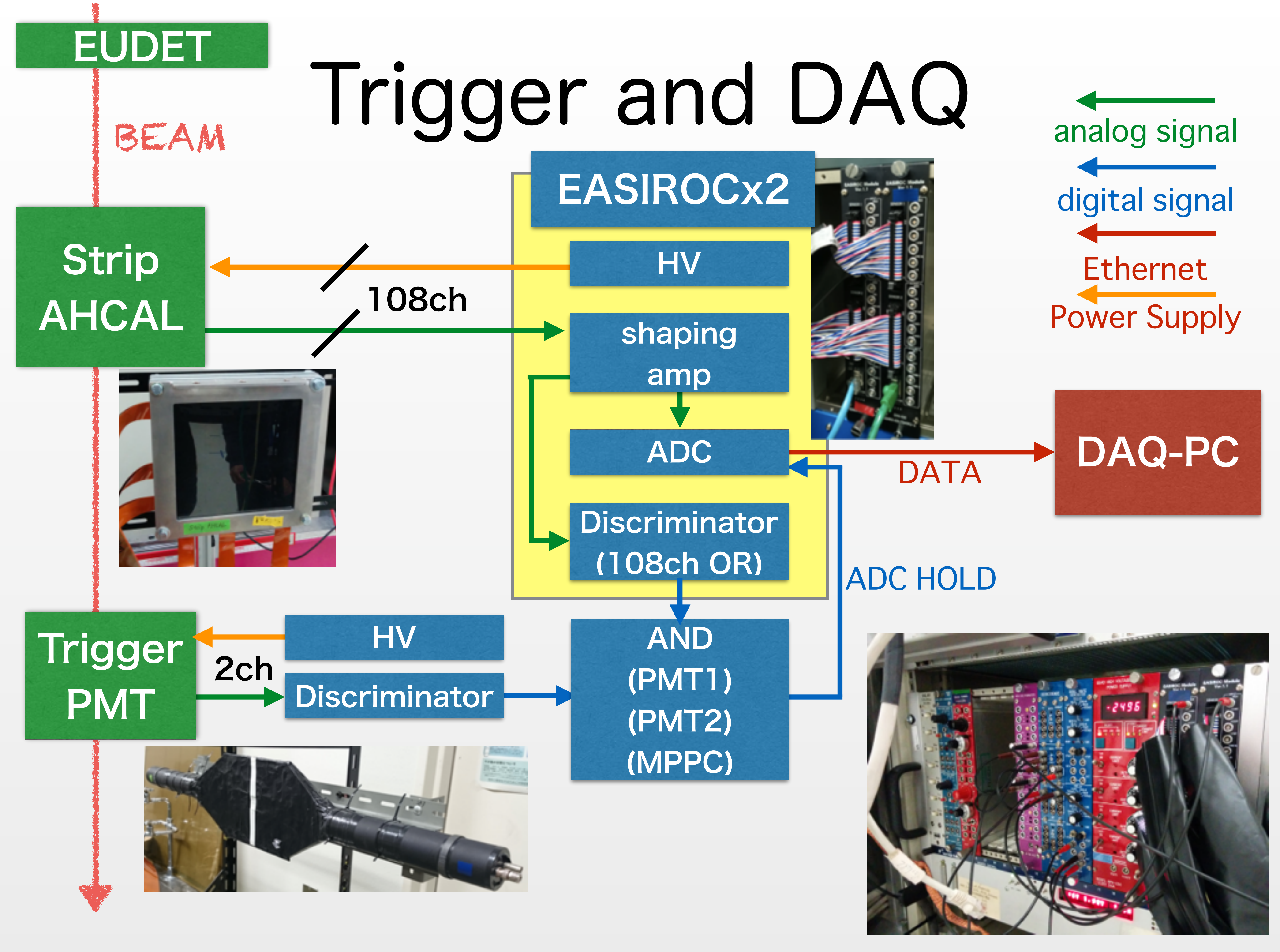


36ch

4layer 108ch

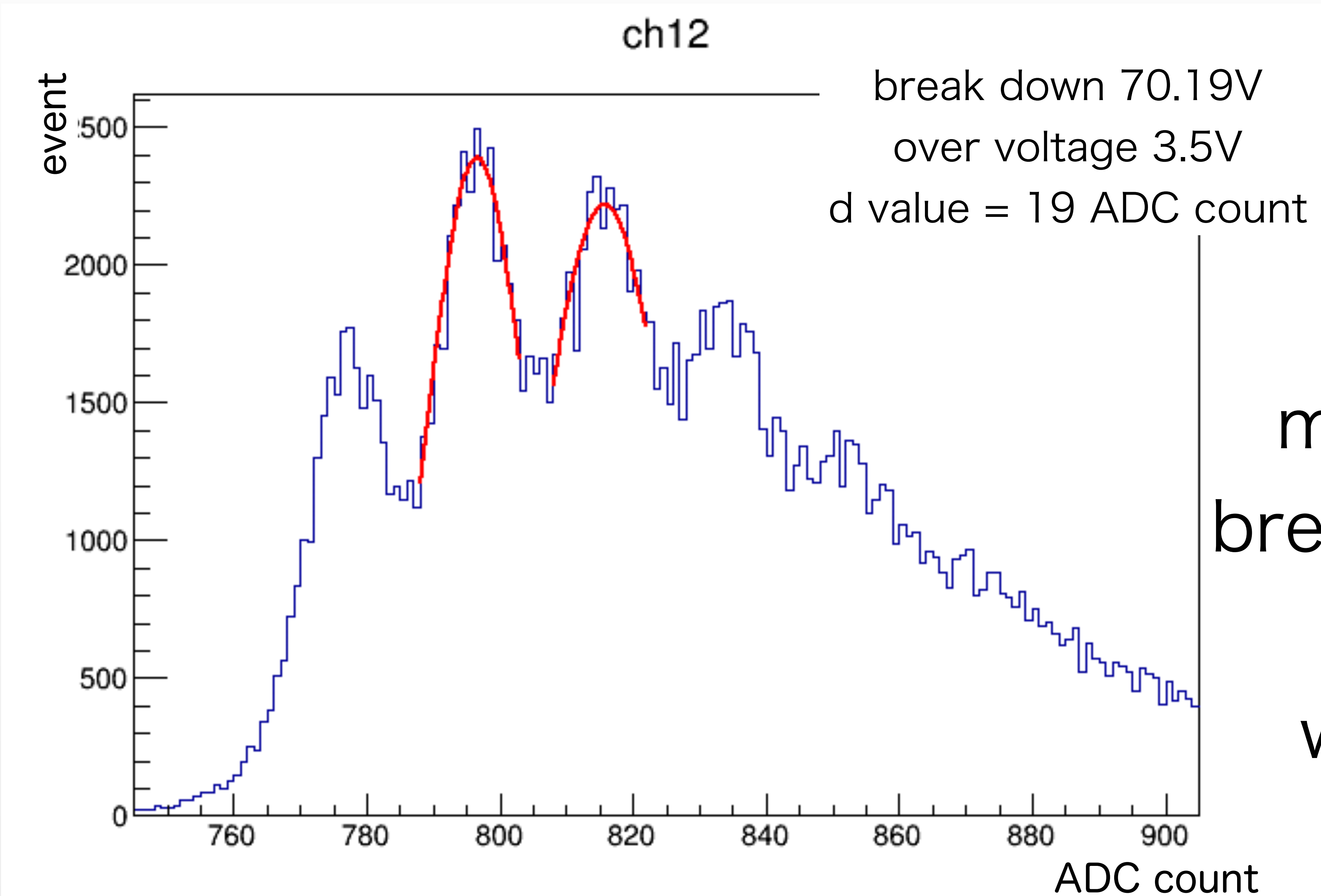
no absorber use in this test beam





Trigger and DAQ
EUDET
BEAM
analog signal
digital signal
Ethernet
Power Supply
EASIROCx2
HV
shaping
amp
ADC
Discriminator
(108ch OR)
Strip
AHCAL
108ch
DAQ-PC
DATA
ADC HOLD
Trigger
PMT
2ch
HV
Discriminator
AND
(PMT1)
(PMT2)
(MPPC)

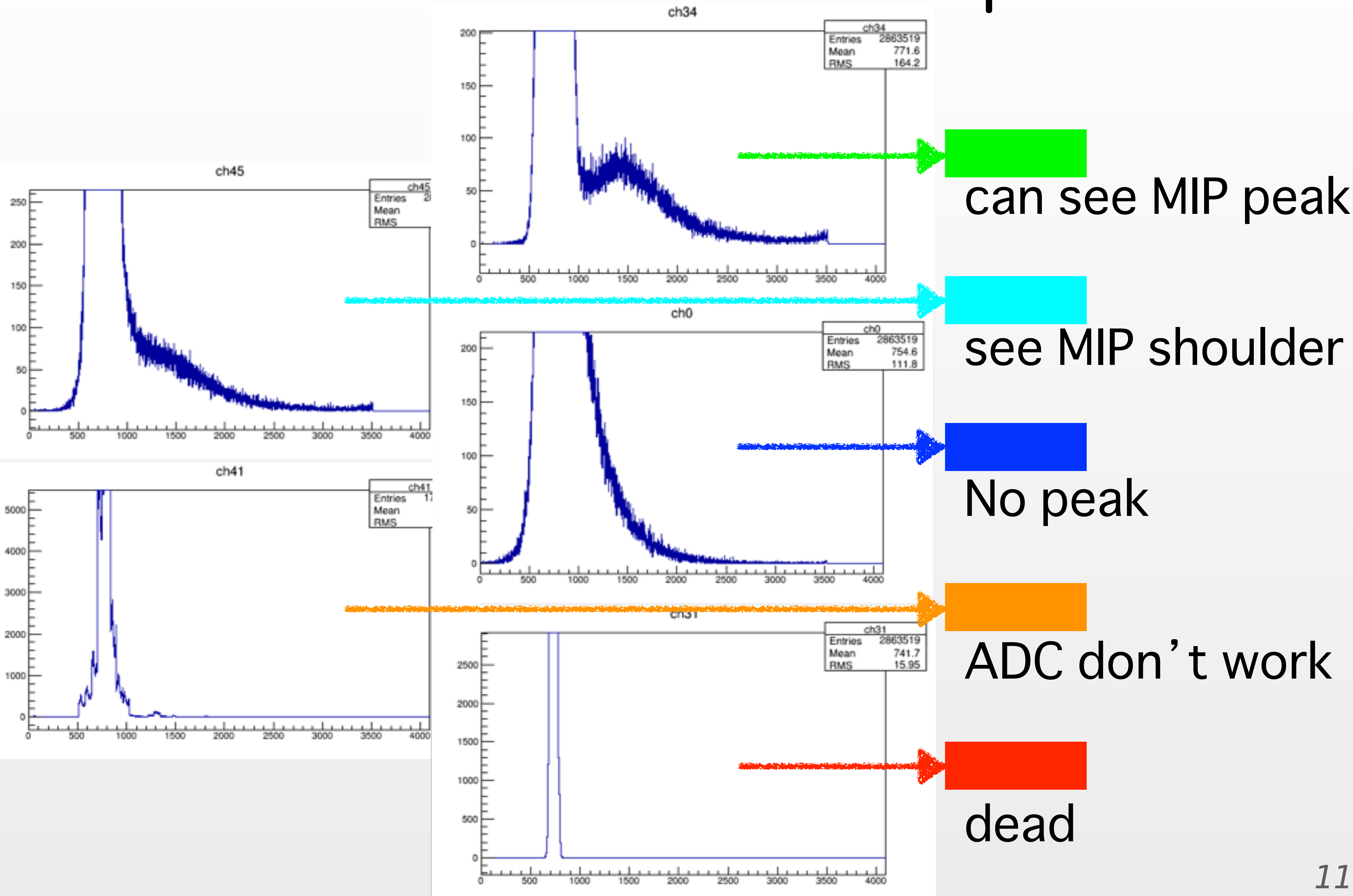
LED calibration at Lab



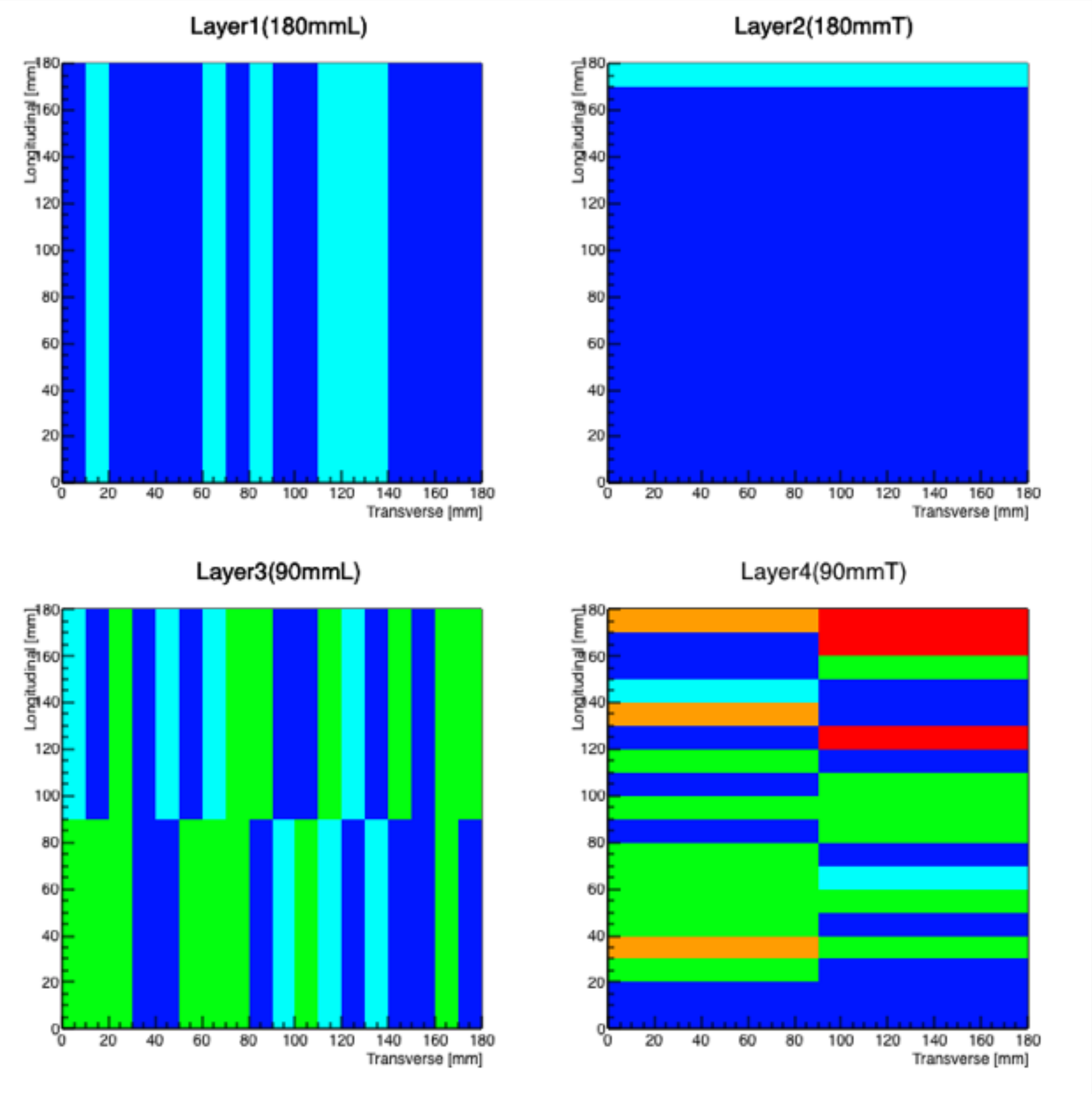
separation 1p.e. , 2p.e.

measure MPPC
breakdown Voltage
and gain
with EASIROC

channel status Map



channel status Map



can see MIP peak

see MIP shoulder

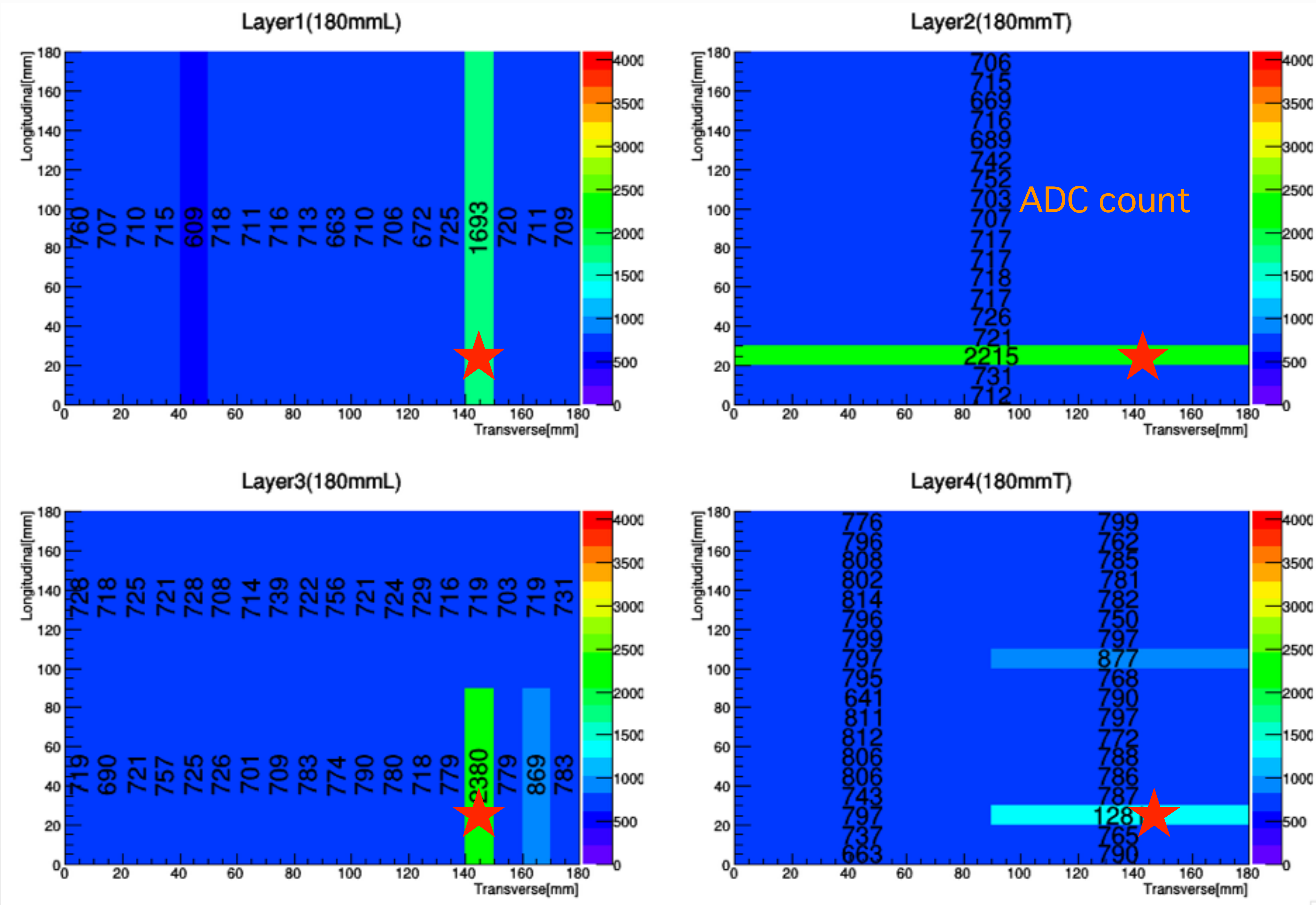
No peak

ADC don't work

dead

MIP event display

★ Hit Position

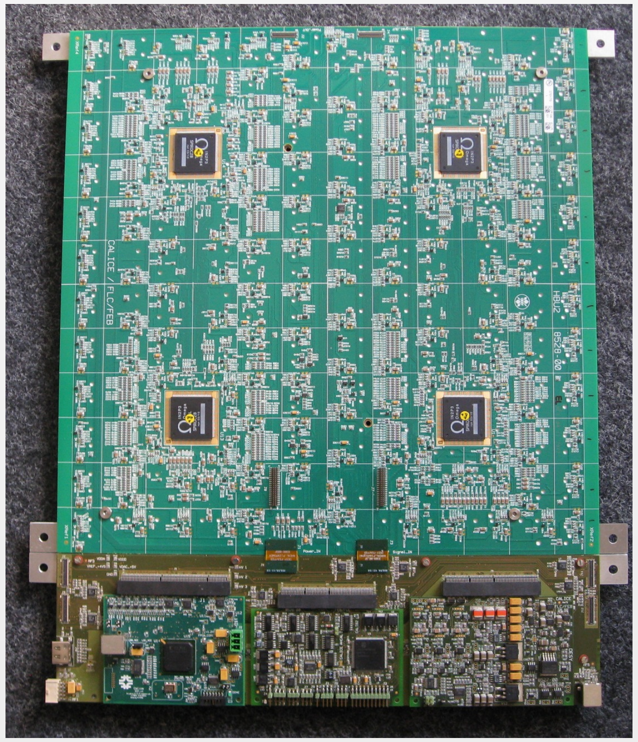


Analysis status

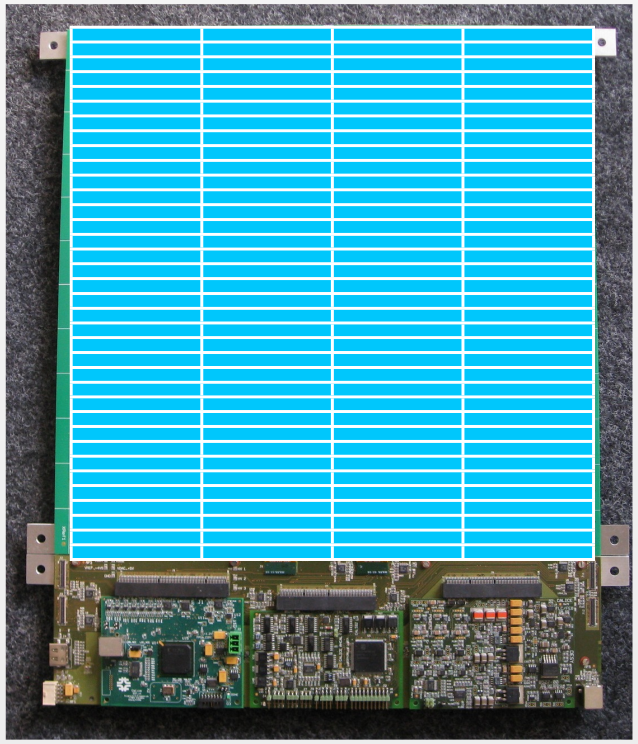
- took 33M events at beam time.
- half of 90mm strips can separate MIP peak.
- all 180mm strips and other 90mm strips cannot separate MIP peak.
- dead channels are 6ch.
- now try temperature correction.
- try MIP analysis of all data, apply SSA, extract det.eff. and response uniformity

Next Test Beam Plan

- SPS test beam (next year)
  - Use HBU (strip Ver.)
  - 2mm Sc -> 3mm Sc (TDR thickness)
  - New MPPC
  - with absorber
  - take muon and pion data



tile HBU



strip HBU

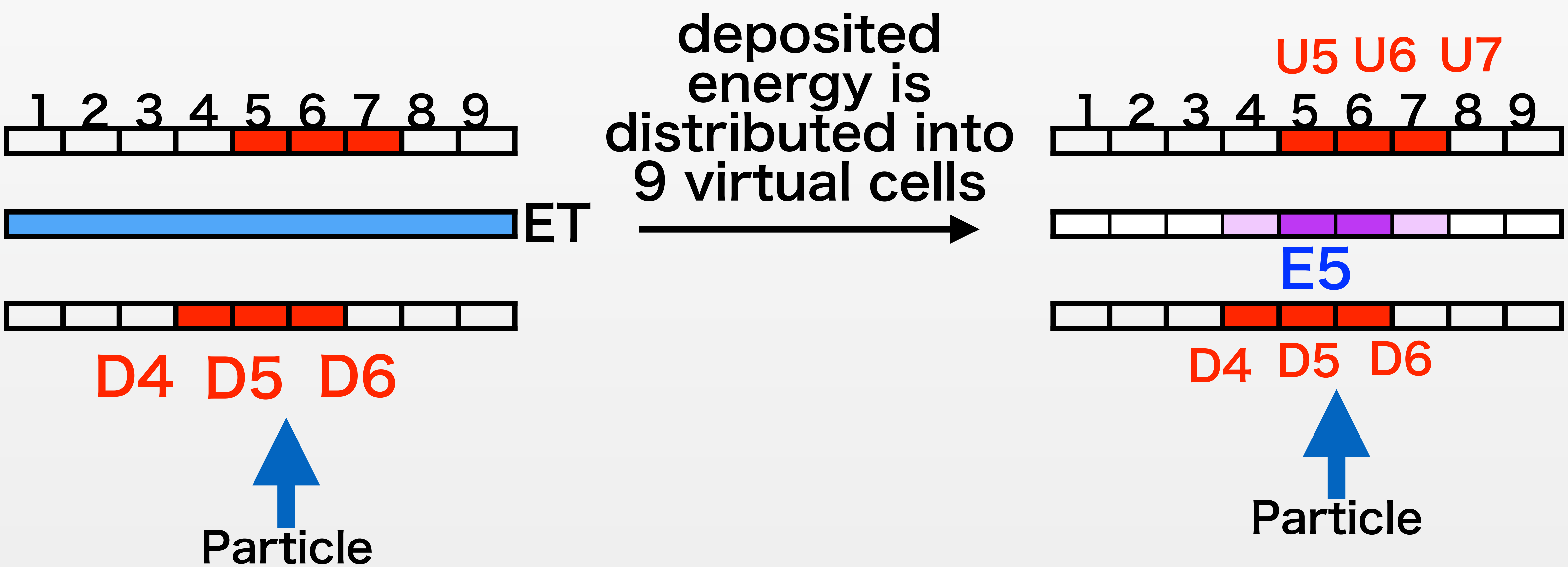
Summery

- We are developing strip AHCAL.
- Strip AHCAL has potential to have good position resolution.
- need to study the simulation more.
- took a lot of data at CERN Test Beam Oct. 2014.
- analysis of test beam data on going.
- plan next test beam at SPS next year

Back Up

Strip Splitting Algorithm(SSA)

- SSA recovers better position resolution to strip direction.

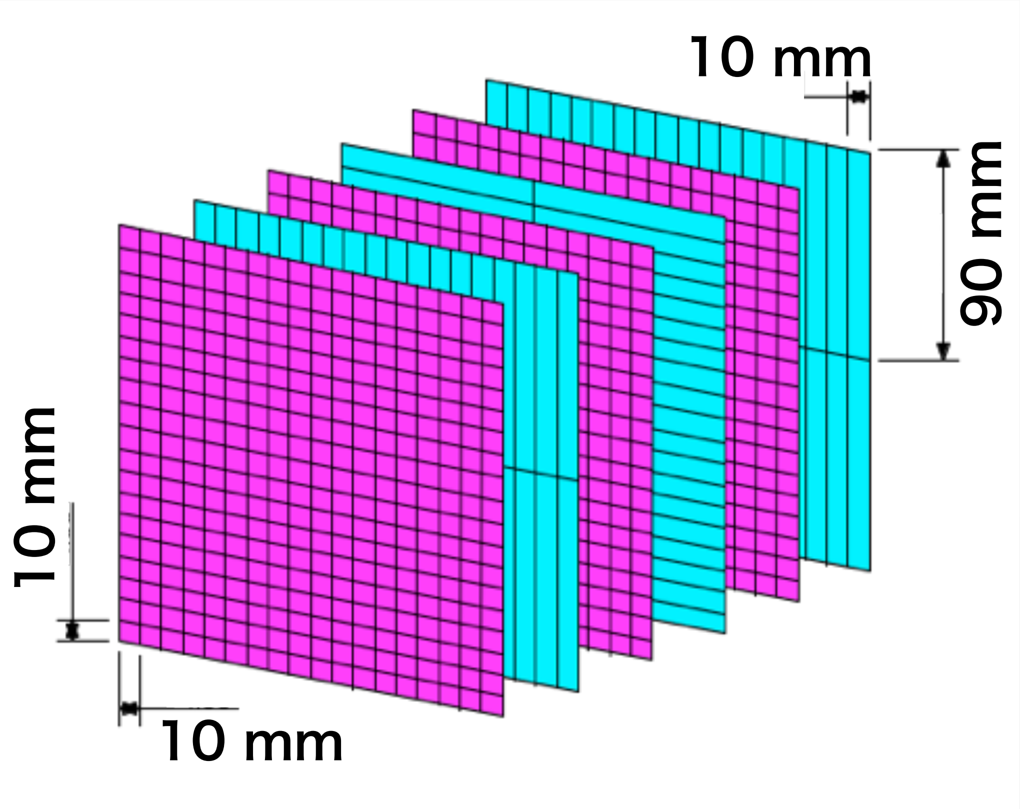


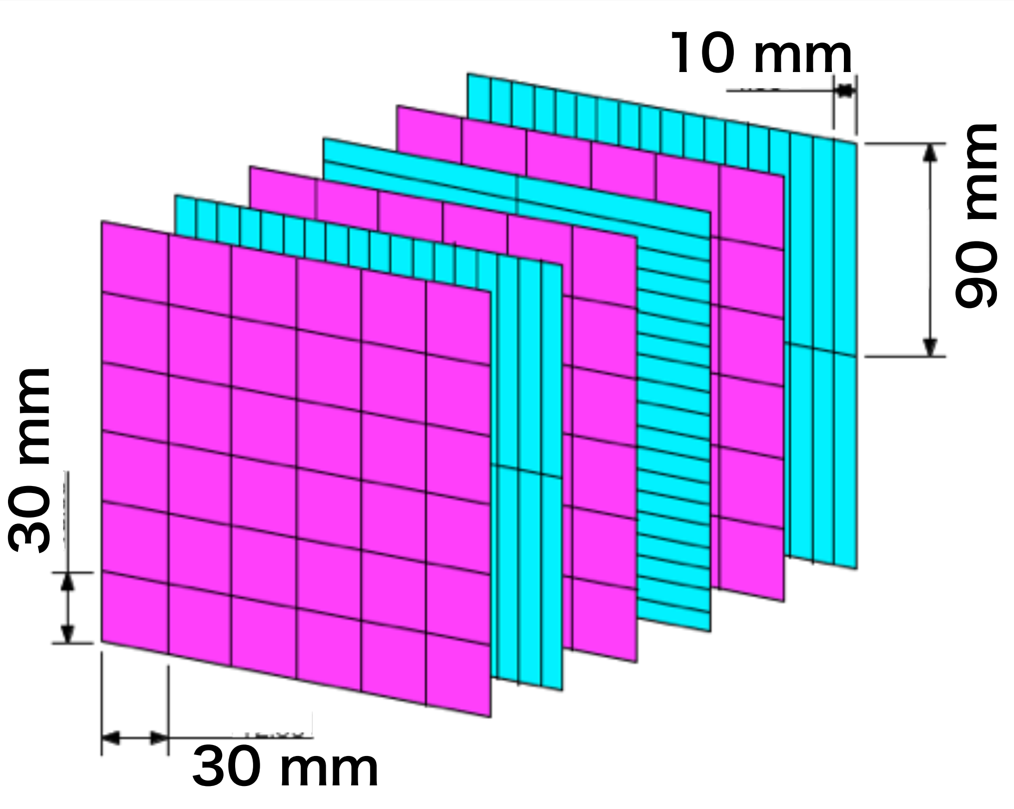
energy distributed in #cell5

$$E5 = ET \times \frac{U5 + D5}{\sum^{9} Uj + \sum^{9} Dj}$$

Alternative option

- Further improvement is expected with tile layers between strip layers.
- We install it to ILD detector model.

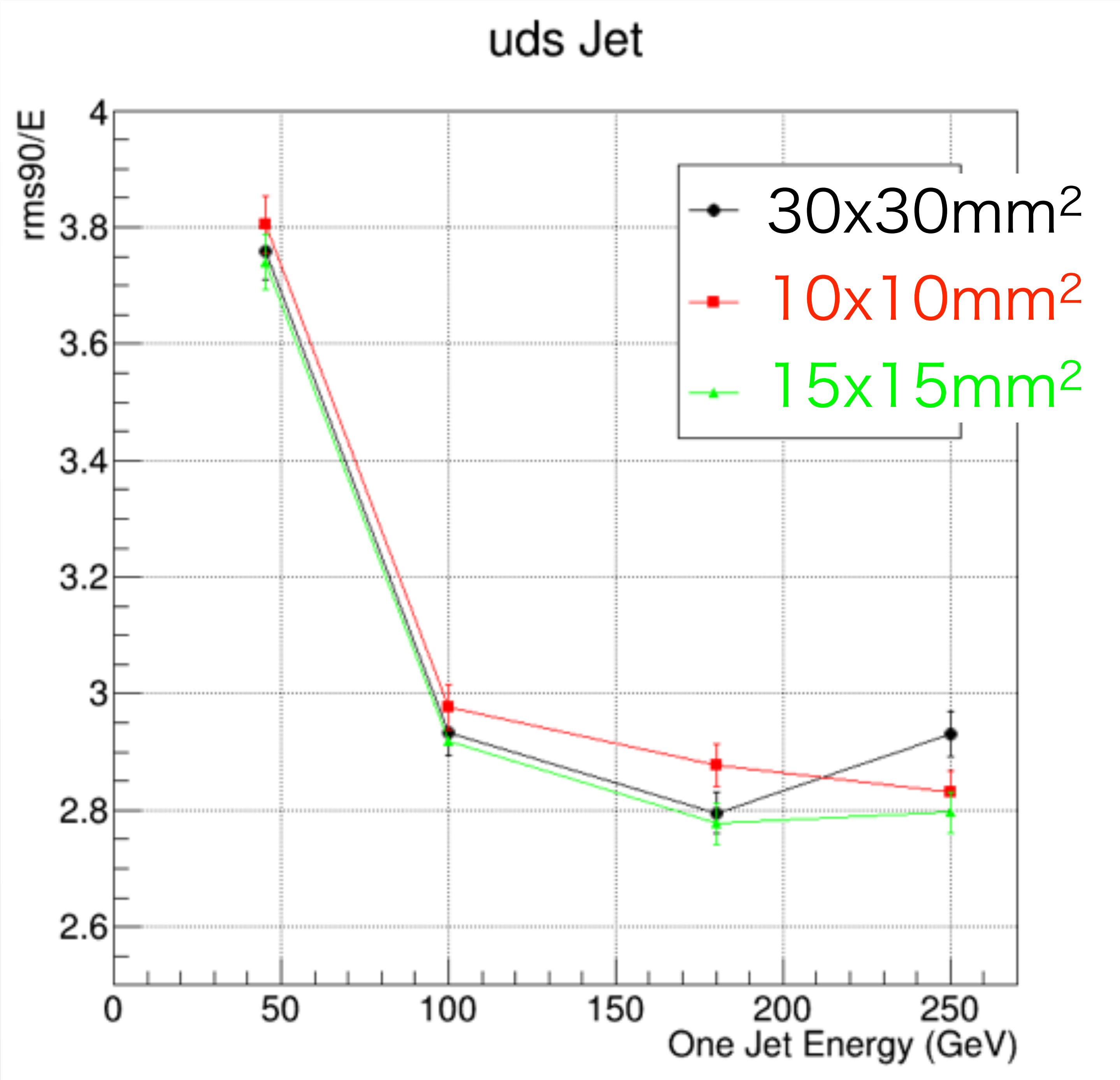




30mm x 30mm

simulation on going

Jet Energy Resolution



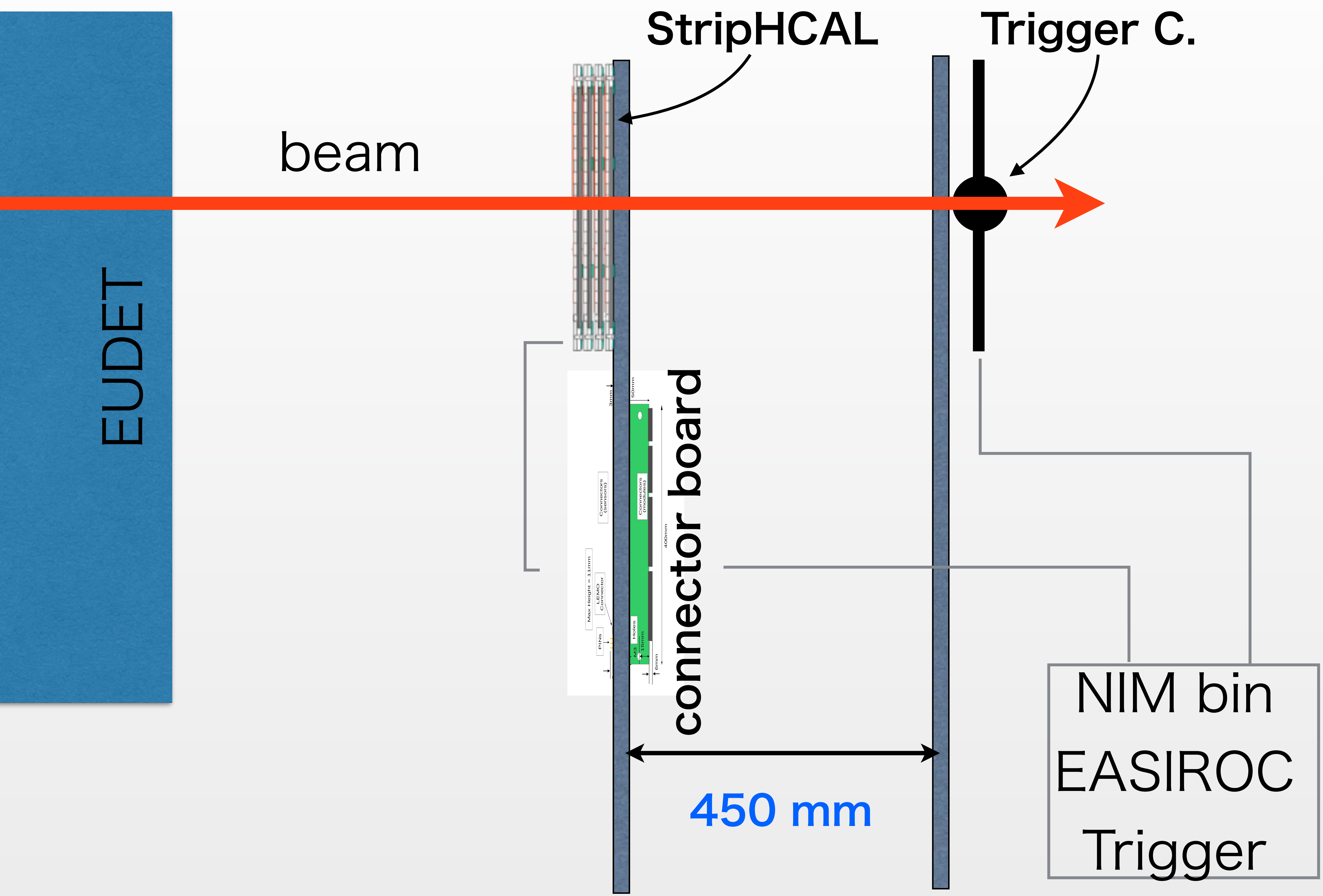
With default
PandoraPFA parameters

10mm x10mm segmentation
results are similar
to 30mm x 30mm tiles.

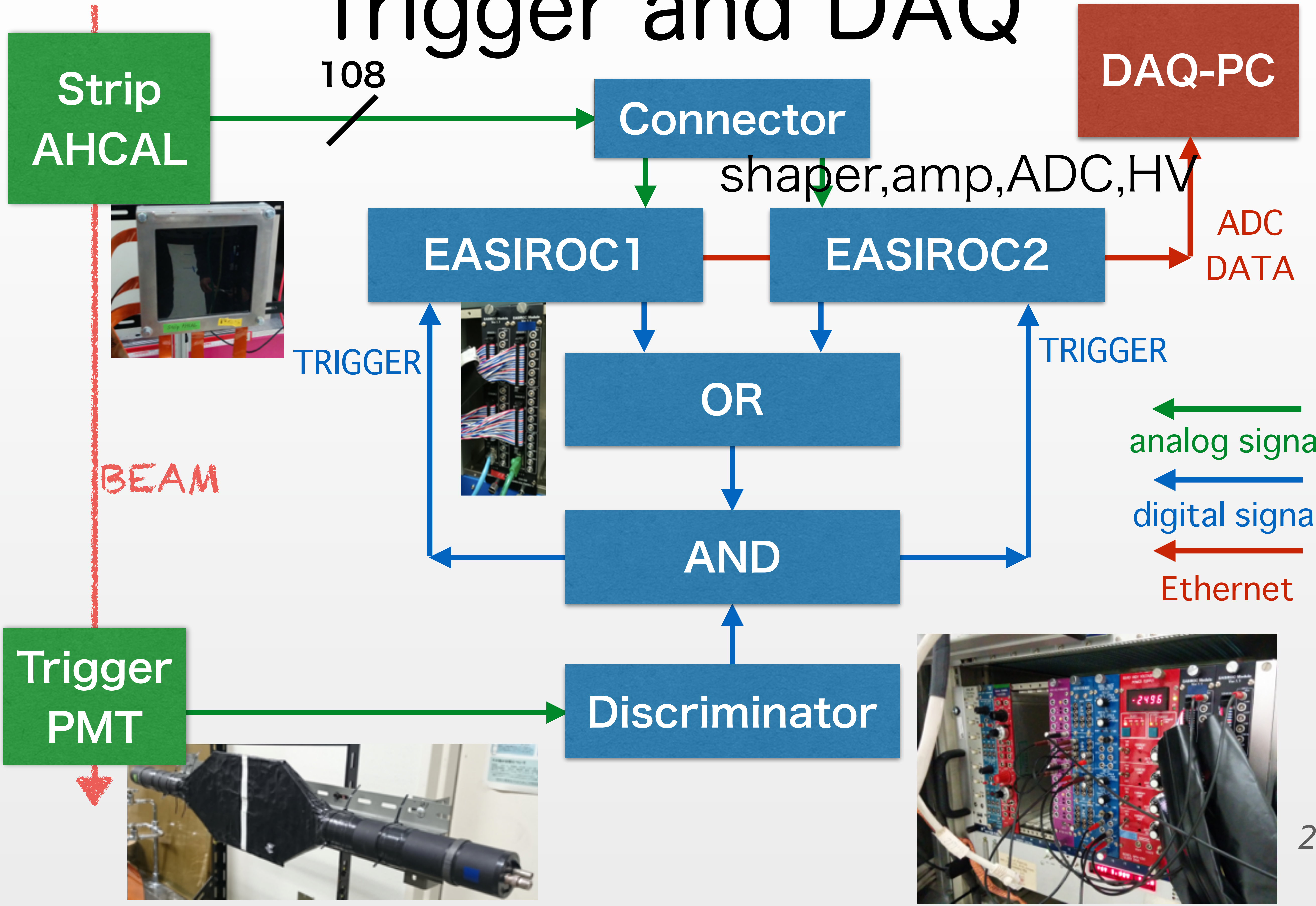
need optimization of
parameters

simulation is on going

setup


StripHCAL
Trigger C.
beam
EUDET
connector board
450 mm
NIM bin
EASIROC
Trigger

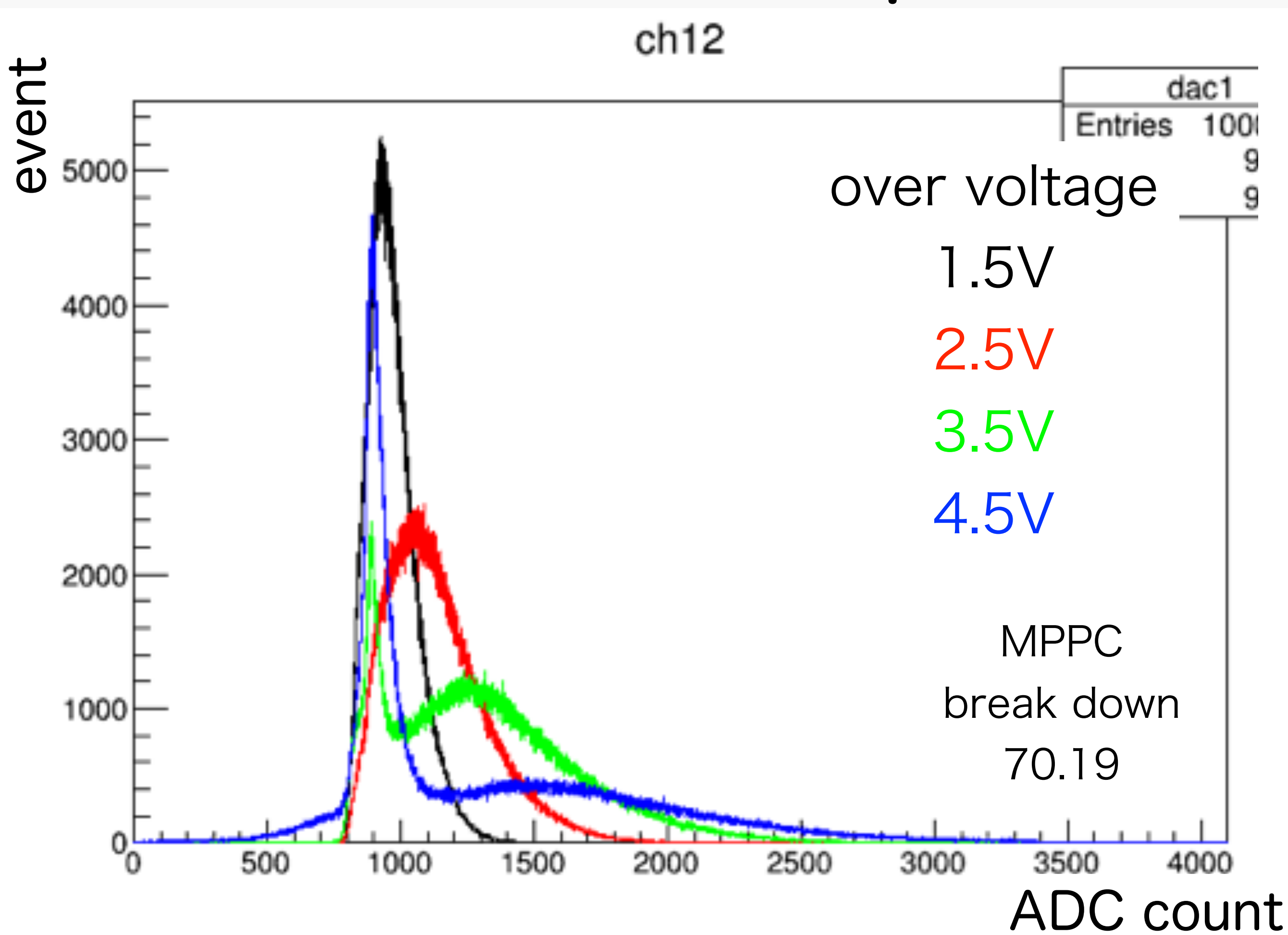
Trigger and DAQ



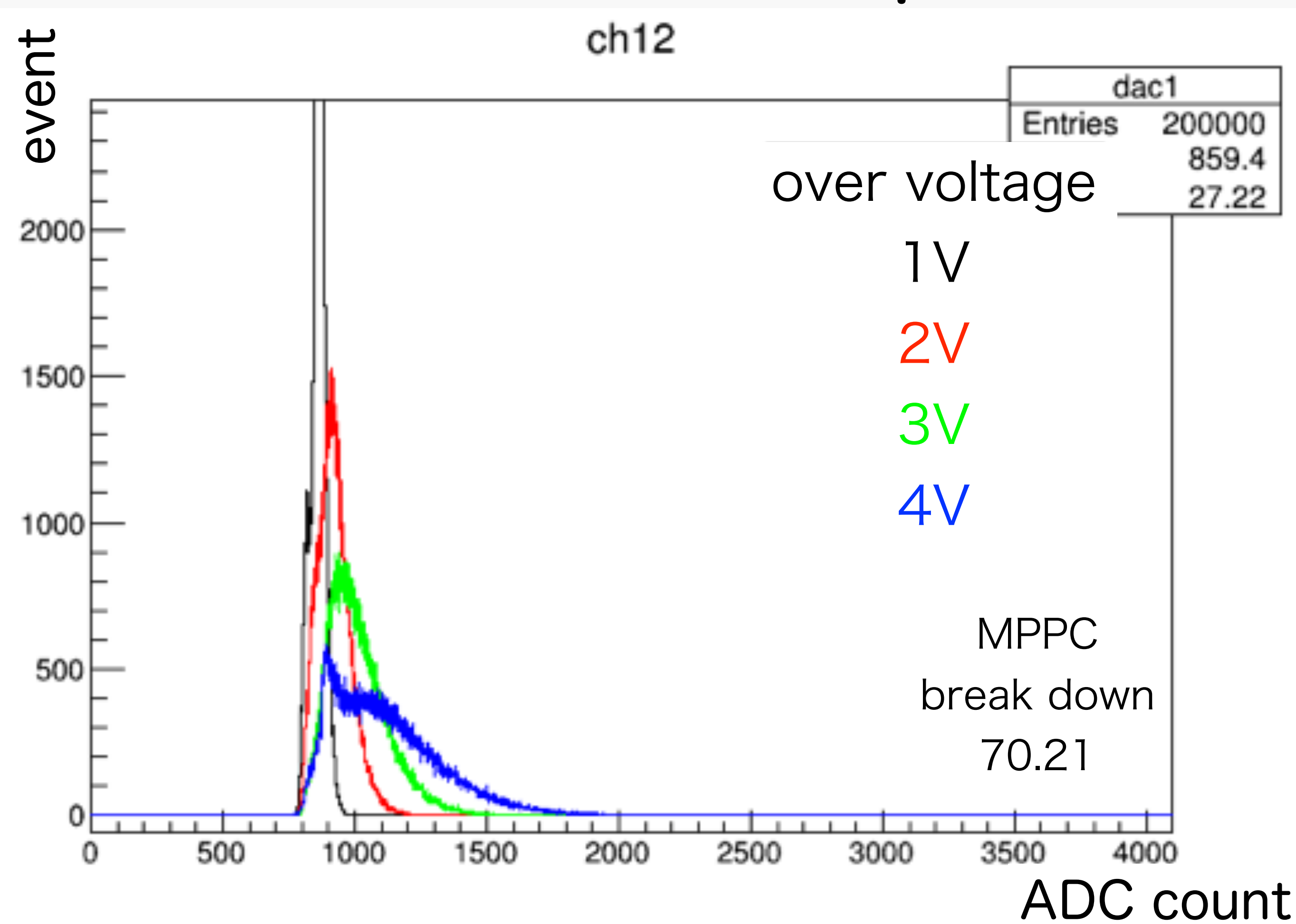
^{90}Sr test

put ^{90}Sr at center of strip with EASIROC

90mm strip



180mm strip



MIP peak = 18p.e.

MIP peak = 8p.e.

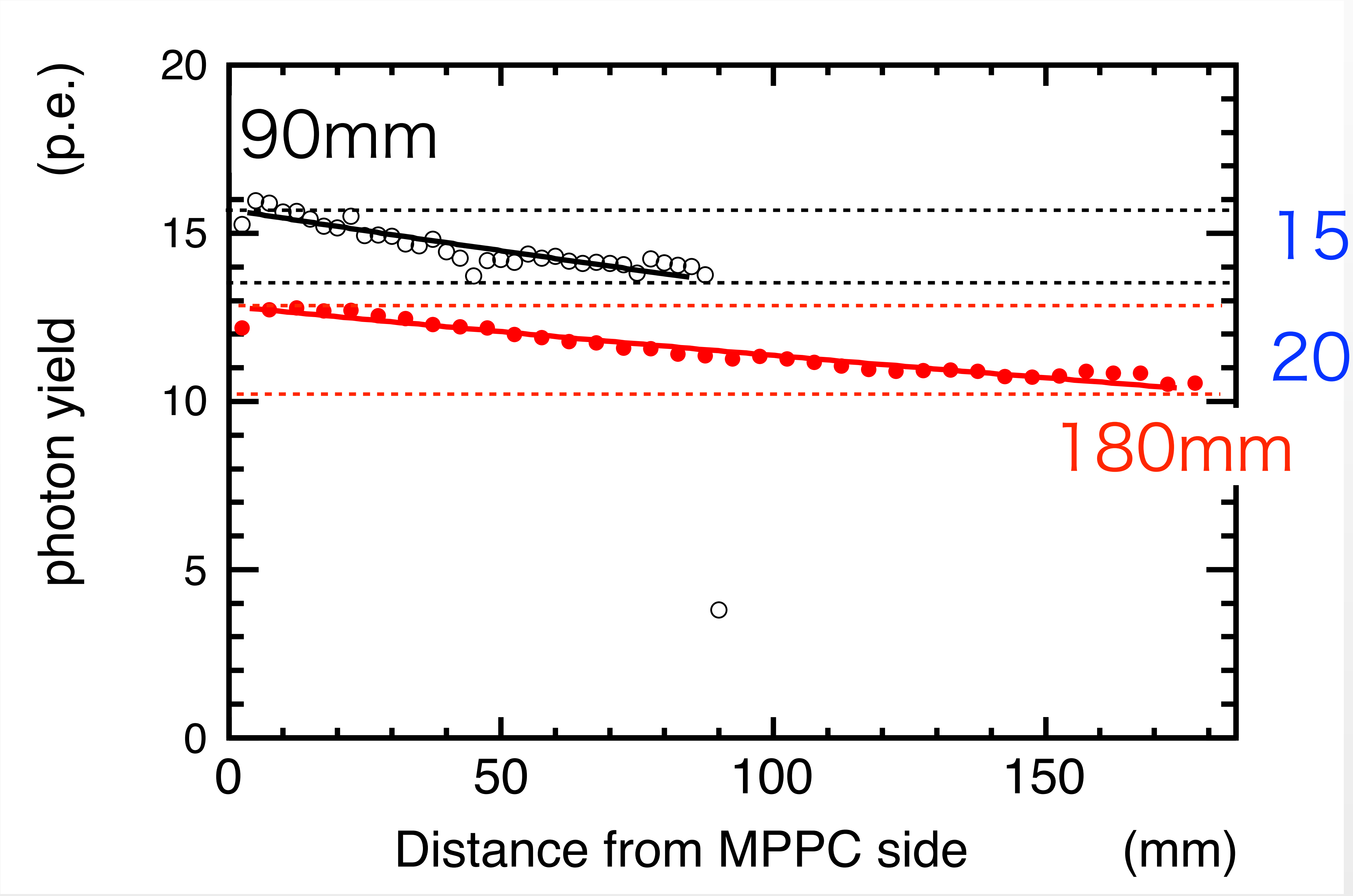
decide operation voltage set 90mm 3.5V 180mm 4V

events

date	event	
1010	5,852,760	
1011	4,491,974	
1012	4,491,974	
1013	3,694,628	
1014	3,072,119	
1015	3,466,431	
1016	1,908,871	
1017		blackout
1018	1,656,375	
1019	2,838,432	
1020	1,807,382	
1021	5,010,846	
sum	33,799,818	

Uniformity of response

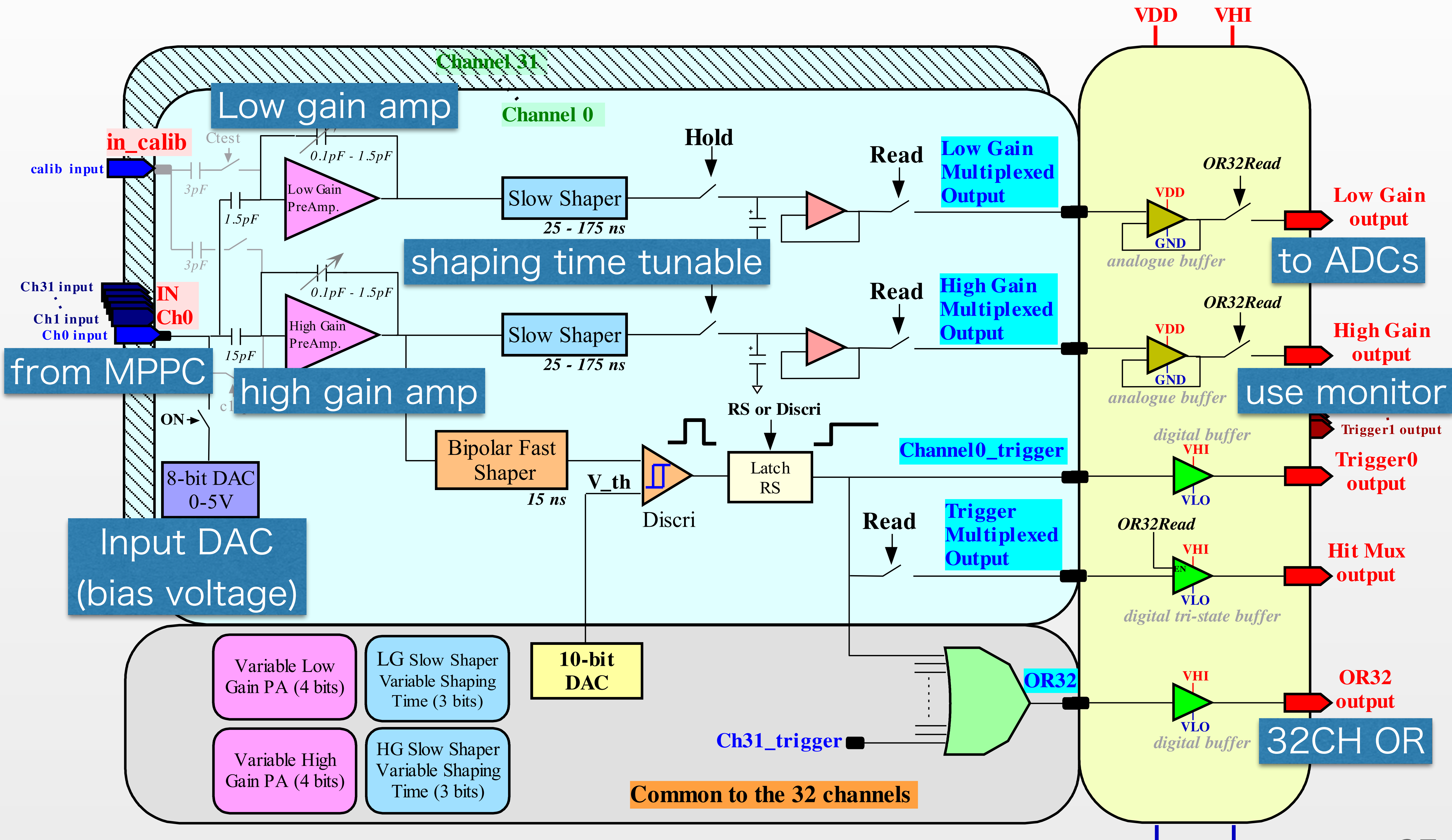
with camas ADC
by Tsuzuki



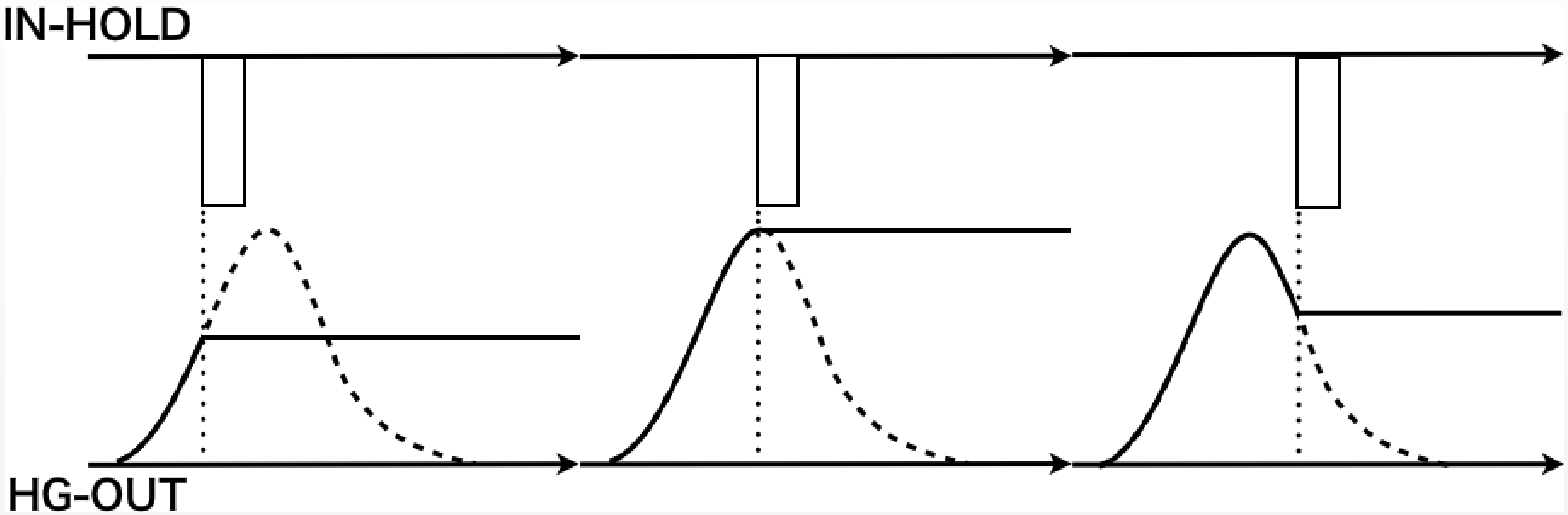
EASIROC-NIM MODULE

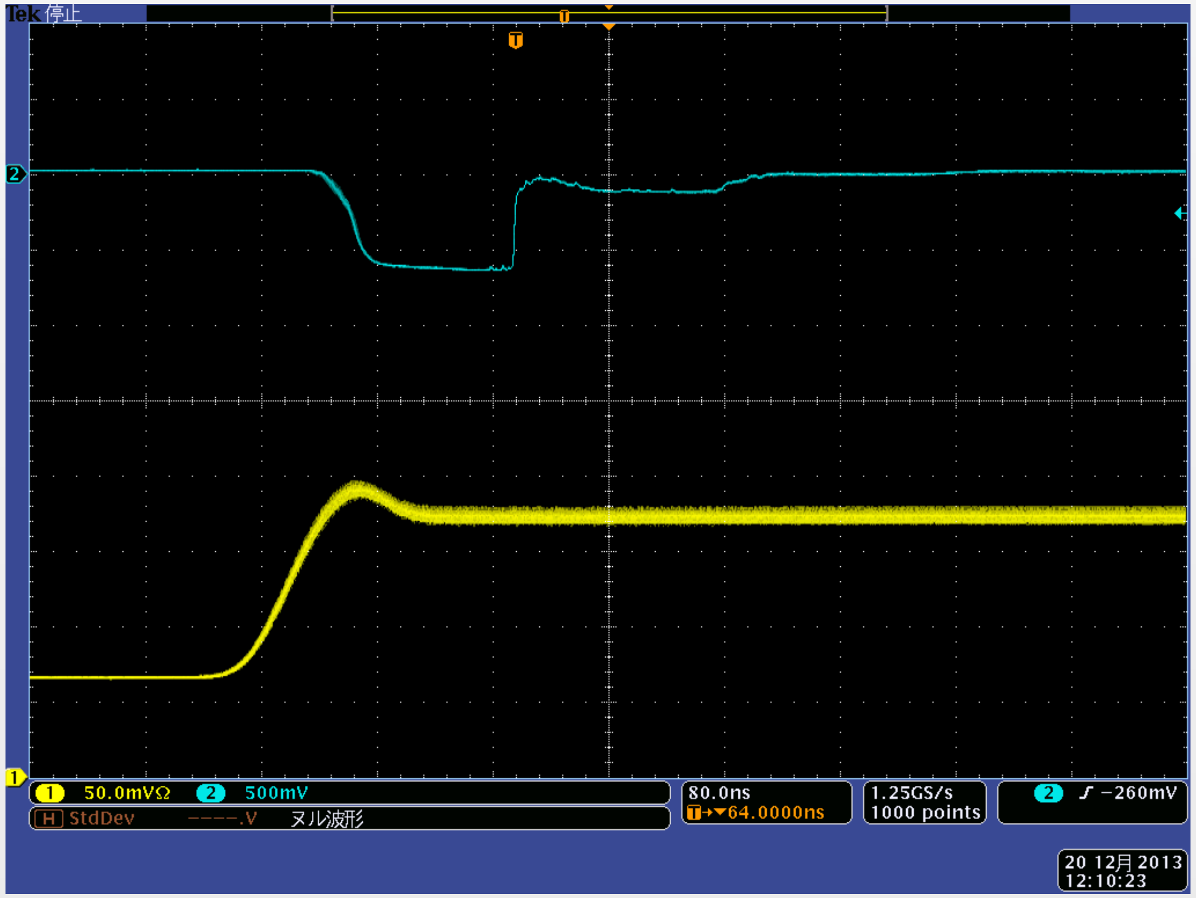
- for MPPC
- developed by KEK and OSAKA University
- EASIROC Chip x2
- 64 ch / module
- + ADC, HV power supply
- settable Individual bias voltage,gain,shaping time
- controlled by PC via Ethernet
- power needs 6V (NIM or AC adapter)

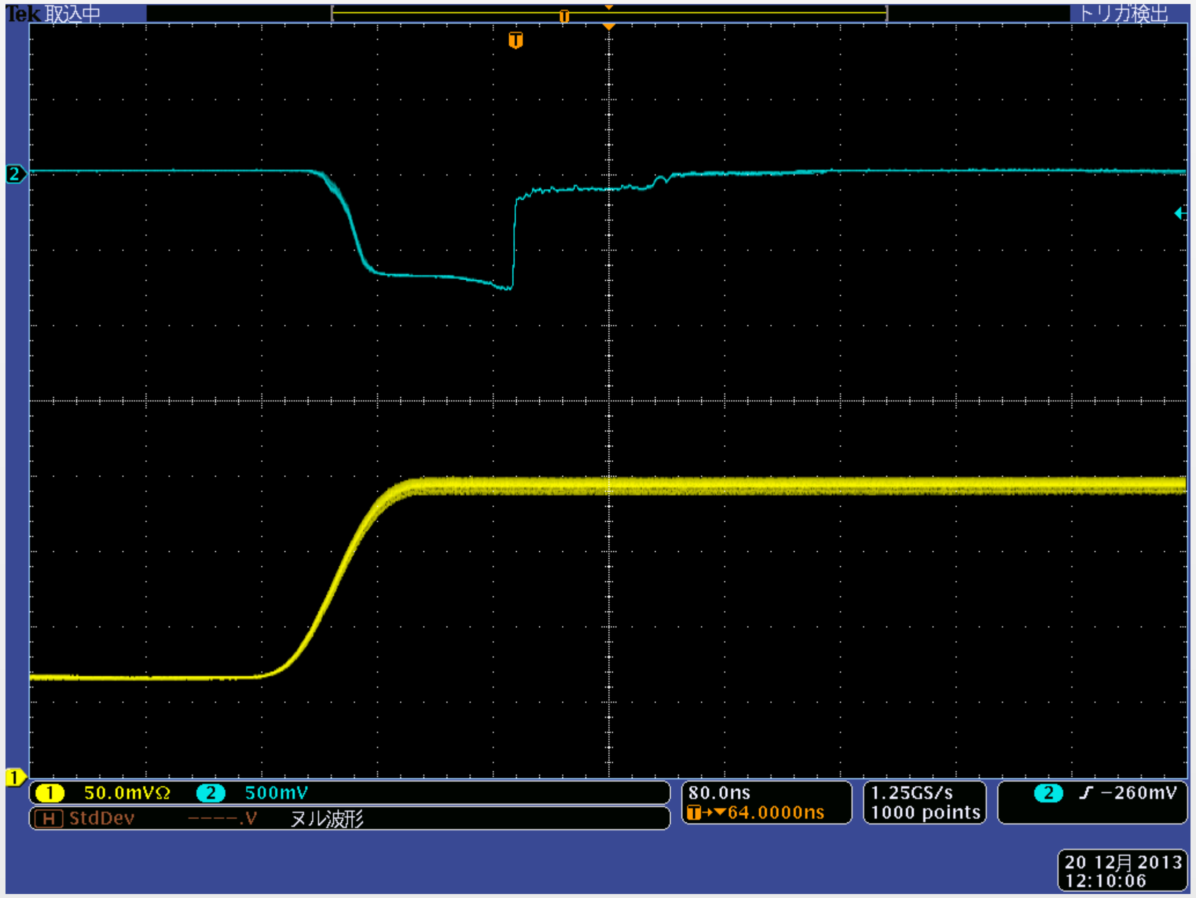
EASIROC chip



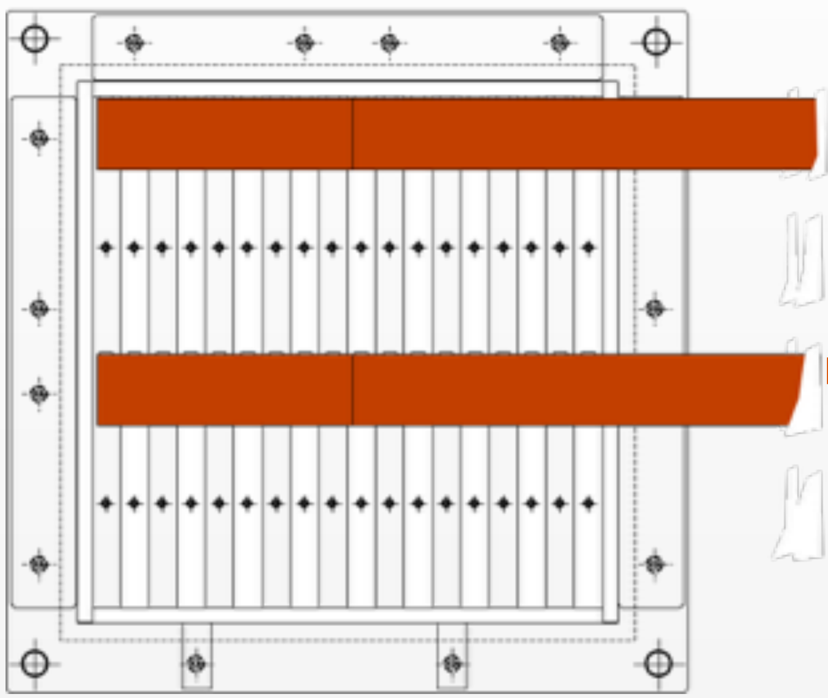
peak hold


IN-HOLD
HG-OUT


Tek 停止
50.0mVΩ
500mV
StdDev
ヌル波形
80.0ns
64.0000ns
1.25GS/s
1000 points
−260mV
20 12月 2013
12:10:23


Tek 取込中
トリガ検出
50.0mVΩ
500mV
StdDev
ヌル波形
80.0ns
64.0000ns
1.25GS/s
1000 points
−260mV
20 12月 2013
12:10:06

DAQ



108 channels

12 cables

64 channels x 2
Easiroc-NIM module

Trigger and DAQ

EASIROC OR of 64ch

EASIROC OR of 64ch

PMT

PMT

OR (108ch)

Discriminator

coincidence

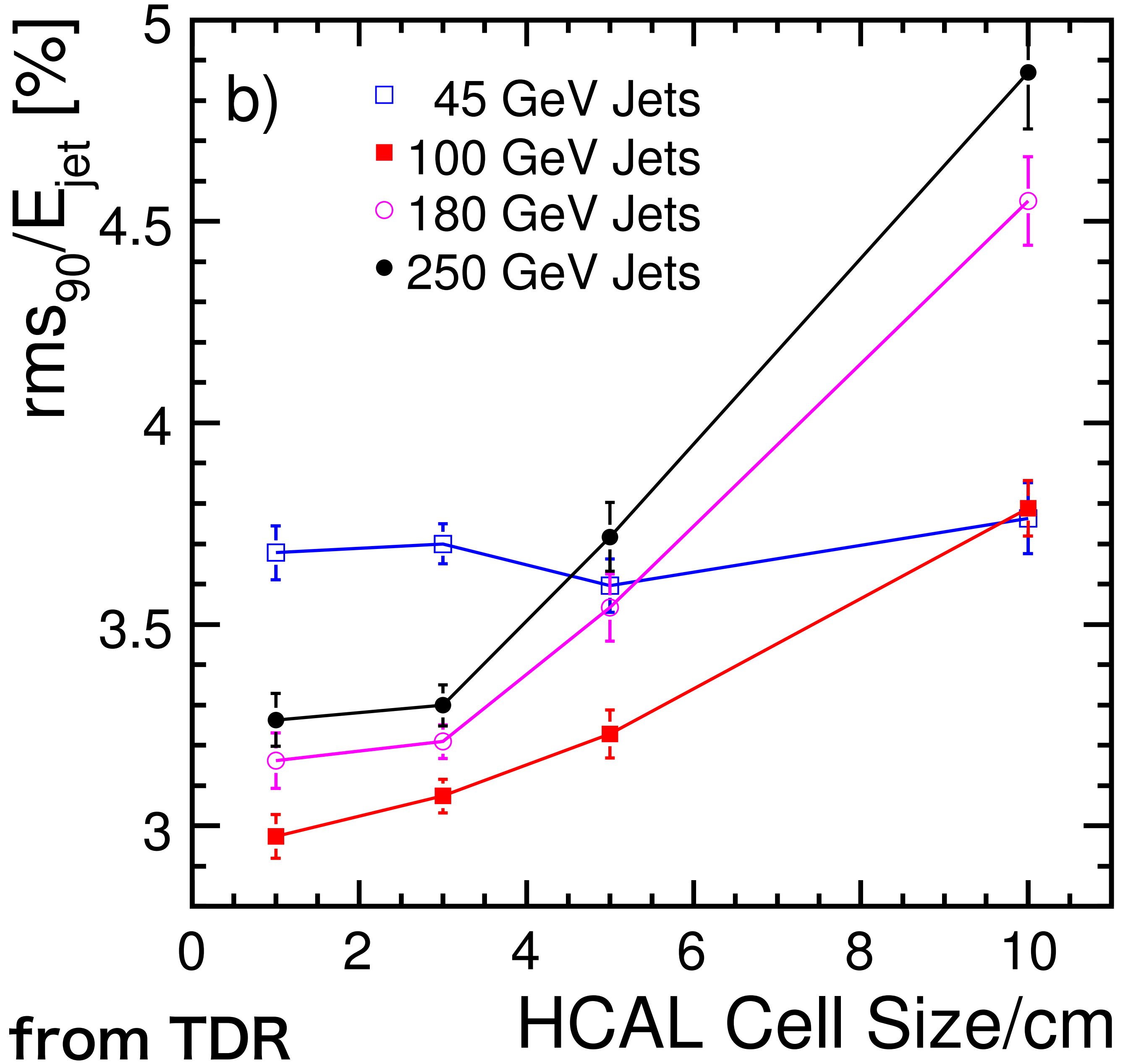
GATE

EASIROC HOLD

SiTCP

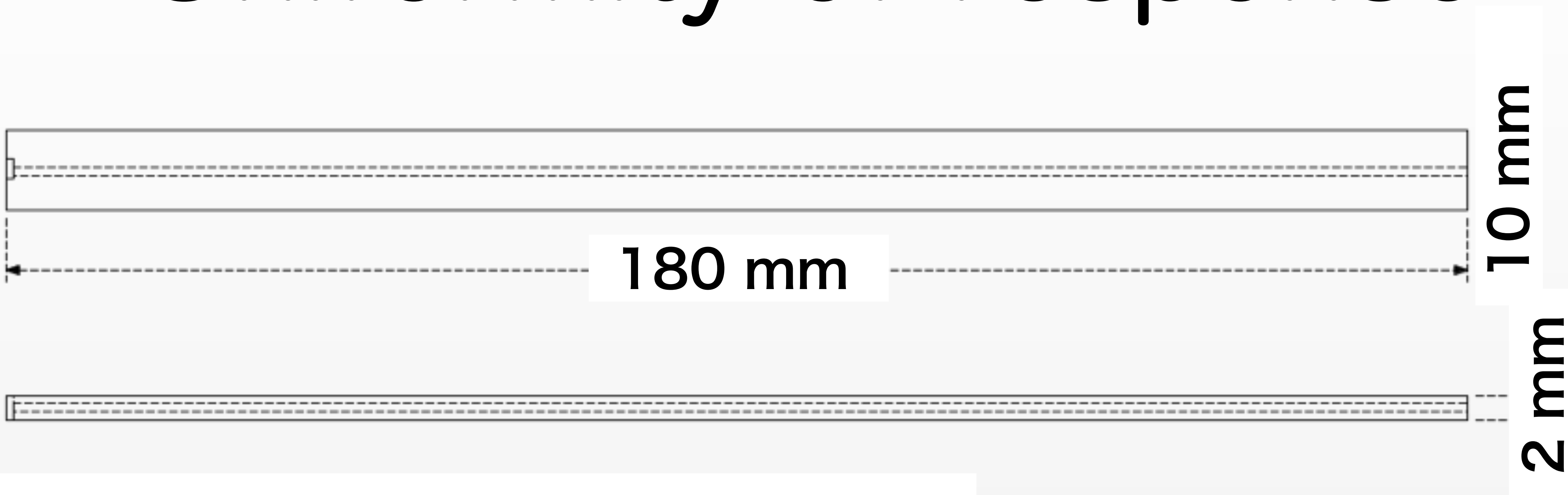
PC

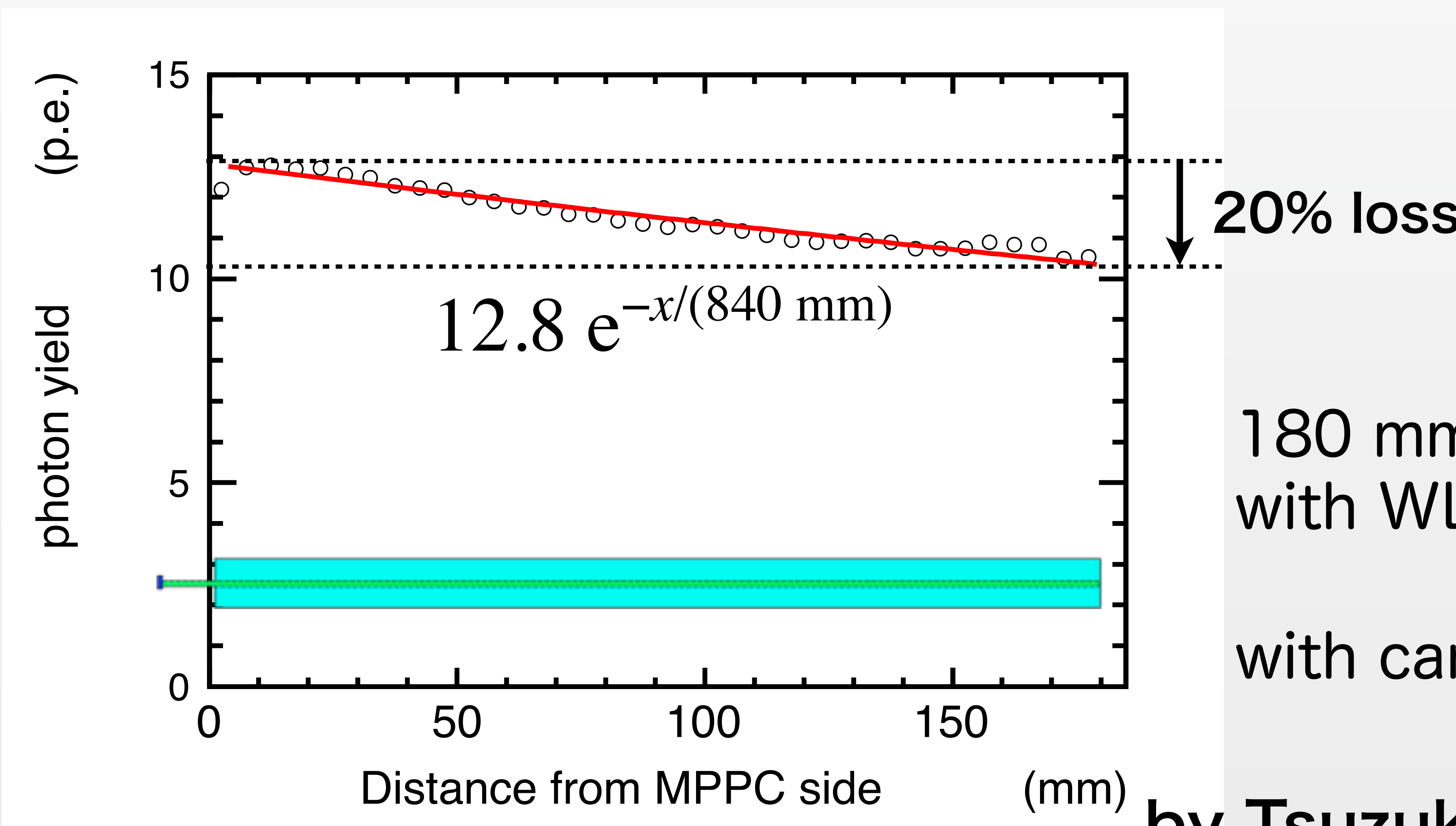
cell size vs Jet Energy Resolution



from TDR

Uniformity of response





180 mm ×10 mm × 2 mm Sc
with WLSF

with camac ADC

by Tsuzuki

^{90}Sr test

put ^{90}Sr at center of strip with EASIROC