Minutes of electronics expert meeting 18.9.2014 Bonn

Attendance:
Bonn: Paul Colas (Saclay), Fabrice Guilloux (Saclay), Jochen Kaminski (U. Bonn). Hans Krüger (U. Bonn)
Fuzebox: Takahiro Fusayasu (U. Saga), Leif Jonsson (U. Lund), Takeshi Matsuda (KEK), Ron Settles (MPI Munich)

1.) Welcome and introduction:
Short welcome by Jochen. Everyone introduced himself giving information on his area of expertise.

2.) Signal formation:
Jochen made a short summary of the typical signal sizes expected in a TPC. He explained the leading effects and the potential implications for the electronics. In particular a signal size of 60-300ke$^-$ and a signal length of somewhat more than 100 ns are important for the design of the preamplifier.

3.) Current TPC designs:
Paul described the currently used typical TPC electronics, in particular the AFTER and the (S-)ALTRO chips. He summarized their characteristic numbers like size, energy consumption, precision, digitization frequency etc. He also mentioned the further developments and the characteristic techniques of the individual chips: AFTER and it successors AGET are based on a switched capacitor array, while in the ALTRO/SALTRO/GdSP design a fast FADC is foreseen for every channel. It was stated, that the AFTER approach is possibly not practical for an ILD-TPC, if all of the bunch train should be recorded (~800 µs). The S-ALTRO in contrast has a too large footprint and a too high current consumtion.

4.) FEE – a chip designers point of view
Fabrice discussed the S-ALTRO ASIC in some more detailed, in particular how the weak points could be improved. He suggested to have a careful discussion which part of the chip does not fulfill the specs, because several issues could be improved by a careful optimization of the chip without a complete redesign. In particular noise, power consumption and event size buffer could easily be improved. Unfortunately, the discussion showed that the required reduction in the footprint would require a new layout. It was also mentioned, that IBM sold its foundries of the 130 nm process to a different company and that the future of this process is therefore unclear.
Fabrice showed also the list of requirements for the common front end developed in the AIDA project. There is a layout for a chip containing only the front end and the simulation of this chip shows good results. The chip will be tested soon.

5.) Requirements of the ILD-TPC
Leif summarized some ideas for the electronics layout of the ILD-TPC. In particular the smaller foot print (<3 mm^2/channel), the larger number of channels per chip, lower power consumption, fewer voltage levels (SALTRO has 8 different voltages), etc were discussed. Leif also added some ideas of how the readout electronics could be implemented, he reported on the HDI (high density interconnect) PCB technology, the 3D stacking of chips and the cooling integrated in the PCB. There were however some caution mentioned, because advanced technologies are usually driven by large volume consumer goods (e.g. mobile phone), which may have slightly different needs. The development and optimization of these techniques for the HEP community can some times take a long time and high financial

resources. It is some times easier to solve the problems in the chip design, but it is worthwhile to look into the advanced PC technologies for a number of reasons.

6.) ADC design:

Hans showed a few transparencies of a 65 nm prototype design done as an exercise in Bonn to study the new technology. A new low power ADC was implemented showing already excellent performance and further improvements are possible by optimization. The 8-bit ADC with 10 MS/s used only 40µW and had a footprint of about 3000µm^2.

7.) Discussion:

During the discussion time several ideas were mentioned and some numbers were discussed in more detail. Here is a random collection of these thoughts:

- It would be important to know what amount of charge has to be expected in a case of a discharge.
- Going to smaller feature sizes does not necessarily gain a smaller footprint or lower power consumption for the analogue part of the chip, but only for the digital part.
- It is rater attractive to do the filtering of the events only in the digital domain. Then only a simple baseline restoration can be used instead of an elaborate shaping unit (usually a (CR-RC)^n circuit) after the preamplifier.
- Different technologies could be used for different tasks: For example a good analog part (e.g. CFE) could be used in one chip in 130 nm and the digital part could be realized in 65nm technology. There are several pros and cons to this approach which have to be carefully evaluated.
- In case of two or more different chip they could be stacked. There are two different connection techniques: Wire bonding or bump bonding on top of each other. Large TSVs (through silicon vias) could help in case the second technology was chosen.
- Bump bonding also of chips on the PCB is a rather major and good technology for the front end electronics.
- Cooling of the endplane seems interesting and should be studied.

A list of parameters which have to be determined by the physics aspects was written. Educated guesses of the numbers were added. These numbers have to be verified by simulations and any help for this would be welcome.

There are some preliminary studies by Lund to two of the numbers (Impact of number of ADC bits and of shaping time on the spatial resolution):
http://www.hep.lu.se/eudet/documents/liangliang-MasterThesis.pdf
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