Requirements on the TPC electronics readout system

Leif Jönsson (on behalf of the Lund group)
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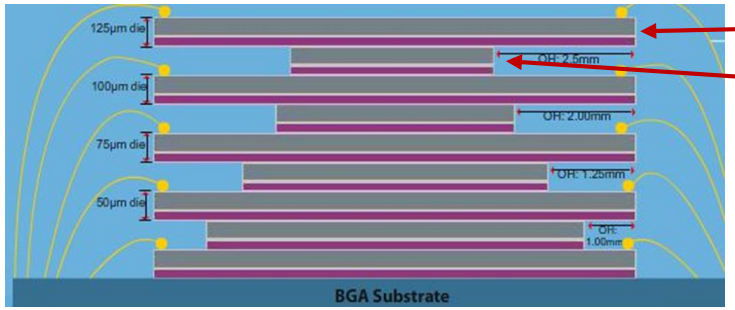
Requirements on the readout electronics

Our experience with the present SALTRO-chip is that it is not ideal for our application but it requires too many cumbersome compromises in the PCB design. Therefore, the development of a new chip is required.

- The new chip should have:
  - Channel occupancy corresponding to 1x4 mm^2, after space for HV connectors and cooling supply has been subtracted (mainly motivated by two-track resolution)
    - more channels per chip (32, 64, 128 ?) and 65 nm CMOS technology?
    - 3D stacking of chips (SALTRO16 could meet space requirements, but the sampling depth is not sufficient and the power comsumption too high)
  - lower power consumption (fast shaping time ⇒ high sampling frequency ⇒ high power consumption)
  - fewer voltage levels ⇒ fewer voltage regulators ⇒ less bulky voltage supply system
  - allow for power pulsing
  - sufficient sampling depth to account for the full drift length
- More elegant cooling system ⇒ microchannel cooling?
- Reduce number of parameters set externally ⇒ use configuration registers

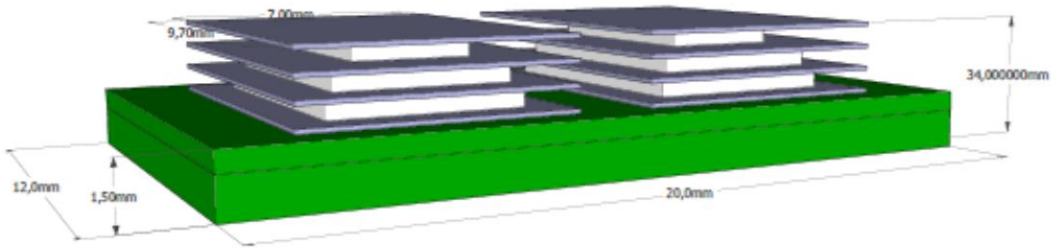
  or even better (from a power consumption point of view) agree upon an optimal running conditions.
- Mounting of the chip carrier boards on the pad planes
  - direct soldering on the pad plane ⇒ avoids micro-connectors
  - connection via microconnectors ⇒ higher flexibility and allows for echange of small units in case of damaged chips. Less heat transmission to the pad plane.
- Minimize the material budget ⇒ PCB-design in HDI-technology
- Optimal dimensions of pad plane?

3D mounting of chips



chip

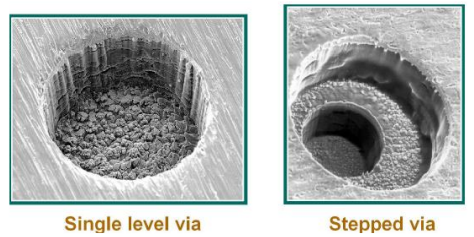
substrate



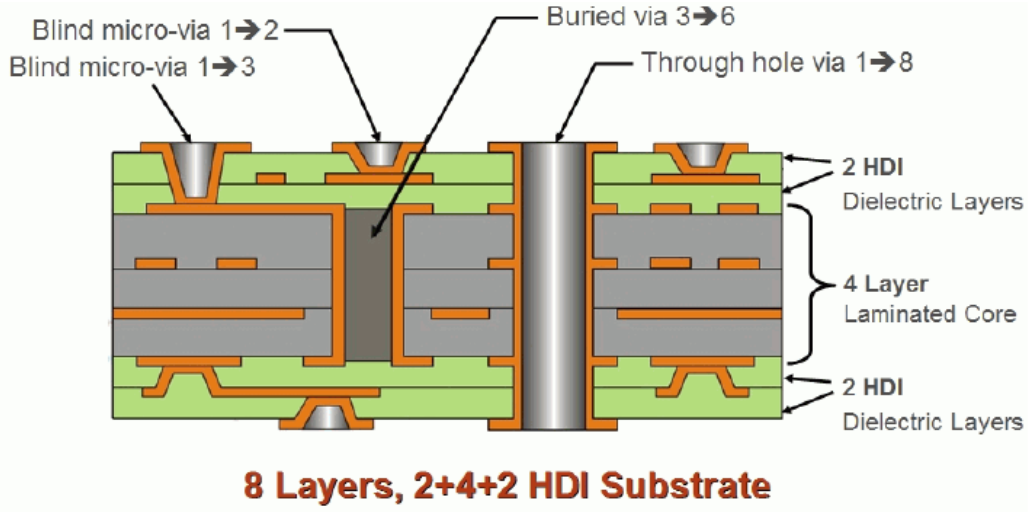
This arrangement corresponds to the present MCM-board (128 channels) with an area of 12x20 mm^2 compared to presently 25x32 mm^2

Advantages of HDI (High density Interconnect) technology

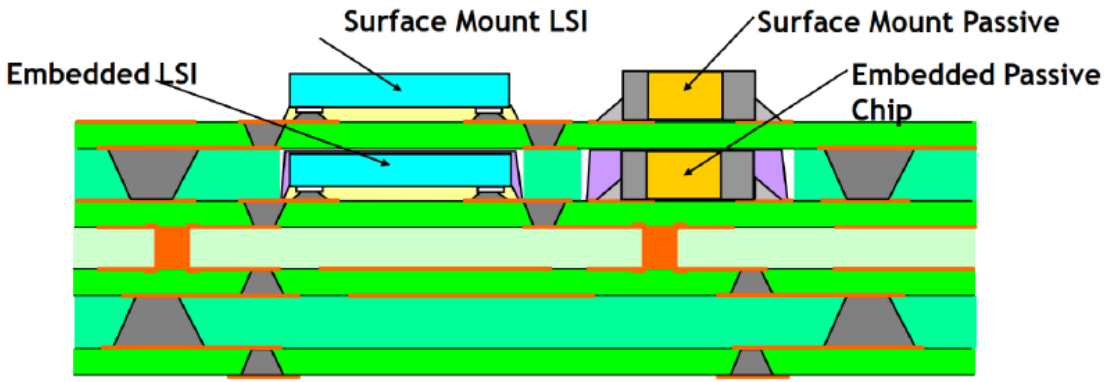
- Routing density higher both for signal and voltage supply
  $\Rightarrow$ number of layers can be decreased
- Laser drilling allows for a holes as small as 25 μm diameter with collars of 50 μm.
- The drilling can be performed to different depths depending on the energy in the laser beam.



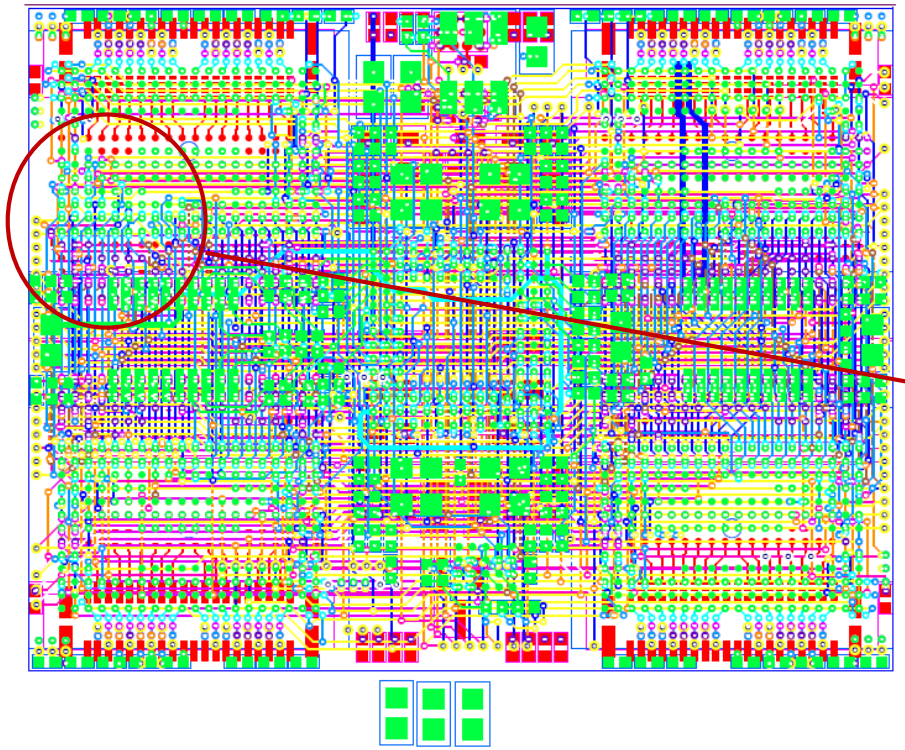
- Together with sequencial laminate application vias can connect different layers.
- The prepreg layers can be as thin as 5 μm.
- Due to via-in-pad techniqies all routing can be performed in the inner layers such that essentially the whole surface can be used for mounting of components.

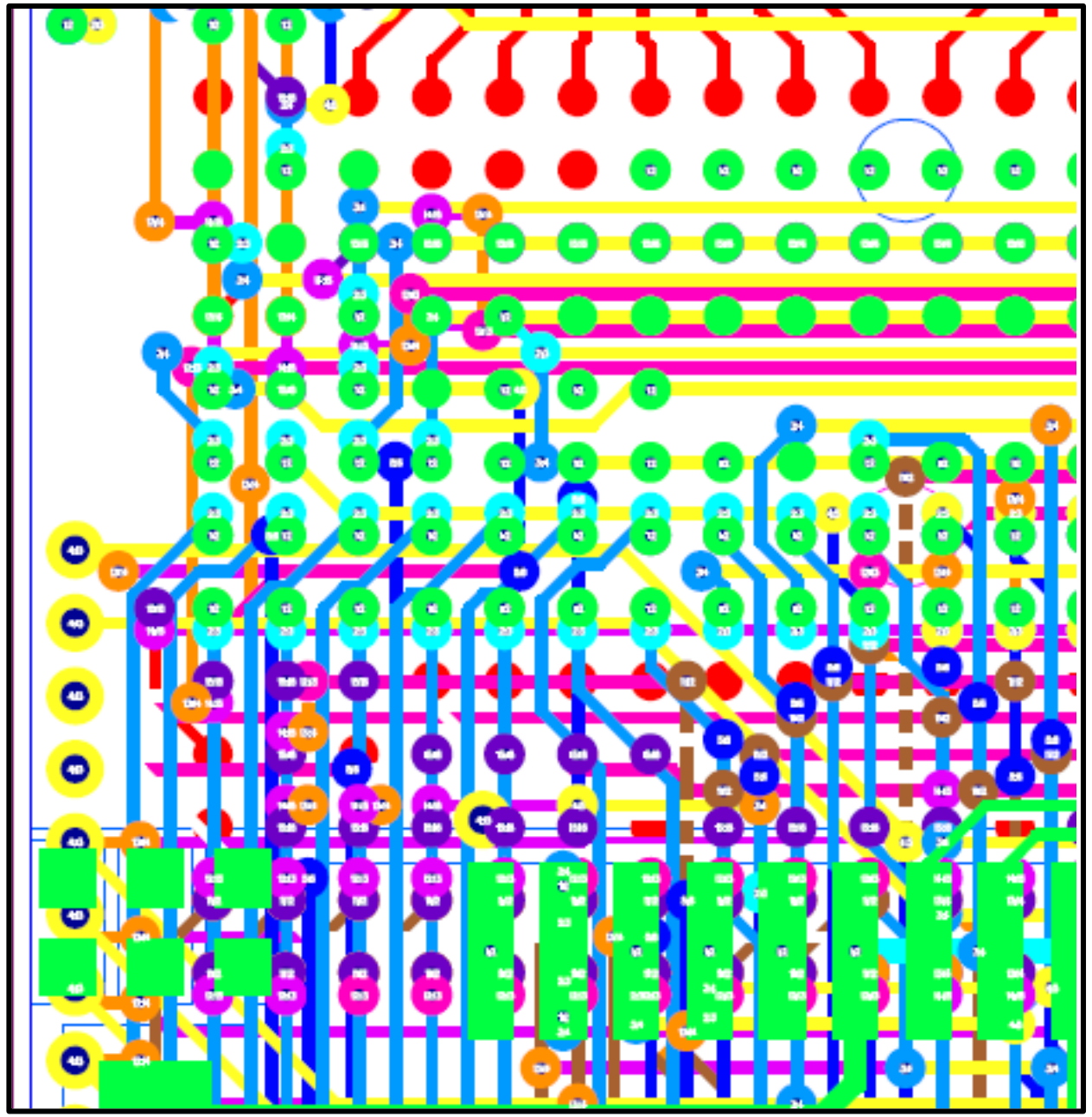


This technology also offers the possibility to create cavities in the PCB where electronic och mechanical components can be mounted and thus embedded into the PCB so that essentially the full surface is available for surface mounting of chips.



The MCM-board in HDI-design





The layer structure of the MCM-board in HDI design

			0.20mm mech drill	0.20mm mech drill	0.08mm laser	0.08mm laser	0.08mm laser	0.08mm laser	0.08mm laser
layer 1	copper foil	36							0.28mm
prepreg HDI	high Tg	60							
layer 2	copper foil	36						0.28mm	
prepreg HDI	high Tg	60							
layer 3	outer copper	36					0.28mm		
prepreg HDI	high Tg	100							
layer 4	inner copper	18	0.40mm			0.28mm			
core	high Tg	65							
layer 5	inner copper	18			0.28mm				
prepreg	high Tg	100							
layer 6	inner copper	18		0.40mm					
core	high Tg	65							
layer 7	inner copper	18							
prepreg	high Tg	100							
layer 8	inner copper	18							
core	high Tg	65							
layer 9	inner copper	18							
prepreg	high Tg	100							
layer 10	inner copper	18							
core	high Tg	65							
layer 11	inner copper	18							
prepreg	high Tg	100							
layer 12	inner copper	18							
core	high Tg	65							
layer 13	inner copper	65							
prepreg HDI	high Tg	100							
layer 14	outer copper	36							
prepreg HDI	high Tg	60							
layer 15	copper foil	36							
prepreg HDI	high Tg	60							
layer 16	copper foil	36							

Yellow = copper layers
Hatched green = prepreg layers
Full green = core layers

Total thickness = 1608 µm

Microchannel cooling

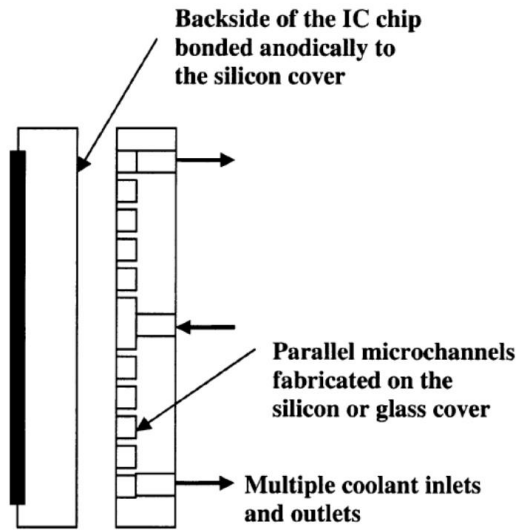
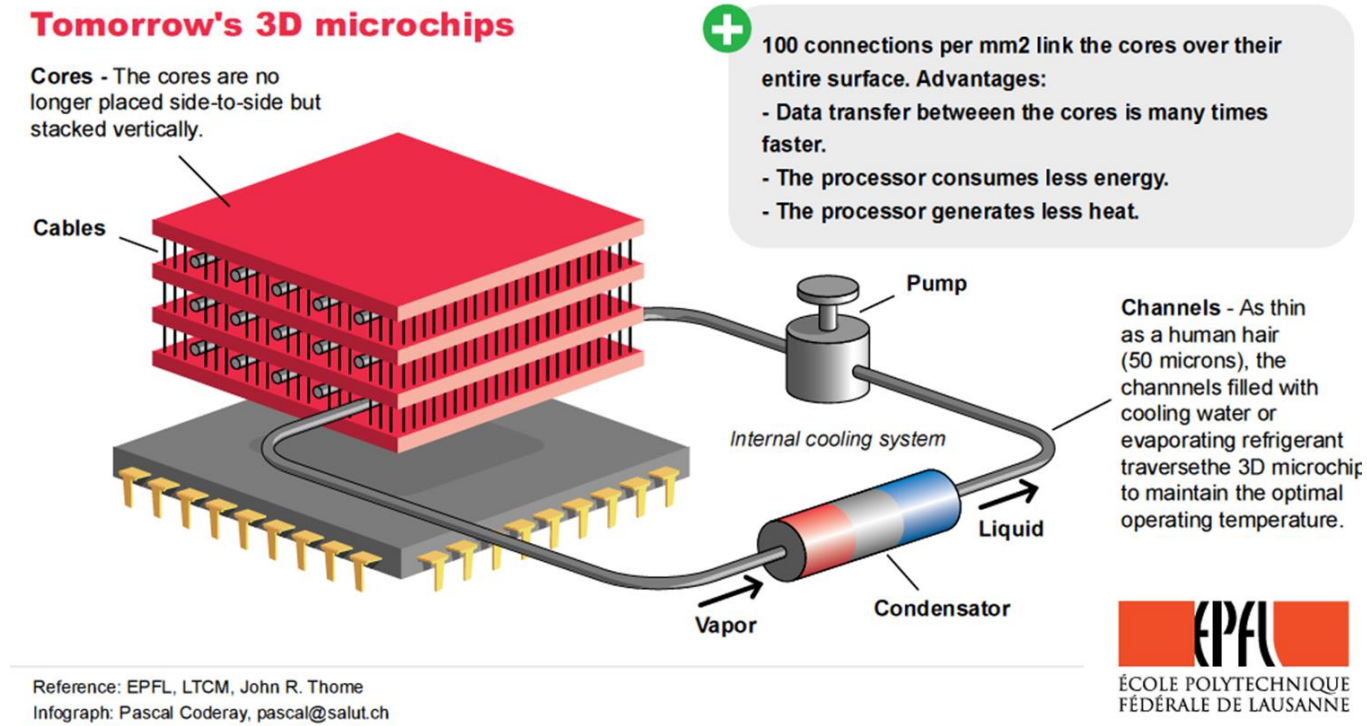


Figure 2 Schematic arrangement of an IC chip cooled with microchannels fabricated on a silicon or glass cover bonded anodically or glued to the backside of the chip (not to scale).



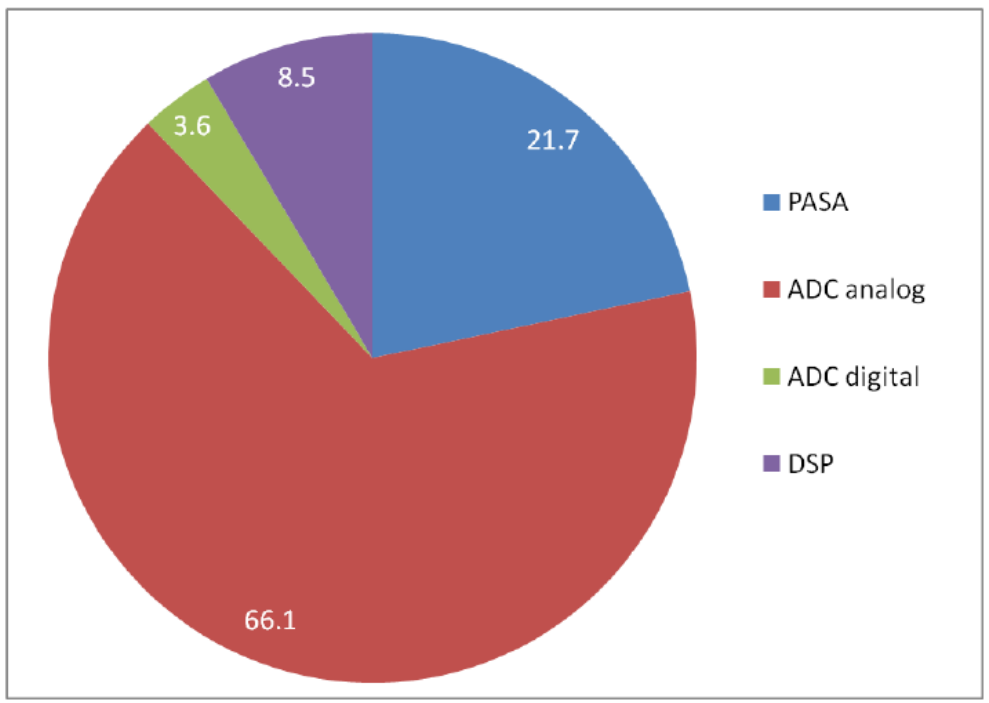
Planned beam structure for the various stages of the ILC

Table 12.1. Primary parameters for a proposed 250 GeV centre-of-mass-energy first stage, the luminosity upgrade for the 500 GeV baseline machine, and the two parameter sets for the TeV upgrade: low Beamstrahlung (A) and high Beamstrahlung (B). The baseline 500 GeV parameters are included for reference.

			Baseline	1st Stage	L Upgrade	TeV Upgrade A	TeV Upgrade B
Centre-of-mass energy	E_{CM}	GeV	500	250	500	1000	1000
Collision rate	f_{rep}	Hz	5	5	5	4	4
Electron linac rate	f_{linac}	Hz	5	10	5	4	4
Number of bunches	n_b		1312	1312	2625	2450	2450
Bunch population	N	$\times 10^{10}$	2.0	2.0	2.0	1.74	1.74
Bunch separation	Δt_b	ns	554	554	366	366	366
Pulse current	I_{beam}	mA	5.79	5.8	8.75	7.6	7.6

Measured standby power consumtion of the SALTRO16-chip in mW

Power domain	Power/channel	Total power
PASA	10.26	164
ADC analog	31.28	500
ADC digital	1.71	27
Digital Core	4.04	65
Chip total	47.3	757



Ideas on power pulsing schemes for the SALTRO-system

Power pulsing can be implemented either by removing the supply voltages or by using the shut-down features:

- Switching off the preamplifier dynamically
- Disconneting the biasing resistor of the ADC dynamically
- Removing the sampling clock and/or the readout clock dynamically
- Shutting down the the voltage regulators dynamically
- Reducing the voltage supply of the Digital Signal Processor (DSP)

The option of shutting down the voltage regulators implies large switching currents to charge and discharge all supply decoupling capacitors.

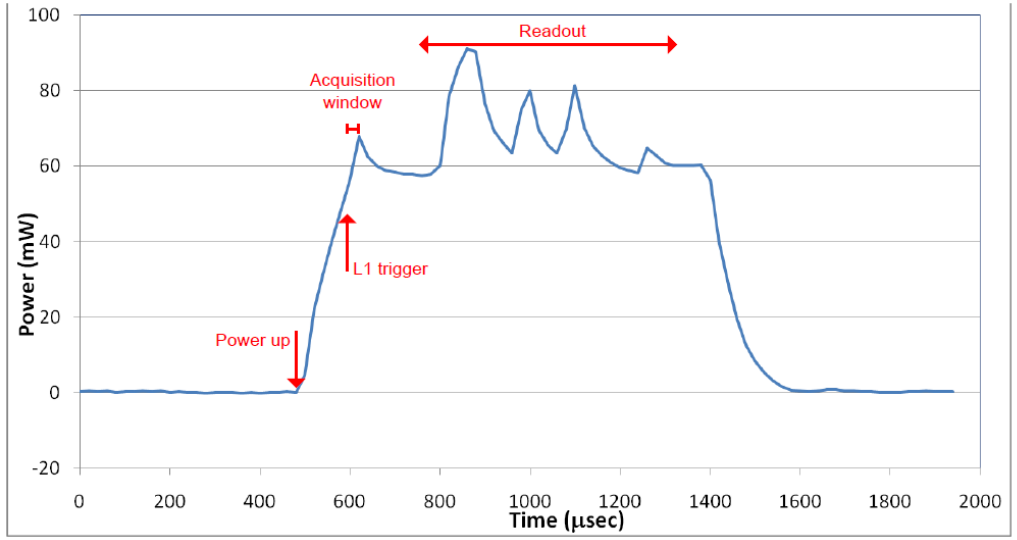
From a system point of view, a much more advantegous option is to let dedicated control lines act:

- on the shutdown line of the preamplifier
- on the biasing resistor of the ADC
- on the enabling of the sampling and readout clock

In this way, all supply voltages remain constant and decoupling capacitors keep their charge.

For the new chip one can imagine to integrate the power pulsing scheme in the chip, which is activated throug a shut down input signal

Power pulsing tests with the SALTRO16-chip



Power pulsing

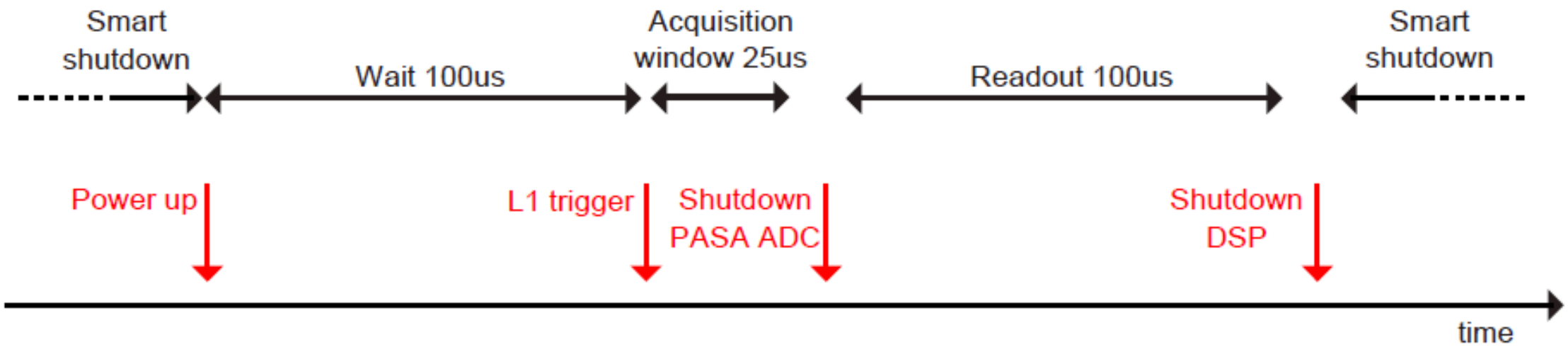
Power domain	Smart Shutdown (mW)	Power pulsing cycle (μJ)
PASA	2.12	145.2
ADC analog	6.88	421.1
ADC digital	$\approx$0	22.9
Digital Core	0.16	58.3
Digital Pads	$\approx$0	6.9
Total	9.2	654.3

Without power puling

Power domain	Power/channel
PASA	10.26
ADC analog	31.28
ADC digital	1.71
Digital Core	4.04
Chip total	47.3

A power pulsing scheme for the SALTRO-system where the preamplifier (PASA) and the ADC are only active for 150μs per cycle

If the preamplifier and ADC are shut down right after the data aquisition window, whereas the DSP performs the readout, a further reduction of a factor 5 is expected in the power consumption per power pulsing cycle.



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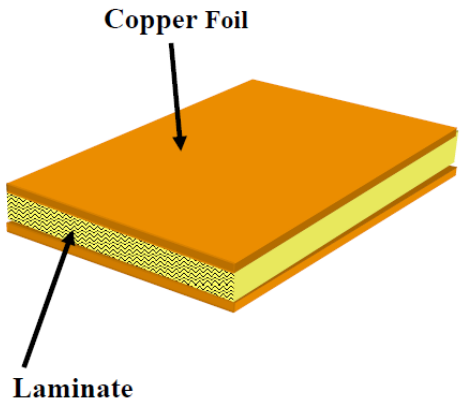
Back-up slides

The principle layout of the multi layer board

- A multi layer PCB is produced by stacking a number of core layers and pre-preg layers.
- A core layer is a thin dielectric consisting of cured fibre glass epoxy resin, with copper foil bonded to both sides.
- A pre-preg layer is a thin sheet of fibre glass, impregnated with uncured epoxy resin, which hardens when heated and pressed in the PCB fabrication process.
- Pre-pregs can be stacked to achieve the desired thickness.
- The difference between core and prepreg layer lies in the roughness of the fibre material and what epoxy material being used.

Multi-layer fabrication begins with the selection of an inner layer core – or thin laminate material of the proper thickness. Cores can vary from 0.038" to 0.005" thick and the number of cores used will depend upon the board's design.



The basic materials needed to build a multi-layer board are copper foil, prepreg and inner-layer cores.