Krakow, IFJ-PAN, ILD Pre-meeting
September 18, 2014

Current TPC electronics

P. Colas

- Orsay May 10, 2011, TPC electronics discussion
- GDsP CERN, starting July 2011 (converged to CFE)
- Krakow, IFJ-PAN, ILD Pre-meeting, Sept 24, 2013
- ECFA-Pannel Detector review, DESY, Nov. 4, 2013
- LC-TPC collaboration meeting, DESY, June 2014
  - Decision to start a group of electronic experts (physicists and designers) to follow the evolution of technologies and guide the preparation of a 'list of requirements'

Past TPCs and electronics for beam tests

- ALEPH and DELPHI. Discrete amplifiers (1 channel each), FADCs 12 MHz

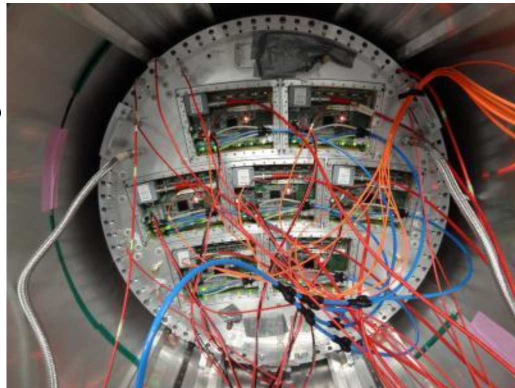
    Used for prototype tests (KEK 2005-2006)

- Carleton amplifiers. 200 MHz sampling
- STAR electronics : full wave sampling at 10-40 MHz by SCA, 10 bit ADC (out of 12 bits available)
- Then used AFTER (for Micromegas) and ALTRO (for GEMs)
  - AFTER Evolved to GET and AGET
  - ALTRO Evolved to SALTRO

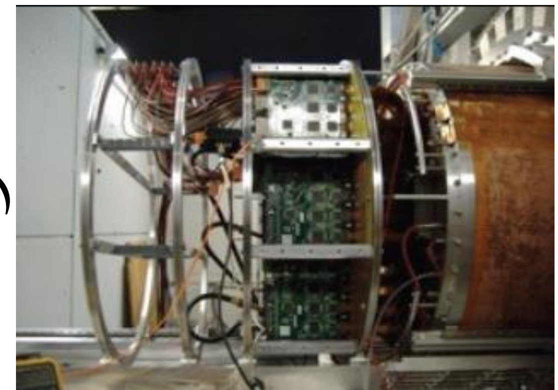
- Electronics for LP: AFTER and SALTRO-16

Readout		Pad Size	Electronics	Groups
MPGDs	Micromegas (Resistive anode)	(~ 3 × 7 mm^2 Pad)	AFTER	Saclay-Carleton
	Double GEMs (Laser-etched)	(~ 1 × 6 mm^2 Pad)	ALTRO	Asia
	Triple GEMs (wet-etched)			Desy

Micromegas (test with 7 modules)



GEM (test with 3 modules)



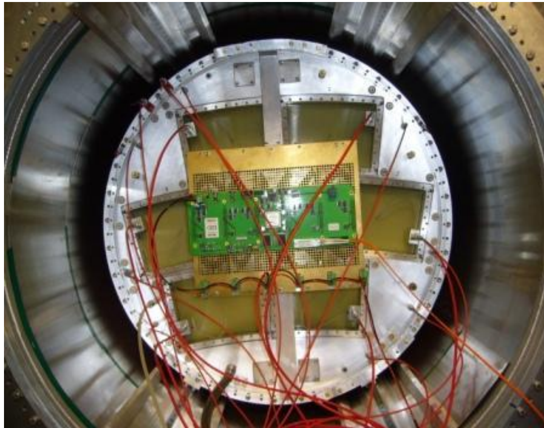
- The road to the electronics for ILD.

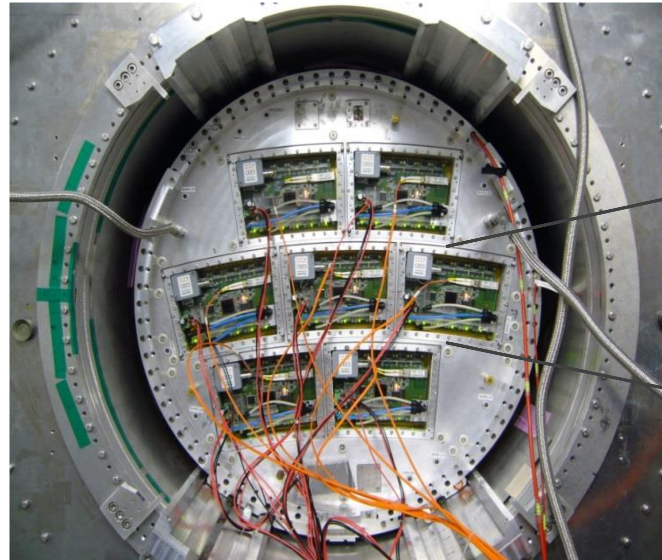
News and progress report from prototype electronics

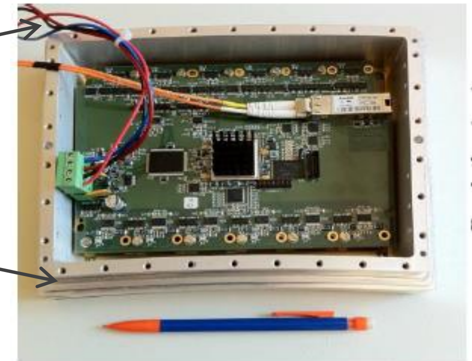
- **AFTER**-based (ASIC For TPC Electronic Readout). Designed at Saclay for T2K. Adapted in 2011-2012 to the Large Prototype. 72 channel Amplifier-shaper, full wave sampling by Switched Capacitor Aray, large versatility (1-100 MHz, 100-2000 ns peaking time, 120 to 600 pC full scale, 12 bit ADC).
- **ALTRO**-based (ALice TPC Read Out). SALTRO: evolution from Alice readout, 16 channel Amplifier-shaper 60-200 ns peaking time, 25 MHz and 40 MHz sampling , Digital filtering, memory buffering.

AFTER integration to fully cover the endplate of LP-TPC (2012-2013)

D. Attié, D. Calvet, P. Colas, E. Delagnes, A. Le Coguie, M. Riallot et al.







The integration has been carried out so that the new electronics is flat behind the modules, and fits in 25 X° and 5 cm, with comfortable margins. It requires 3 connections only: 1 optical fibre, 1 LV and 1 HV.

Remaining refinements are going on (for March 2014):

- More robust connections
- 2P CO2 cooling

Integrated electronics

- Remove packaging and protection diodes
- Wire-bond AFTER chips
- Use two 300-point connectors

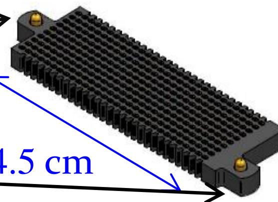
Front-End Card (FEC)

14 cm

25 cm

12.5 cm

2.8 cm



4.5 cm

AFTER Chip

3.5 cm

3.5 cm

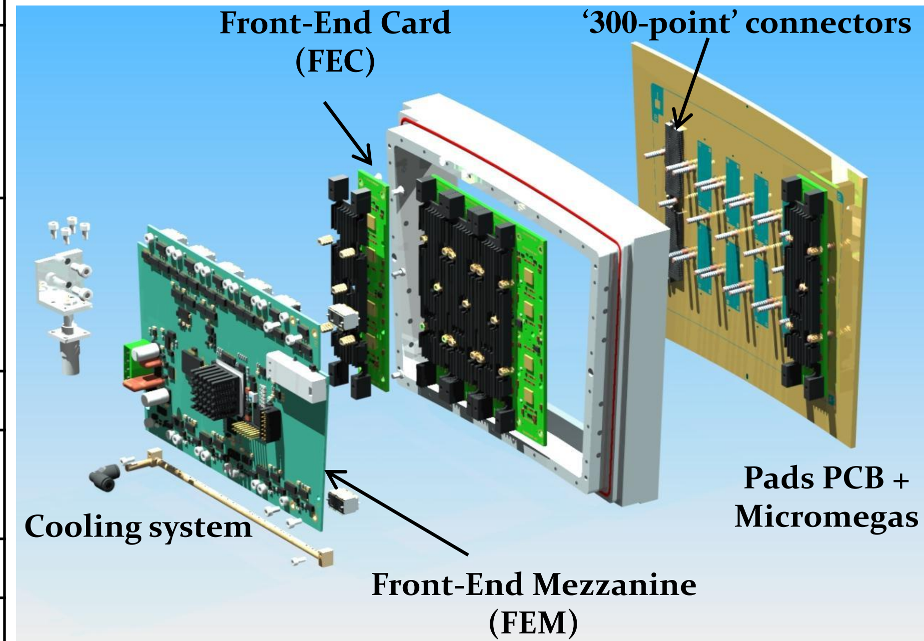
0.78 cm

0.74 cm

The resistive foil protects against sparks

Material budget of a module

		M (g)	Radiation Length (g/cm²)
Module frame + Back-frame + Radiator (×6)	Al	714	24.01
Detector + FEC PCB (×6) + FEM	Si	712	21.82
12 '300-point' connectors	Carbon	30	42.70
screws for FEC + Stud screws+	Fe	294	13.84
Air cooling	brass	12	12.73
	Plexiglas	128	40.54
Average of a module		1890	21.38



Low material budget requirement for ILD-TPC:

- **Endplates: ~25% X_0**
  (X_0: radiation length in cm)

$$\frac{d}{X_0} = 0.236 < 0.25$$

AGET (**A**SIC for **G**eneral **E**lectronics for **T**PC)

- Four ASICs are soldered on the AsAd (**A**SIC **S**upport & **A**nalog-**D**igital conversion) card with four 12-bit ADC (one per AGET). The digital outputs of the 4 ADCs are transmitted by 8 differential lines with a maximum speed of 1.2 Gbit/s to the CoBo board.
- The CoBo (**Co**ncentration **Bo**ard) board is responsible for applying a time stamp, zero suppression and compression algorithms to the data. It will also serve as a communication intermediary between the AsAd and the outside world. The slow control signals and commands to the AsAd will be transmitted via the CoBo (four AsAd per CoBo).
- Much faster (2 kHz DAQ rate instead of 50 Hz)

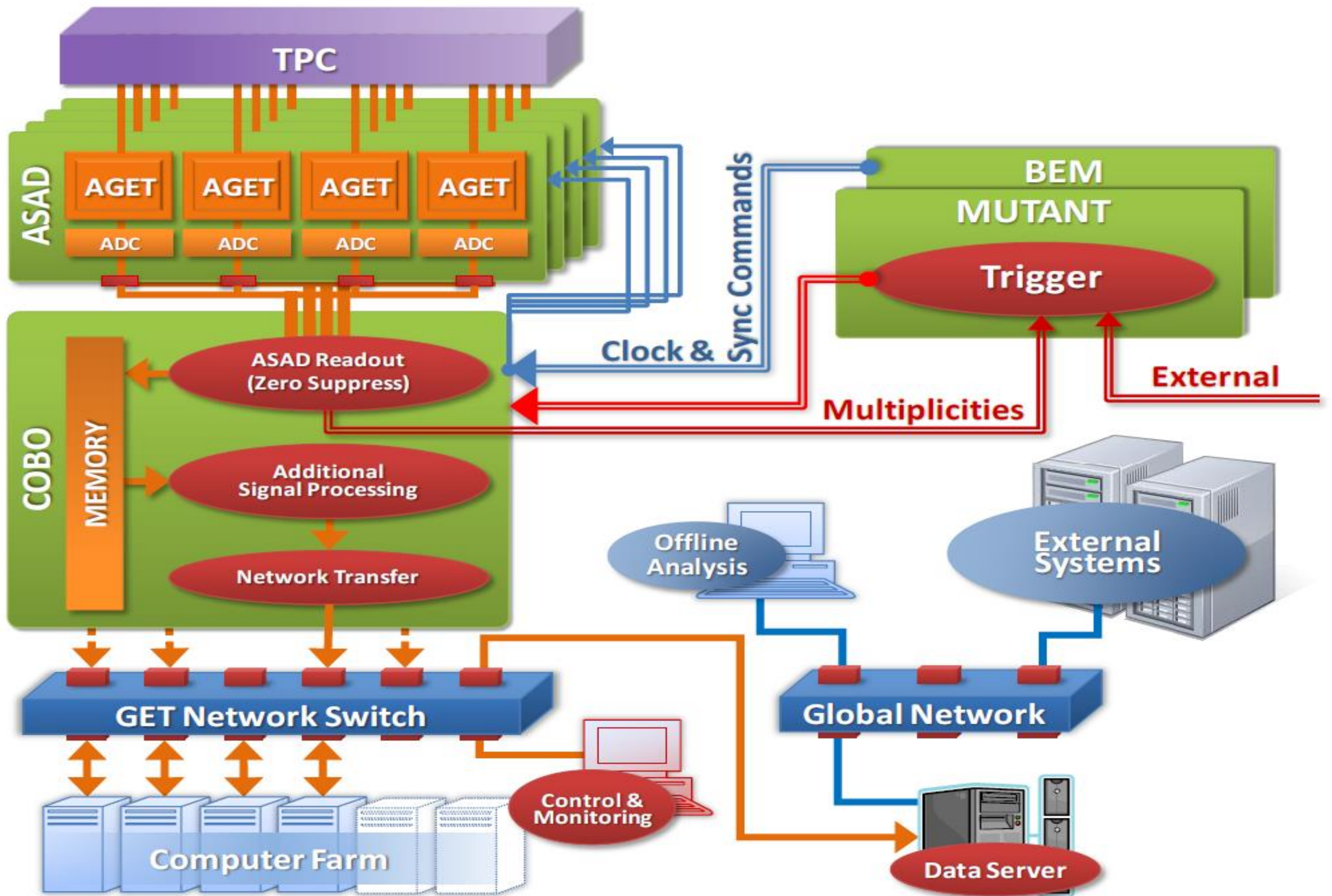


Fig. 1: Global view of the GET electronic.

S-ALTRO 16 Developments

V. Hedberg, L. Jönsson, B. Lundberg, U. Mjörnmark, A. Oskarsson, L. Österman

- Chip and carrier board
- Test Socket and Test Socket Board
- MCM board (multichip module) and its prototype
- The CPLD chip
- Ancillaries: LV board,…
- DAQ with SRU (Scalable readout unit from RD51)

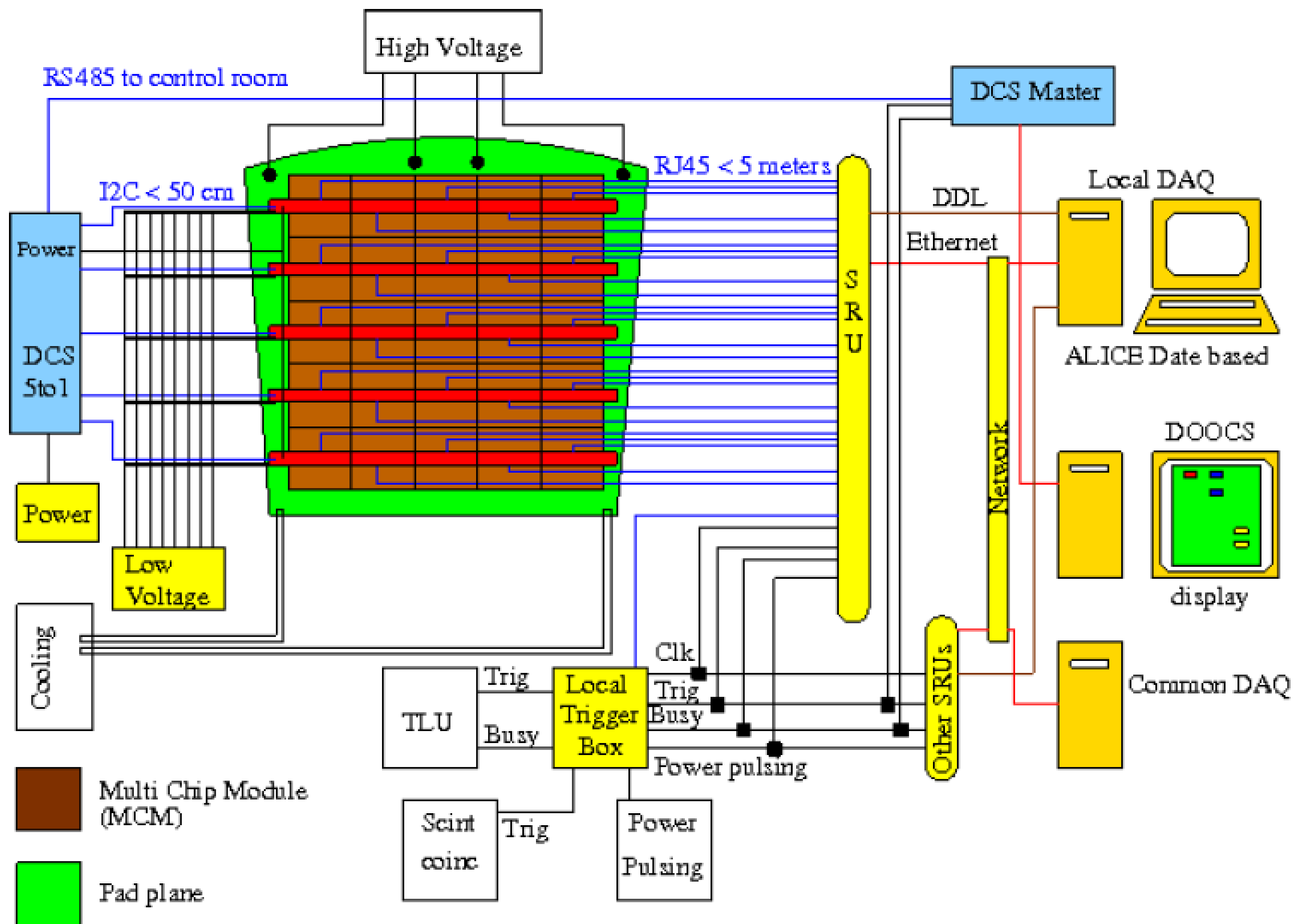
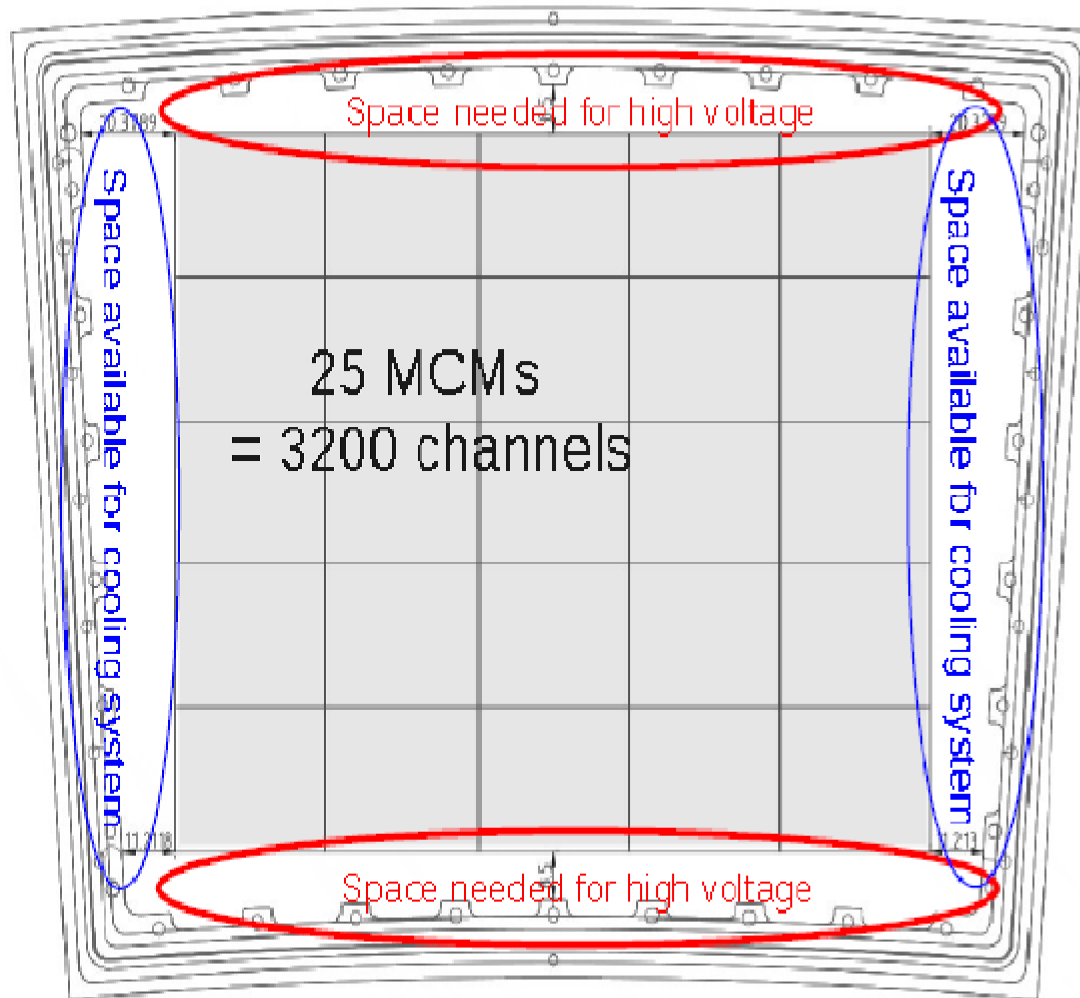


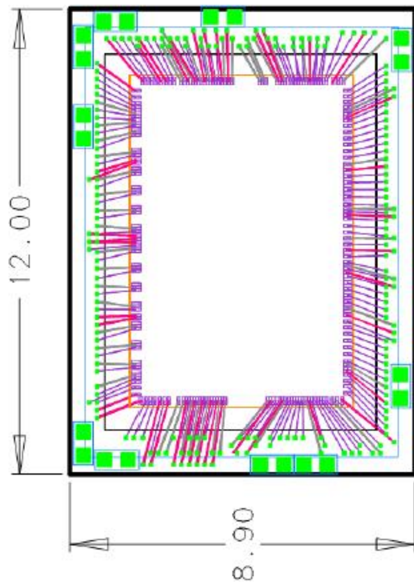
Figure 1: *Schematic view showing the DAQ architecture of the SALTRO system.*

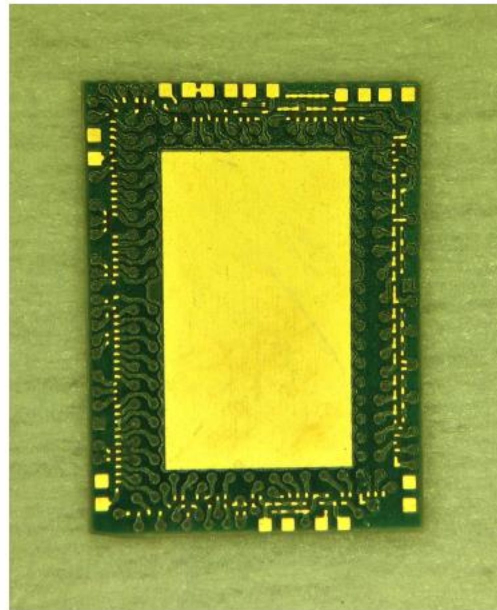
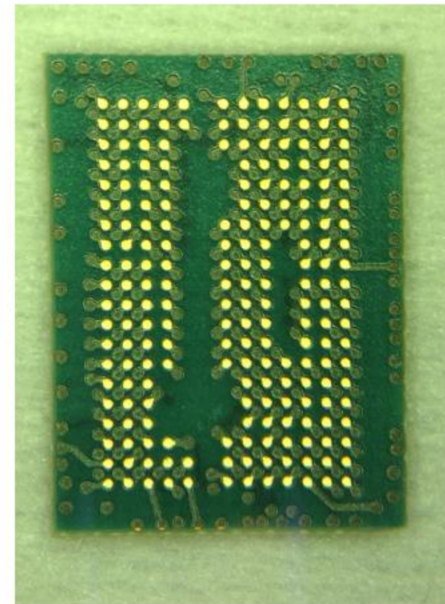
MCMs on a pad board



Carrier board

- Arrived in Lund on 19/9/2013
- Fully cabled and ready for testing end October



- For the final electronics, dies could be either wire bonded to the MCM or mounted by chip-flip tech.

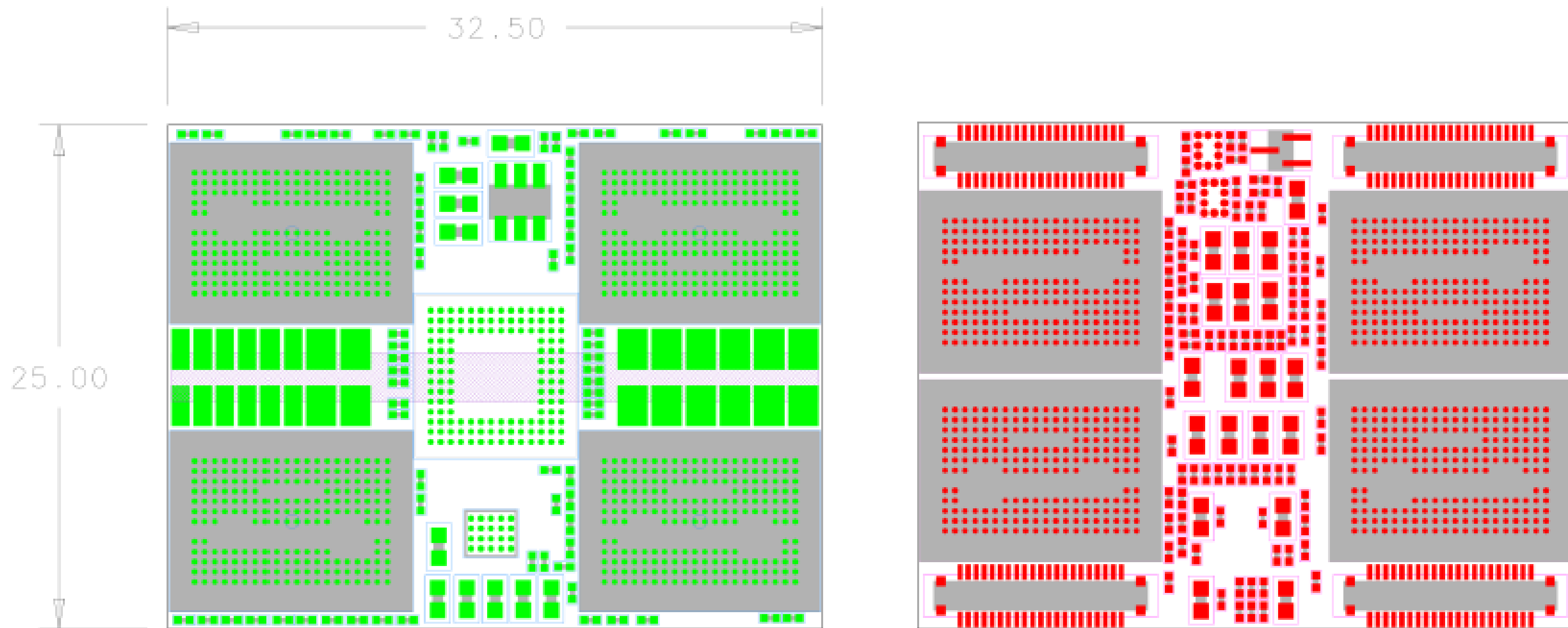
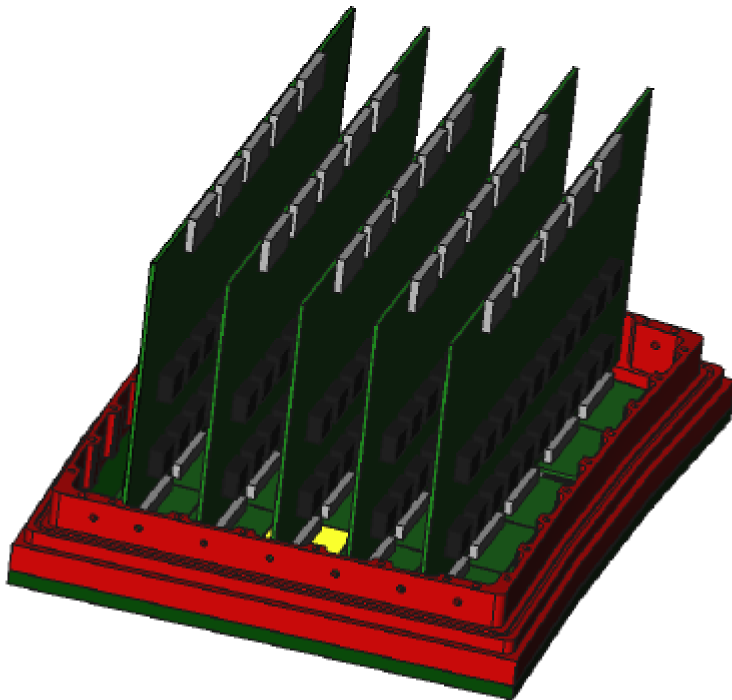


Figure 4: *The MCM-board top surface (left, green) and bottom surface (right, red)*

The Low Voltage board



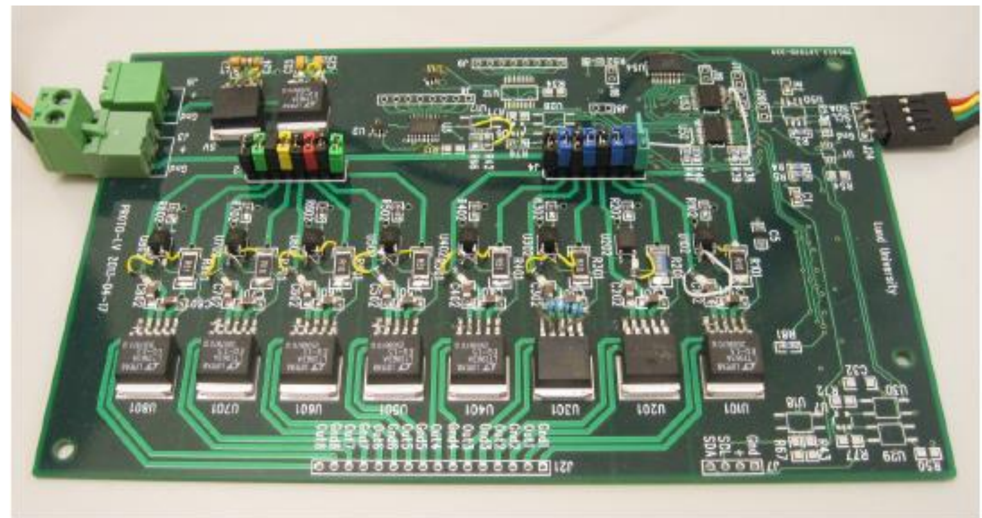
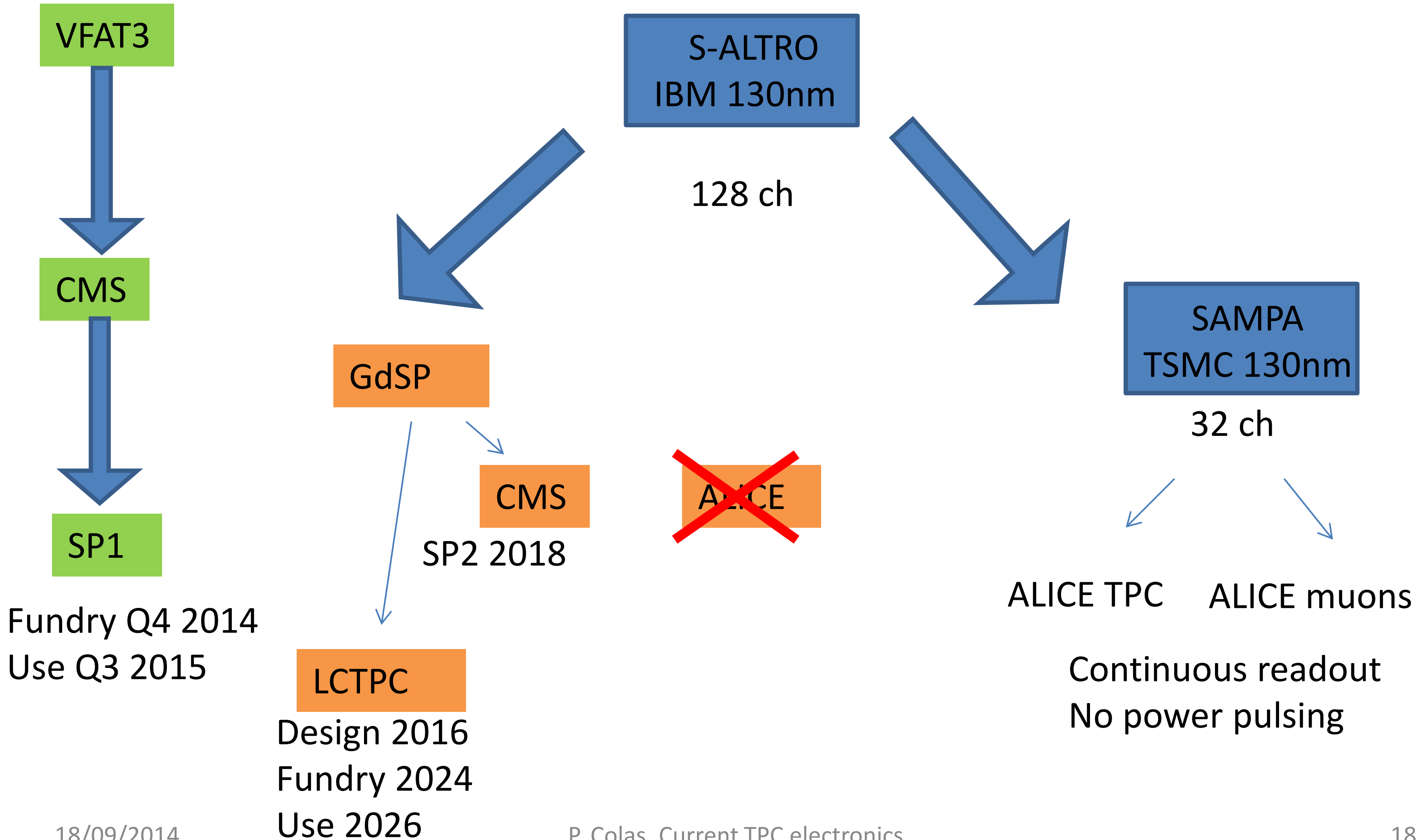


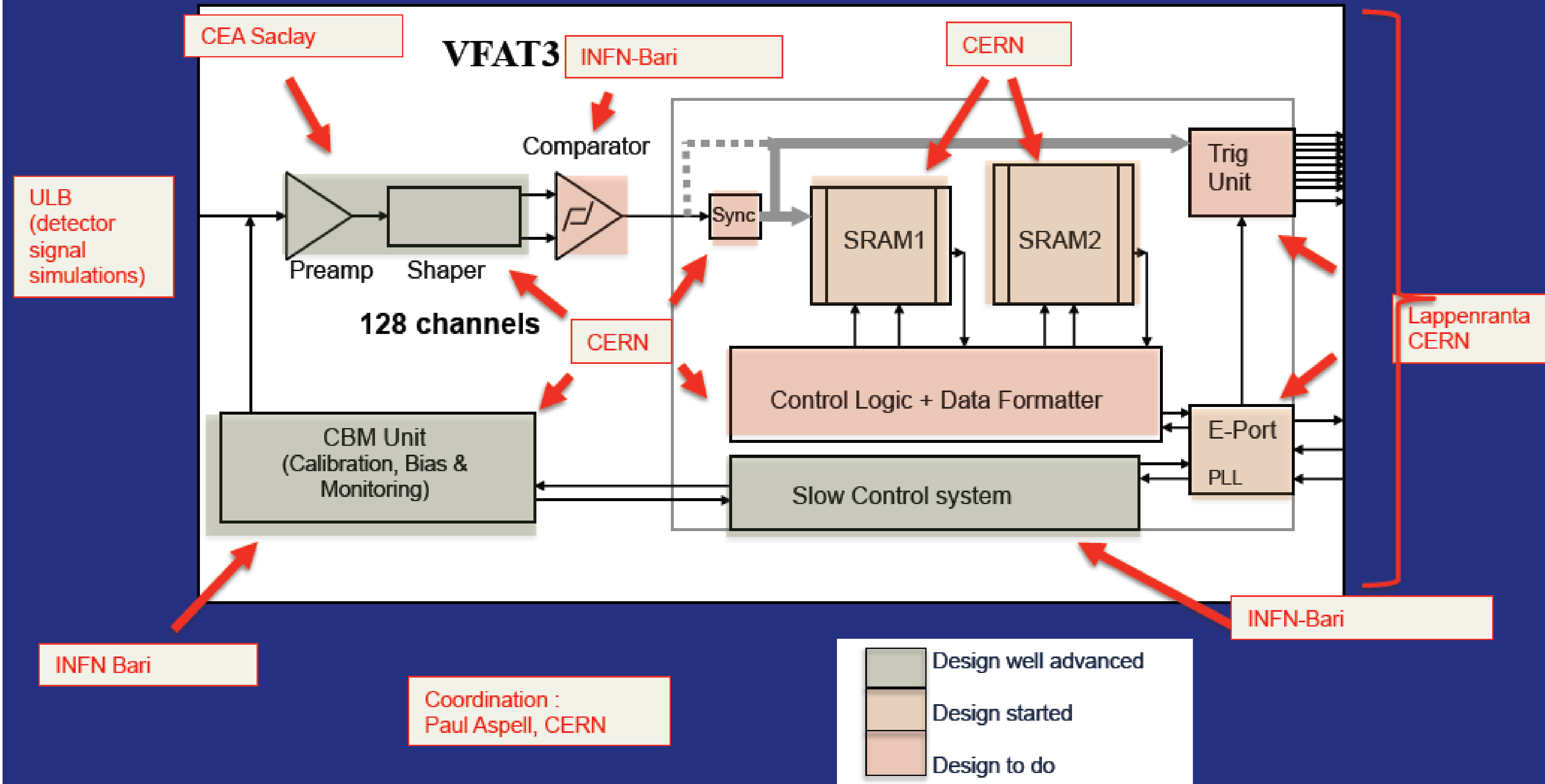
Figure 7: *The LV Prototype Board.*

Future electronics

- GdSP (Paul Aspell et al.), joint R&D with other applications.
- Common Front End : part of a multi-user wafer to test several options, within AIDA.

Developments in progress




VFAT3 design institutes
CEA Saclay
VFAT3
INFN-Bari
CERN
Comparator
ULB
(detector
signal
simulations)
Preamp
Shaper
Sync
SRAM1
SRAM2
Trig
Unit
128 channels
CERN
Lappenranta
CERN
Control Logic + Data Formatter
CBM Unit
(Calibration, Bias &
Monitoring)
E-Port
PLL
Slow Control system
INFN-Bari
INFN Bari
Coordination :
Paul Aspell, CERN
Design well advanced
Design started
Design to do
P. Aspell CERN
CMS Upgrade week DESY June 2013

The CFE project (Paul Aspell et al.)

Common Front End Design Overview *CEA \ DSM \ IRFU*

Fabrice Guilloux

CONTEXT:

The *common front end* study (CFE) is a prototype toward two new *application specific integrated circuits* (ASIC): the *gaseous detector signal processing* (GdSP), a general purpose gaseous detectors readout ASIC and VFAT3 a “trigger and tracking” front end.

GdSP is the natural successor of the *super Alice time projection chamber readout* ASIC (SAltro) - designed and tested at CERN - sharing with it a multichannel architecture and providing for each channel a complete analogue to digital data processing chain, i.e. a charge sensitive amplifier, an analogue filter, an analogue to digital converter circuit and a digital signal processing unit. This architecture is expected to be suitable to the *linear collider time projection chamber* (LC-TPC) project and is kept as a second option for the GEMs for CMS project. Alice-TPC and Alice-dimuon spectrometer experiments have also shown some interest about this ASIC concerning

…but ALICE electronics is being made in Brazil…

Future electronics

- Need to refine the specifications: packing (number of channels per unit surface), number of bits for the ADC, frequency, noise, shaping time, etc…
- Simulation required to justify the specifications
- Need to have in LC-TPC a team including specialists to monitor the electronics R&D
- Define the technology (130 nm? 95 nm?...) at the time of final design and vendor selection. Detailed design depends on the technology and is prone to become obsolete if choices are done too early.
- The feasability of the project is demonstrated (though 1mm pads are still challenging).