universitätbonn

Chip Developments of the Bonn Group

Hans Krüger, Bonn University

ASIC Design Projects

- ATLAS Pixel Detector
  - Hybrid pixel sensors
    - FE-I3 (250nm, current pixel detector)
    - FE-I4 (130nm, Insertable B-layer, current upgrade) → done
    - FE-x (65nm, future HL upgrade, RD53 collaboration) → work just started
  - Fully depleted Active CMOS Sensors (DMAPS)
    - Commercial CMOS technology for the sensing layer, monolithic or hybrid → HL upgrade option

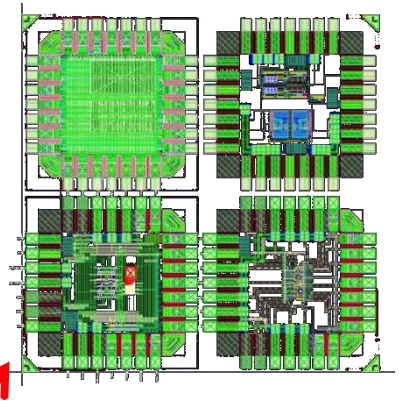
- Belle II Pixel Vertex Detector (SuperKEKB e+ / e- collider)
  - Digital signal processing on pixel module (65nm, DHP chip) → (alomost) done
    - 1.6GHz PLL
    - High speed serial links
    - High density digital signal processing
    - Low power, high density 10 Msps 8-bit ADC

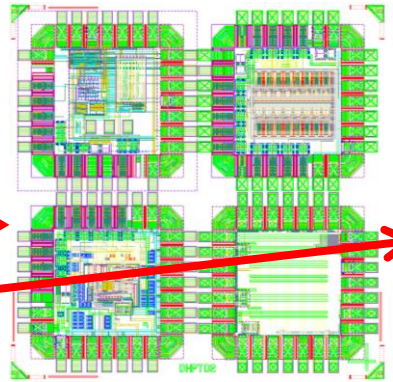
- X-ray imaging (low energy, synchrotron light sources, X-FEL)
  - AGIPD (130nm hybrid pixel detector, XFEL@DESY)
  - New developments: monolithic or hybrid with active CMOS sensors

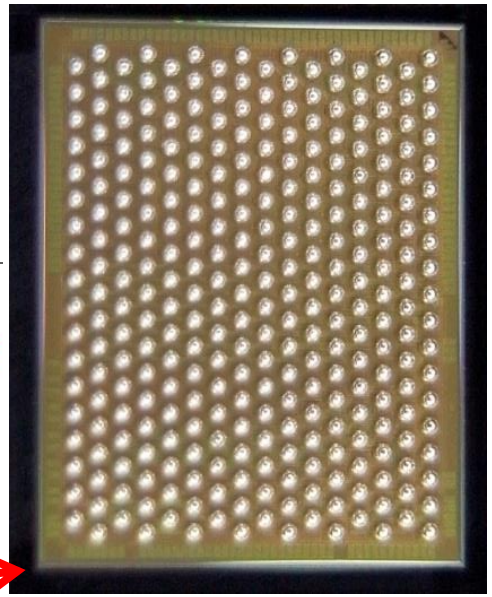
65nm CMOS Design Activities – Belle II

Projects

- DEPFET Pixel Vertex Detector for BELLE II (2015)
  Data handling processor (DHP), mainly digital design, including full custom blocks:
  - PLL (1.6 GHz)
  - High speed serial link (1.6 Gbps)
  - LVDS IO
- „Generic“ (future pixel chips)
  - Low power analog front-end (CSA + discr.)
  - Low power, small area ADC
  - SEU test structures







Chip submissions

- DHPT 0.1, four chiplets, Oct. 2011
- DHPT 0.2, four chiplets, June 2012
- DHPT 1.0
  - 14 mm^2 MPW
  - C4 bumps

Chip Design Activites – RD53

- Focused on 65nm CMOS technology for HL pixel detector upgrades
- Joint CMS/ATLAS (+CLIC) development
- RD53 collaboration recommended by LHCC June 2013
  - Institutes: 17 (+ 3 new applicants)
    - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
    - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
  - Collaborators: ~100, ~50% chip designers
  - Initial work program covers ~3 years to make foundation for final pixel chips
  - Co-spokes persons: ATLAS: M. Garcia-Sciveres, LBNL. CMS: J. Christiansen, CERN
- RD53 web: www.cern.ch/RD53/

universitätbonn

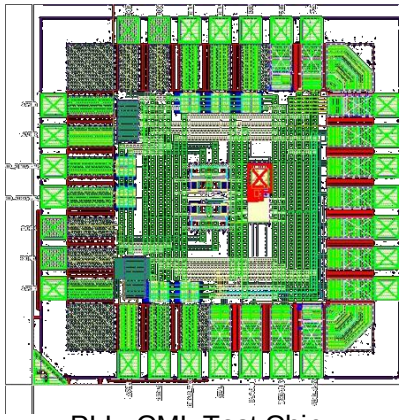
RD53 Working Groups

WG	Domain
WG1	Radiation test/qualification: M. Barbero, CPPM
Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm	
WG2	Top level: (M. Garcia-sciveres, LBNL)
Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.	
WG3	Simulation/verification framework: T. Hemperek, Bonn
System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells	
WG4	I/O : To be started
Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.	
WG5	Analog design / analog front-end: V. Re, Bergamo/Pavia
Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends	
WG6	IP blocks: (J. Christiansen, CERN)
Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation	

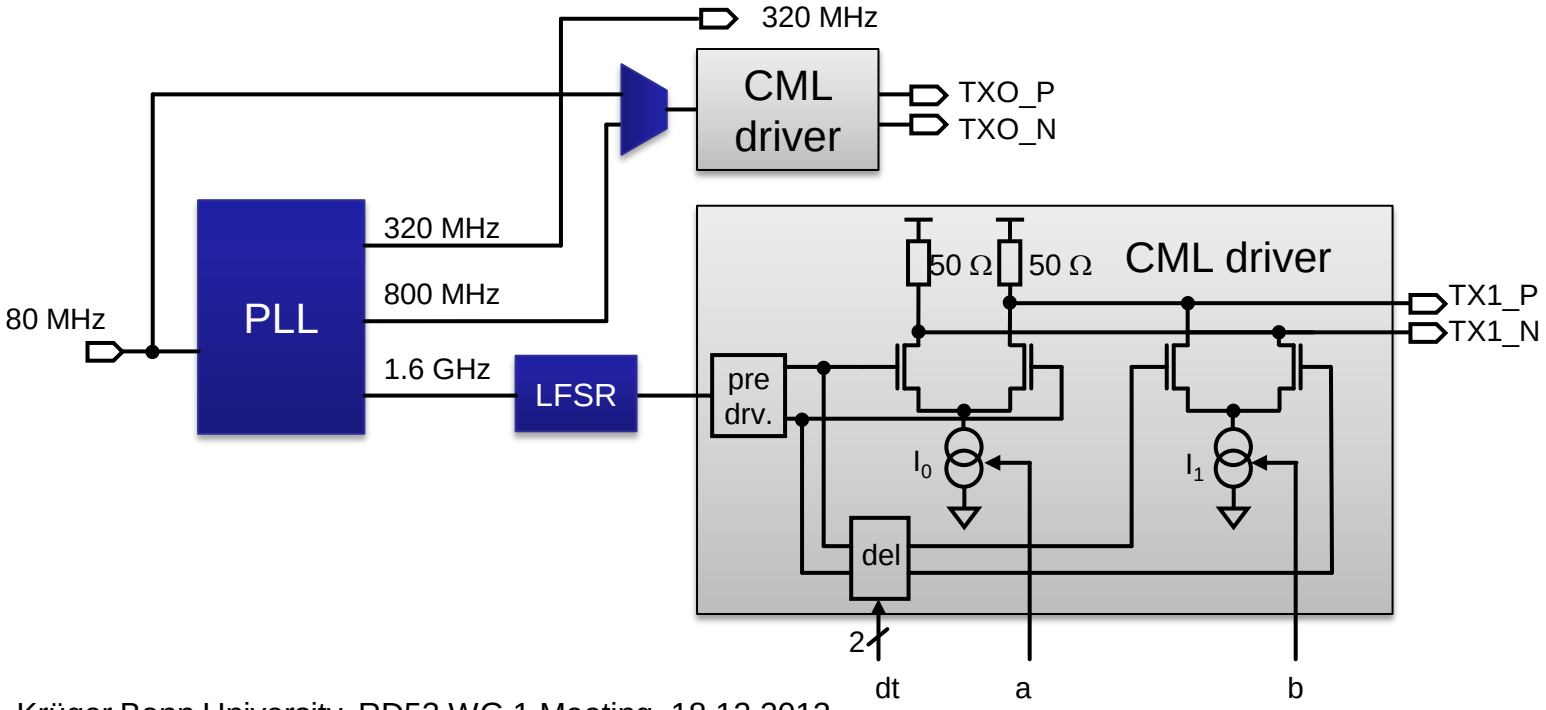
- Backup

PLL & High Speed Link Driver

- PLL
  - 80 MHz reference clock
  - 1.6 GHz, 800MHz & 320 MHz outputs
- Pseudo random bit sequence generator (8 bit LFSR)
- Current mode logic (CML) driver
  - Programmable pre-emphasis (first order FIR filter)
  - Two differential pairs with adj. bias currents (tap weights a, b)
  - Programmable delay dt

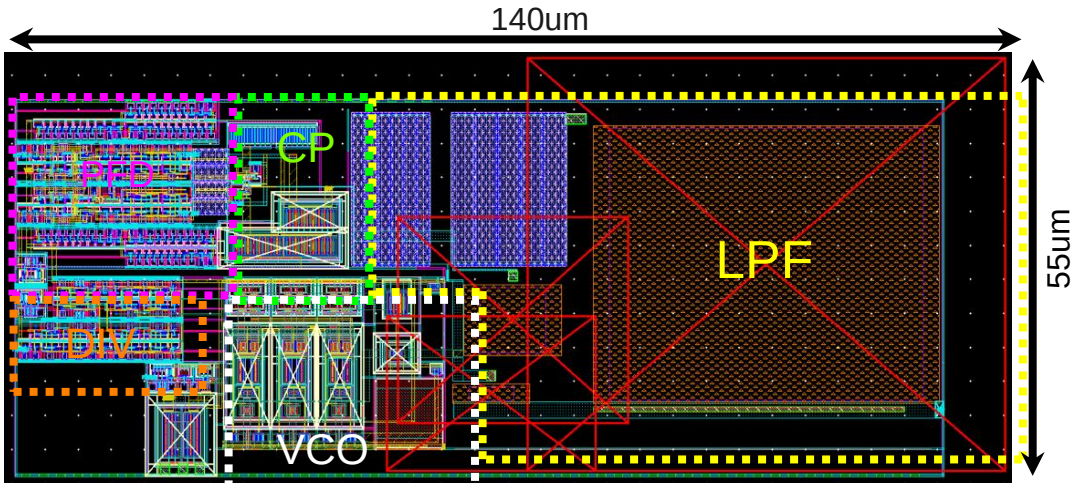


PLL_CML Test Chip,
T. Kishishita

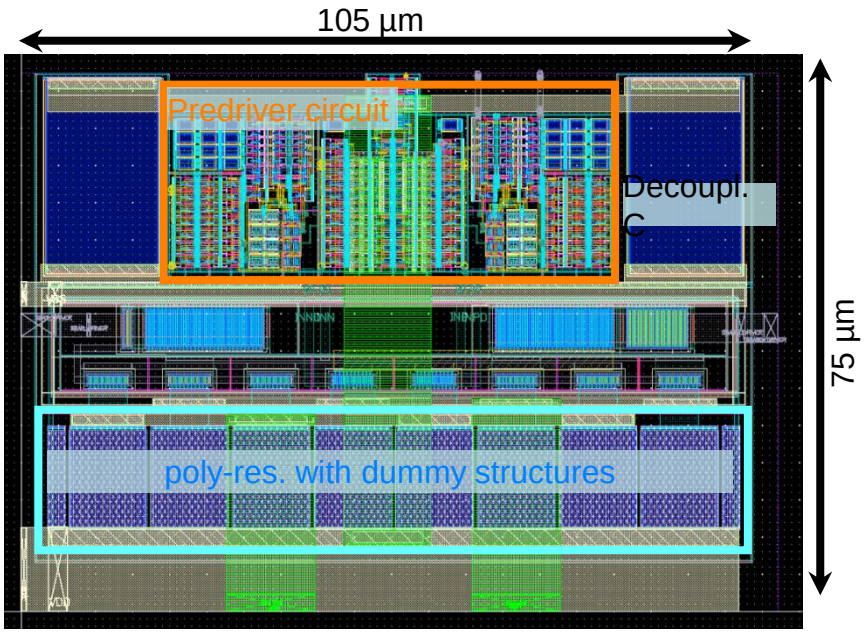


Layouts

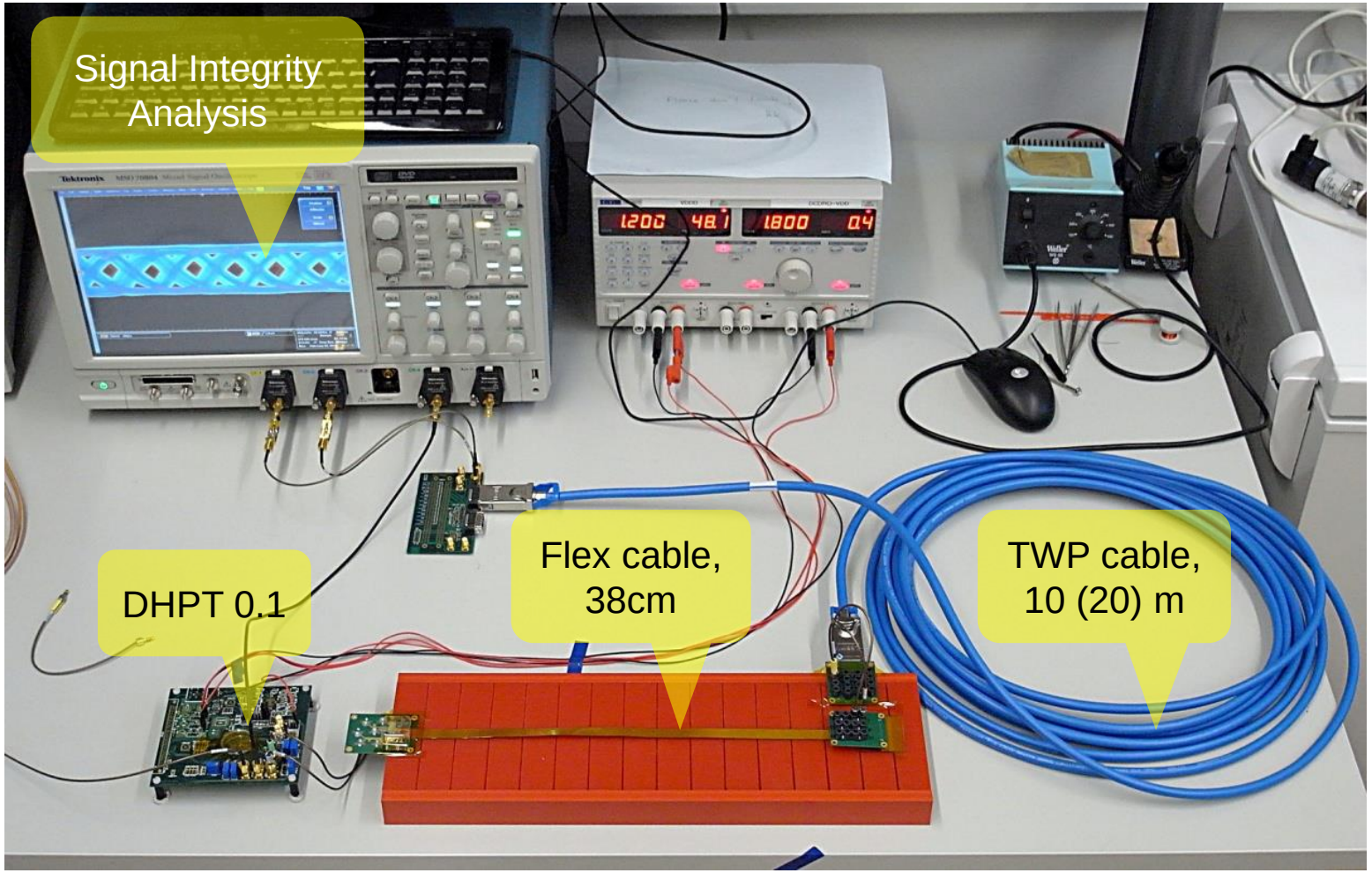
PLL



CML driver

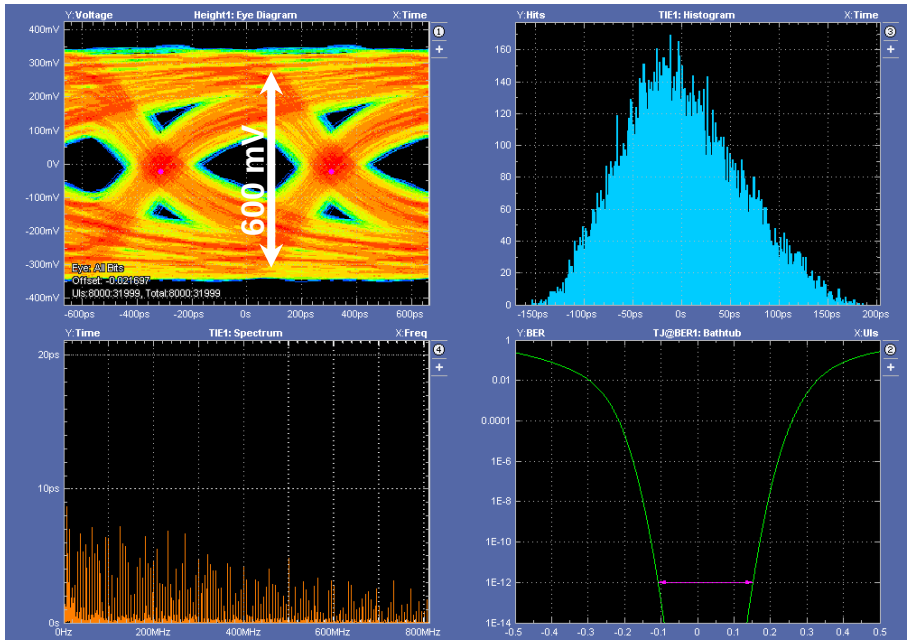


Gbit Link Test Setup

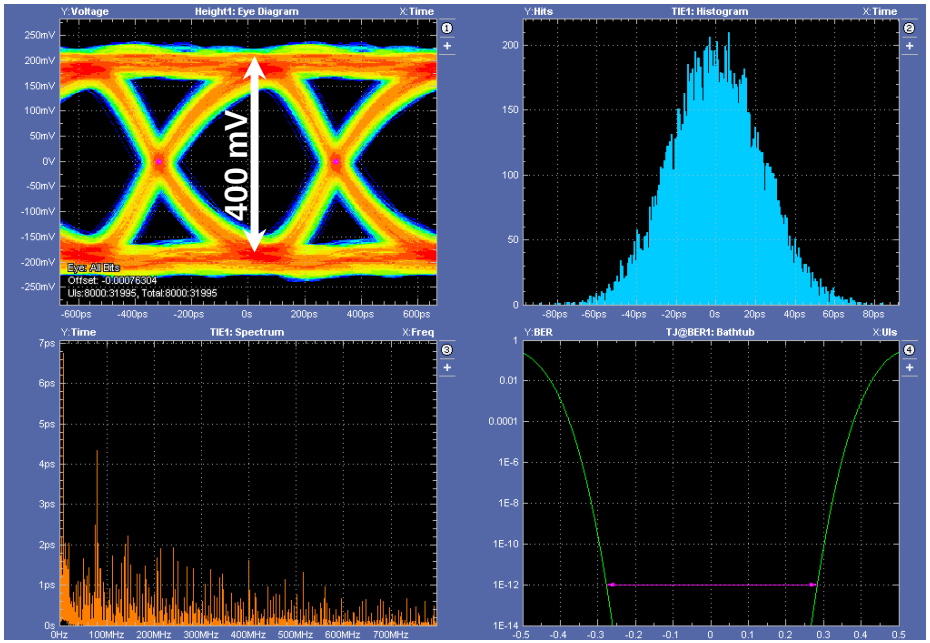


Signal Integrity Analysis

- 1.6 Gbps, 8bit LFSR sequence
- 10m Infiniband cable (LEONI, AWG 26)



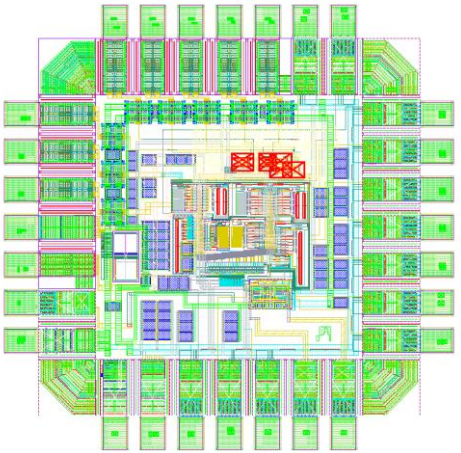
Preemphasis off



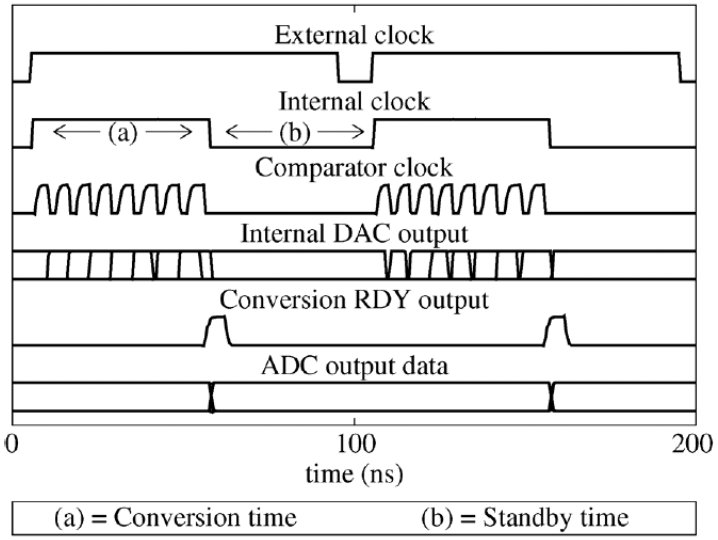
Preemphasis on (600ps, max. I_{boost})

Low Power ADC

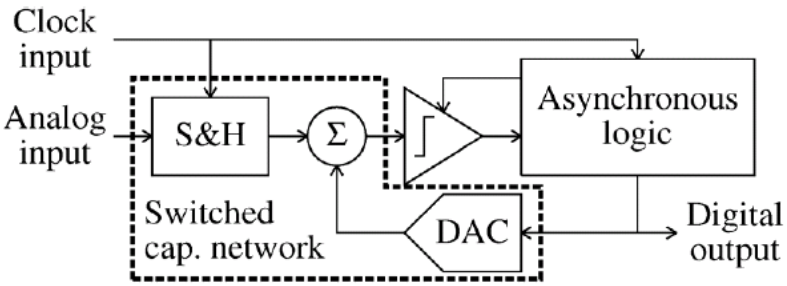
- 8bit ADC
  - 10 Msps
  - Charge redistribution
- Asynchronous operation → low power
  - No clock distribution needed
  - Sample signal triggers digitization sequence
- Serial LVDS data out



T. Hemperek, T. Kisisita



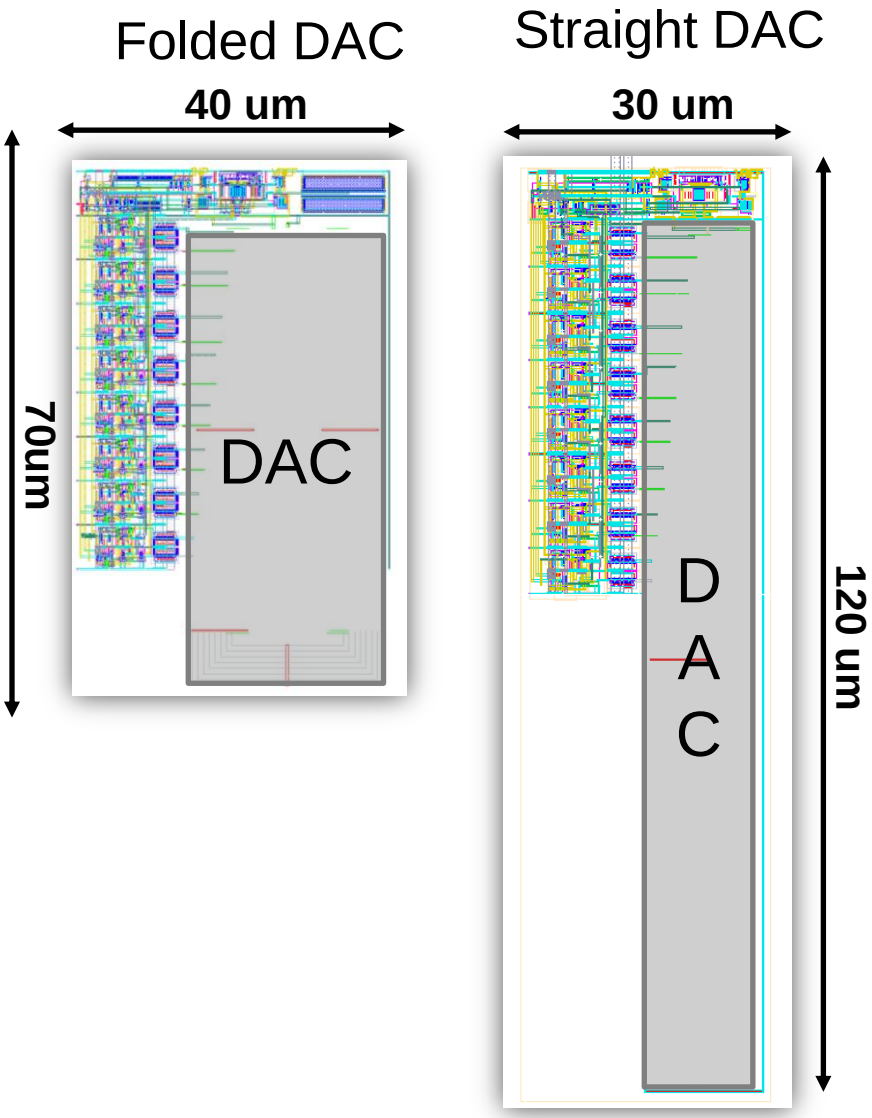
Asynchronous ADC timing



Function Diagram

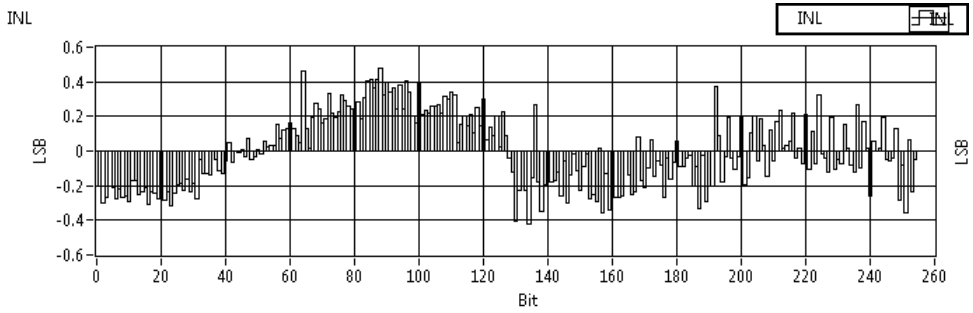
ADC Layout

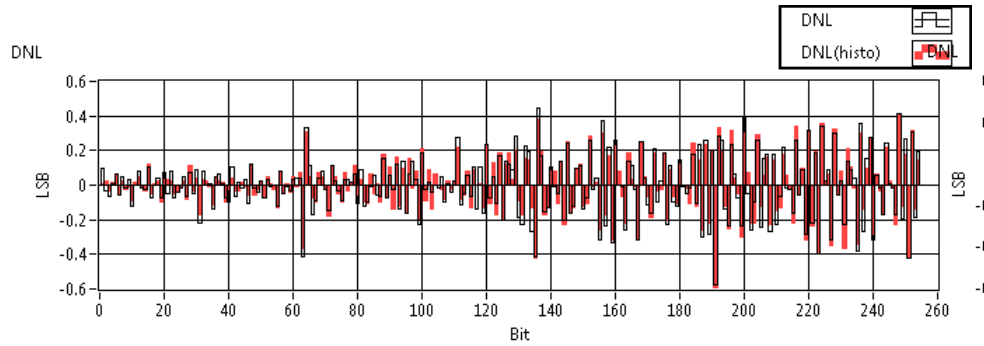
- ADC area dominated by DAC
- Switched capacitor DAC layout critical for DNL performance
- 8 bit ➔ 7 bit: half size



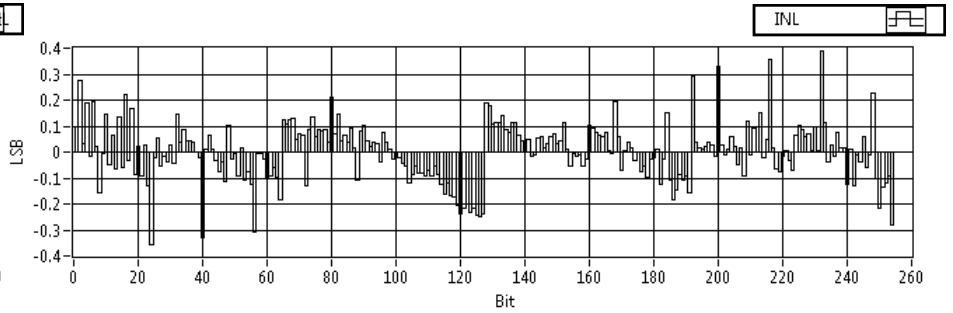
Asynchronous ADC Measurements

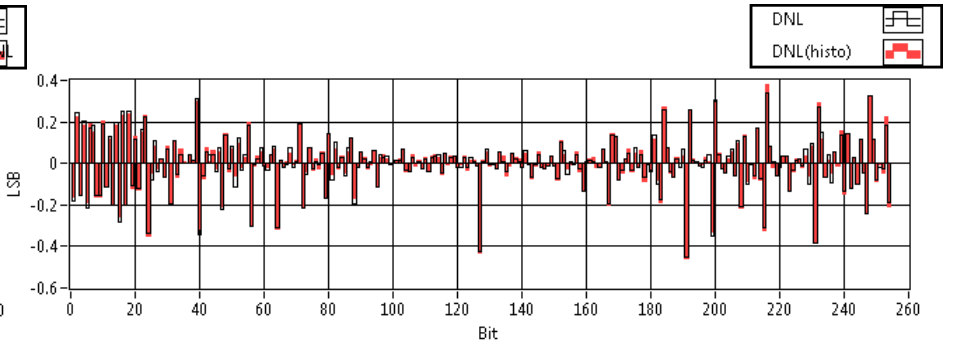
Single Ended Mode





Differential Mode





- Measured at 10 MHz sample rate
- Power consumption: ~40uW
- Works up to 12.5 Msps