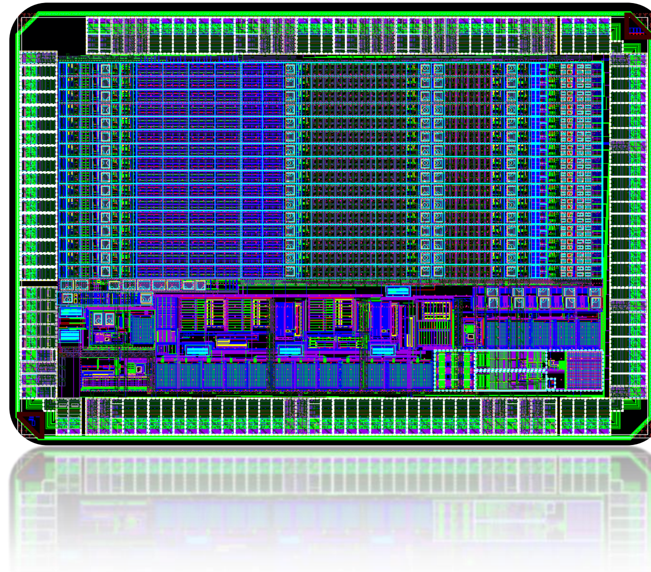
Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

LC-TPC



Front End Electronics
Readout systems for gaseous detectors

The designer point-of view
LCTPC meeting, Bonn, 2014-09-18

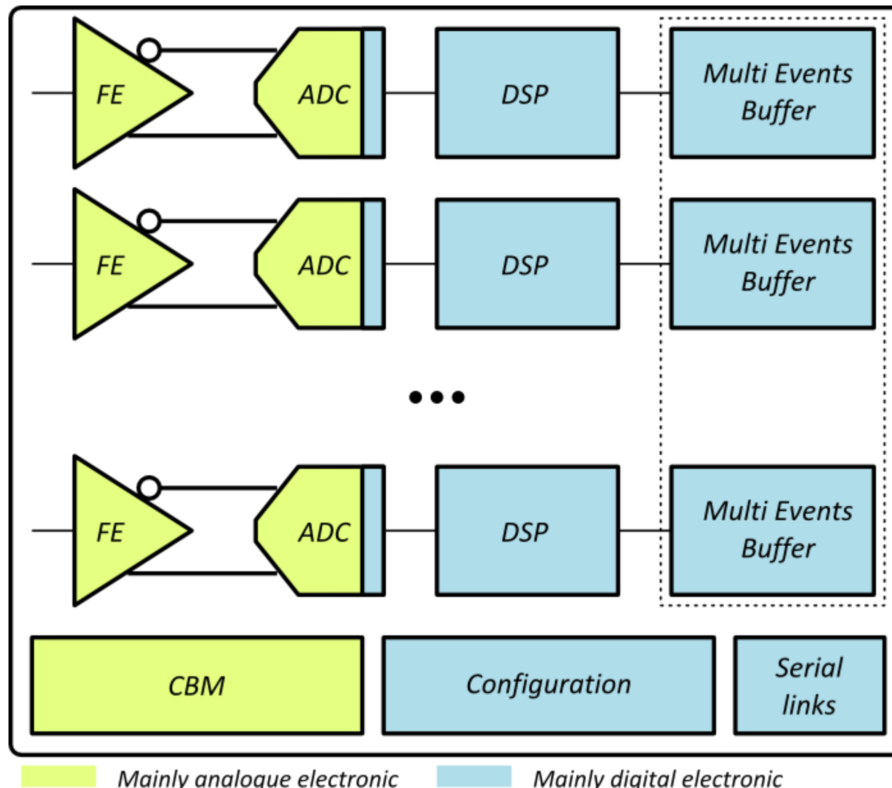
Fabrice Guilloux, CEA Saclay

Outline

- Developments for gaseous detector readout ASIC
  - Present
  - Future
- Optimization : Feedback from a Front End design in IBM 130nm
  - Saltro16
  - Common Front End specification
  - CFE1 ASIC
- New technologies :
  - General tough about deep-submicron technology
  - New integration process

Gazeous detector readout ASIC

- Architecture from SALTRO 16, 2 examples :
  - SAMPA asic for Alice TPC
  - GdSP asic, foreseen first for CMS Muon, could fit also for CMS calorimeter

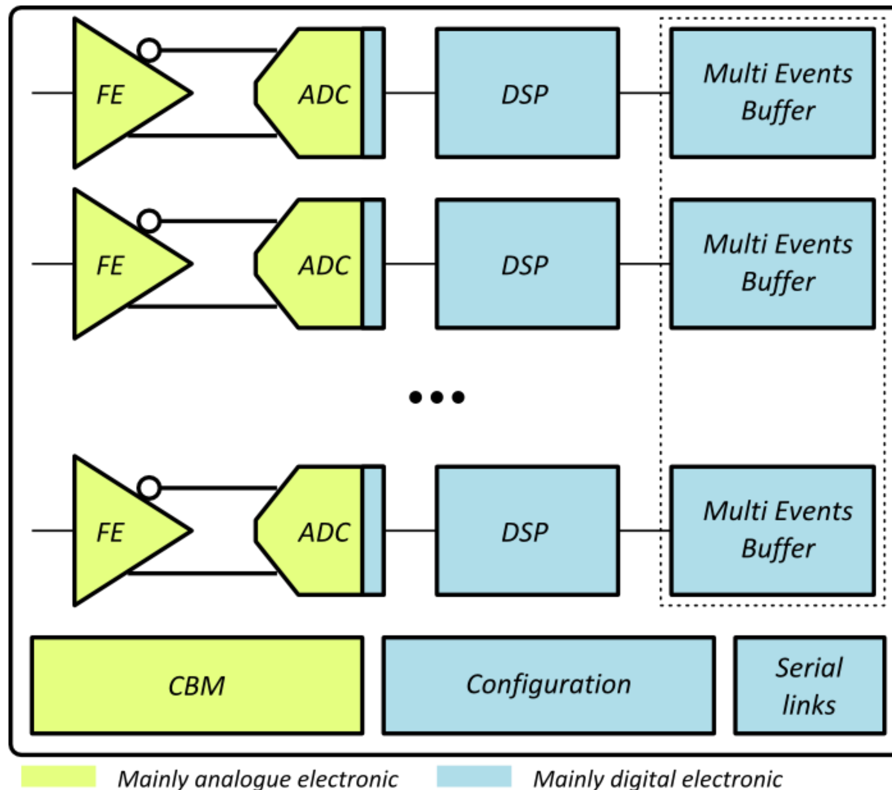


Complete design - for short term production - are in the 130nm node

Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

Gazeous detector readout ASIC

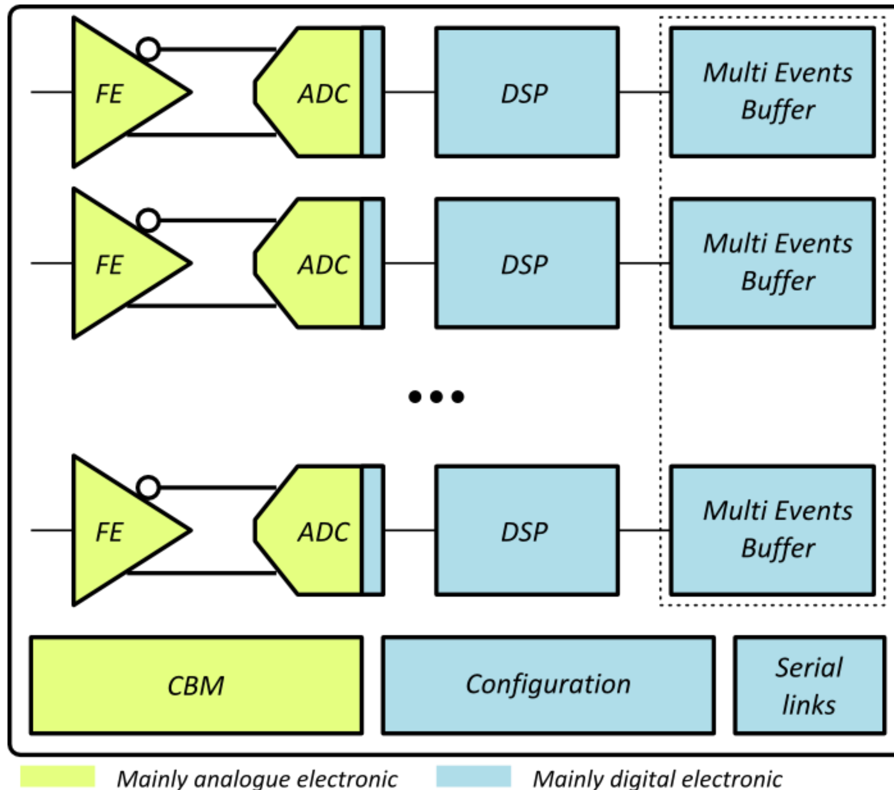
- Architecture from SALTRO 16



- FE : Front End
  - Charge Sensitive Amplifier
  - Transimpedance Amplifier
  - ➔ Noise optimization
- ADC : Analogue to Digital Converter
  - SAR ➔ Low Power
  - Wilkinson ➔ // ADC
- DSP : Digital Signal Processing
- CBM : Calibration Bias and Monitoring
- Serial links :
  - downstream and upstream (i.e. trigger if needed)

Gazeous detector readout ASIC

- After SALTRO 16 ?
  - What is wrong with SALTRO ?



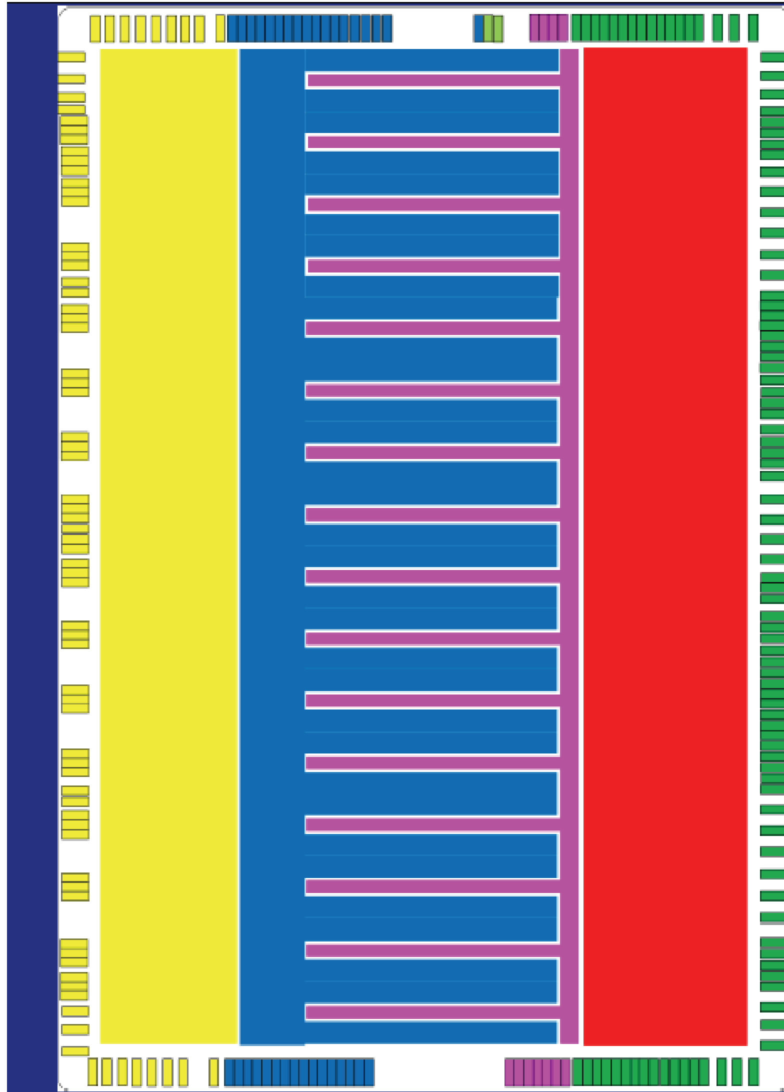
Optimization ?
- Noise
- Power consumption
- Digital filtering
- Digital interface
- Size of Events buffer

→ *Keep current technology*

Above technology limits
- Small ASIC size
- Power consumption

→ *Explore new technology*

SALTRO16



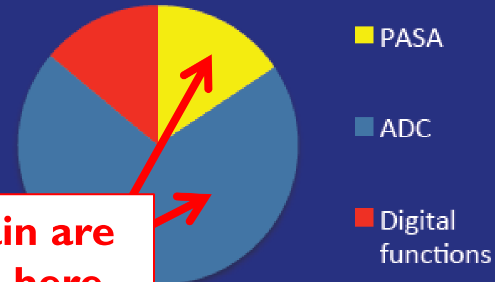
Power domains:

- PASA analog
- ADC analog
- ADC digital
- Digital core
- Digital Pads

PASA ~8mW/ch,
ADC 36mW/ch @40MHz
Digital functions ~114mW
Total power ~ 750mW

Succesful power pulsing operation

Power Distribution for 16 channels



Large gain are possible here

It is clear that the ADC power consumption limits the design to small channels counts.

But times are changing.

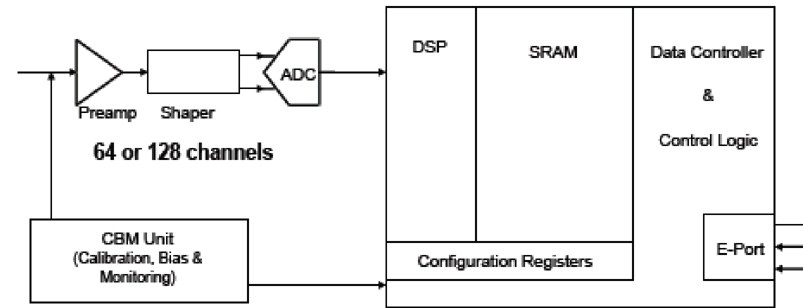
Common Front End

- Join effort to have one ASIC for 2 projects. Or at least large common parts.

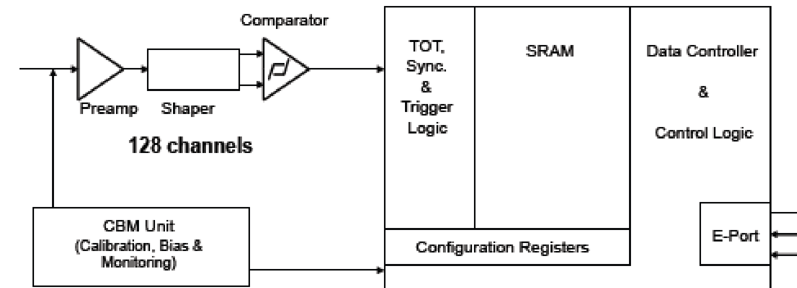
Common front end

- LCTPC (AIDA)
  - specifications derived from SALTRO16 *(slower, low cap)*
- Muon CMS upgrade :
  - First option : VFAT3 ASIC = PSD chip
  - Second option : GdSP ASIC
  - Specifications derived from previous VFAT2 *(faster, high cap)*

GdSP



VFAT3



- Other experiments (Alice Di-Muon …) express their interest
  - "Longer" peaking time
  - "Obsolete" since SAMPA project was launched

FE specifications

Parameter	FE (VFAT3/GdSP)	unit	Remarks
Input capacitance *	5 – 10 -30 – 60 – 80	pF	Simulation cases
Shaper peaking times	25 – 50 – 75 – 100 – 200 – 400	ns	programmable
Shaper order **	3rd order		
Input Leakage current compensation	10	nA	
Sensitivity ***	From 1.25 to 50	mV/fC	programmable
Polarity	dual		
Dynamic range	200 (400 for dimuon)	fC	
Linearity Error : small charges	<1	%	up to 100 fC
Linearity Error : high charges	<5	%	up to 200 fC
Power consumption	**<2**	**mW/chan.**	**Power cycling**
Power supply voltage	1.5	V	
Noise	1100	e-	@ Tpeak = 100 ns @ 2 mW/chan @ Cin = 30pF
Technology	IBM 130nm		

*Design driven for **power** consumption **optimization***

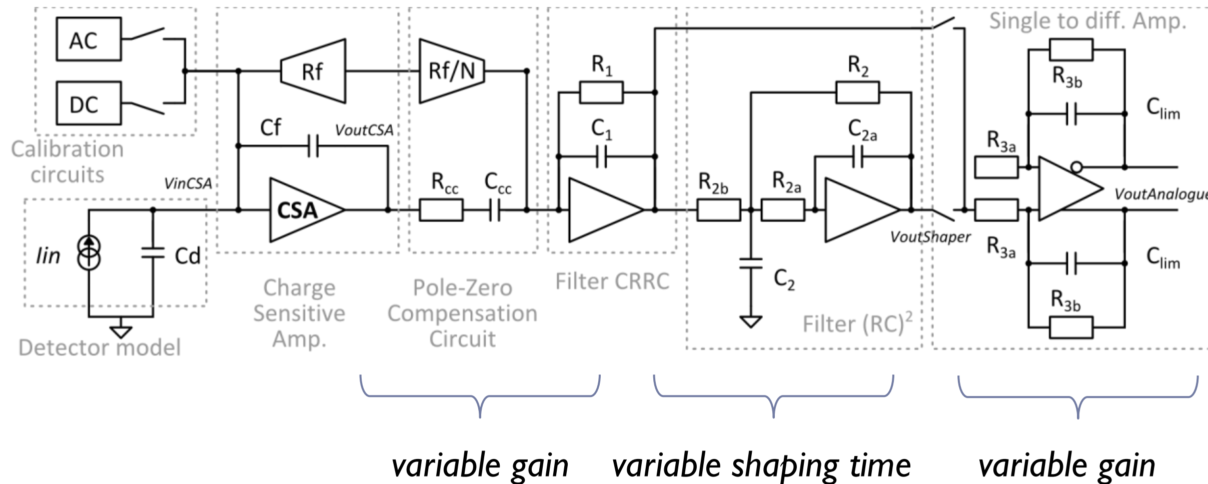
* Stability at 5pF, not all shaping time available (ie. Cd = 80pF and Tp = 25ns)

** 1st order for Tp = 25ns

*** Not all gains available at all peaking times

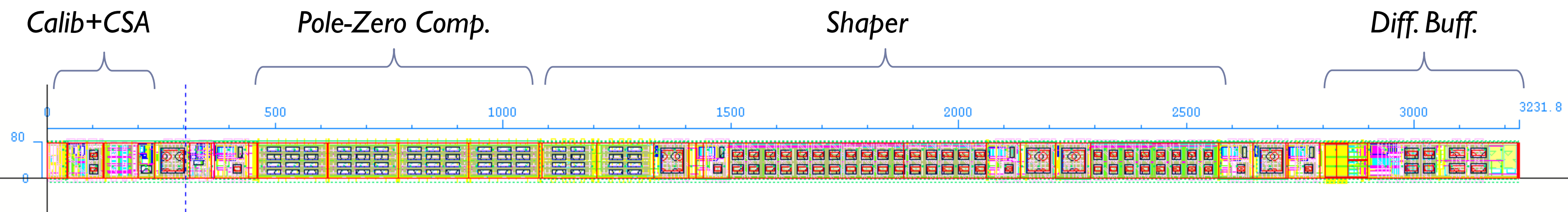
FE architecture

- Technology : IBM 130nm (Power supply 1.5V)
- Architecture :
  - Pre-amp in CSA configuration
  - Shaper : MFB filter
  - Output : Differential buffer



FE architecture

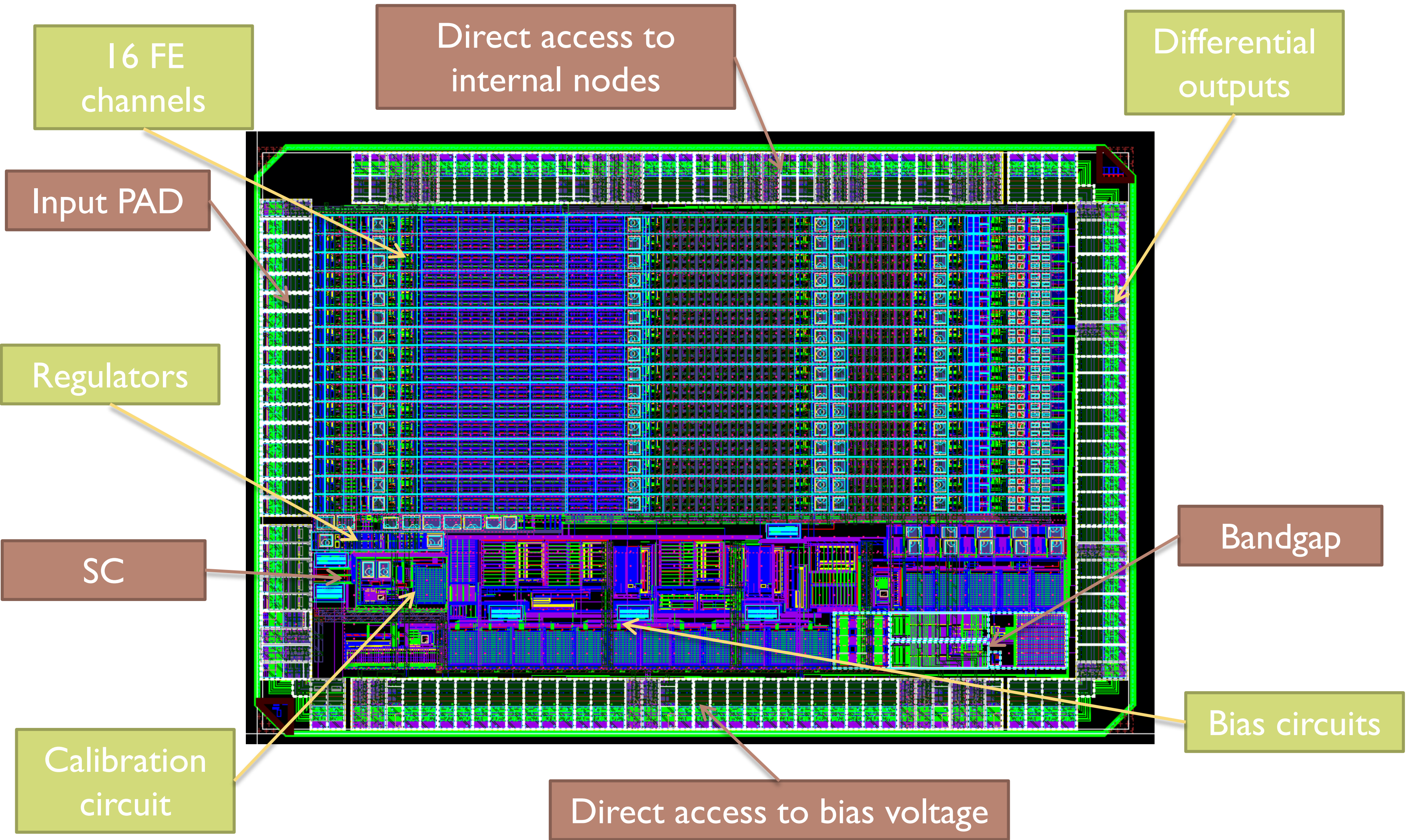
- Architecture :
  - Pre-amp in CSA configuration
  - Shaper : MFB filter
  - Output : Differential buffer



- Height : 80 µm 64 channels ⇔ 5.12 mm
- Width : 3.230 mm

/!\ LCTPC /!\
Impact of technology node on ASIC size
Integration vs Design

CFE1 ASIC



CFE1 simulation results

- Simulations results with :
  - Pad on analogue signals
  - FE : full parasitics

Parameter	AFTER [1]	VFAT2 [2]	SAltro [3]
Technology	AMS 0.35	IBM 0.25	IBM 0.13
Noise	$690e^{-}\oplus 13e^{-}/pF$	$500e^{-}\oplus 40e^{-}/pF$	$650e^{-}\oplus 15e^{-}/pF$
Shaping time	120 ns	22 ns	120 ns
Dynamic range	240 fC	12 fC	150 fC
Input transistor current	800 µA	600 µA	

Input capacitance	Noise (ENC)	Peaking time (ns)	Gain (mV/fC)	
Cd = 10 pF	590	102.2	11.27	
Cd = 30 pF	908	102.3	11.21	
Slope	16 e-/pF	-0.1	0.06	Absolute variation
X_0	431 e-	-0.1 %	0.5 %	Relative variation

Dynamic range : ~ 200fC
Power consumption < 2mW
Noise : 670 e- @ 15pF
Tp = 100ns

[1] P. Baron, "AFTER, an ASIC for the readout of the large T2K time projection chambers," in Nuclear Science Symposium Conference Record, 2007.
[2] P. Aspell, "VFAT2 : A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors," in TWEPP, 2007.
[3] M. De Gaspari, "SAltro 16," [Online]. Available: https://espace.cern.ch/cms-project-GEMElectronics/SAltro%2016/Forms/AllItems.aspx.

CFE1 remarks

- PRO
  - Fit from low input capacitance to "large input" capacitance.
  - Fit from short shaping time to "long" shaping time.
  - Functionalities and programmability.
  - Power consumption.

- Cons
  - Layout could be improve !
    - Height of the channel.
    - MIM cap.
  - Differential buffer. ➔ Design to drive output signal = 2 mW

- The technology issue:
  - Uncertainties on the future of IBM 130nm ?
  - CERN is moving to TSMC technology.
  - CERN is moving to 65nm technology.

New technologies

- Design constrains due to deep-submicron process
  - Power supply voltage reduction
    - Change of architecture need to be **validate**
    - Strong inversion to weak inversion transistor operating point
  - Design rules increase
    - More simulation is needed at layout level to **validate** assess performances (Nwell effects …)
  - Expensive

- Models are not systematically fit to our need
  - Especially noise models need to be **validate**

➔ Trade off between "keeping up to date" and validation process

New technologies

- Integration technology
  - Mixed technology nodes

Advances in Bonding Technologies
(chip to chip, chip to wafer, and wafer to wafer)

Ray Yarema

Workshop on CMOS Active Pixel Sensors
For Particle Tracking

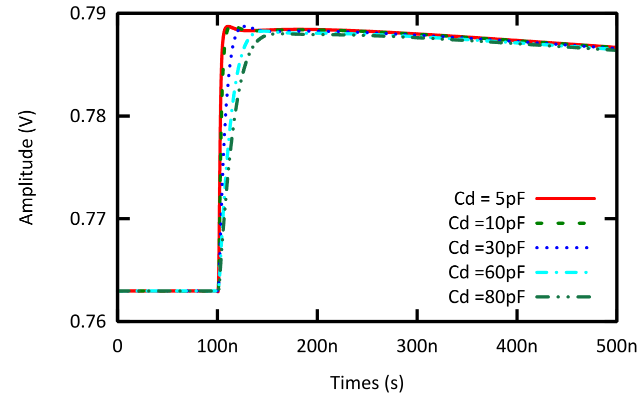
Bonn, Germany
September 15-17 2014

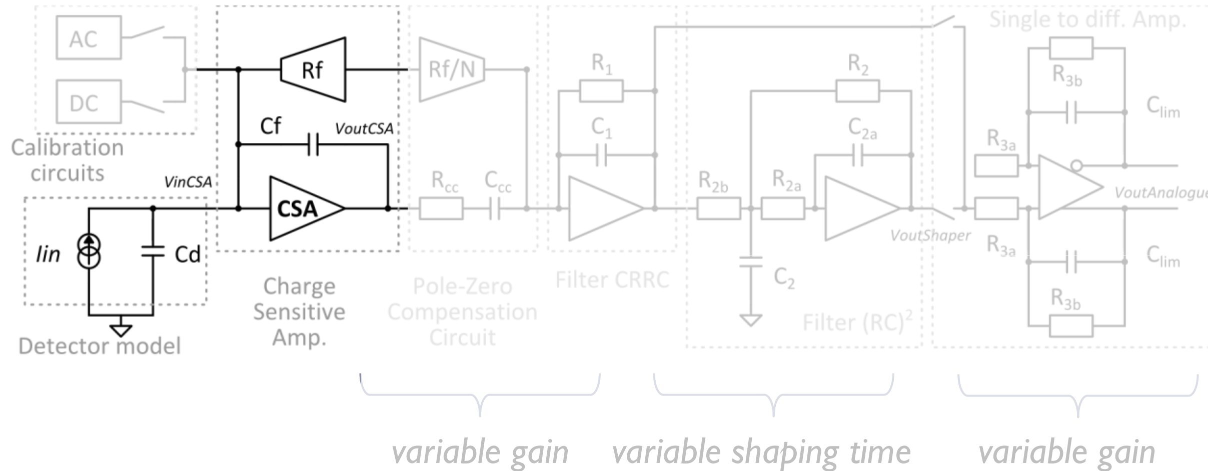
1

- Next slides are backup

FE architecture

- Architecture :
  - Pre-amp in CSA configuration
  - Shaper : MFB filter
  - Output : Differential buffer





FE architecture

- Architecture :
  - Pre-amp in CSA configuration
  - Shaper : MFB filter
  - Output : Differential buffer