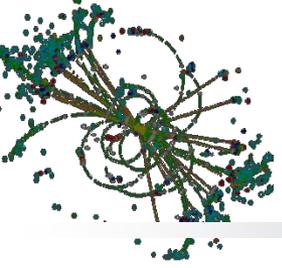


Vertexing for SID status

N. B. Sinev
University of Oregon, Eugene



Outline

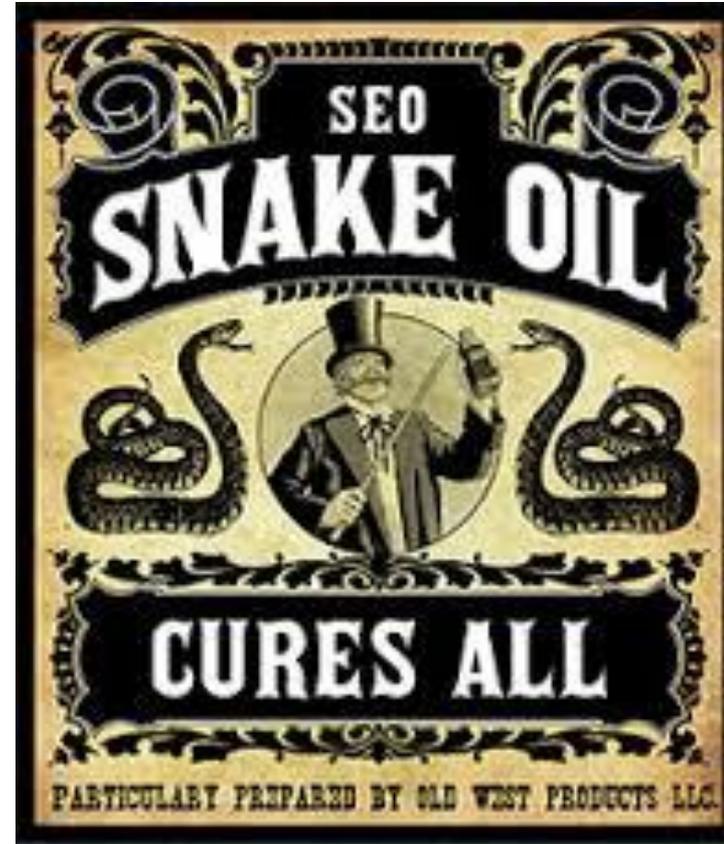


- **Vertexing options**
- **3 D technology status**
- **CMOS sensors (Mimosa like) status and plans**
- **Chronopixel status**
- **Summary**

The 3D Snake Oil

- Low cost, very fine pitch bonding
- Much better power distribution and connectivity
- Radiation hard, thin sensors and readout
- Complex electronics without expensive process nodes
- Separation of analog and digital – lower thresholds
- Lower interconnect capacitance and power
- Tiled, large area devices

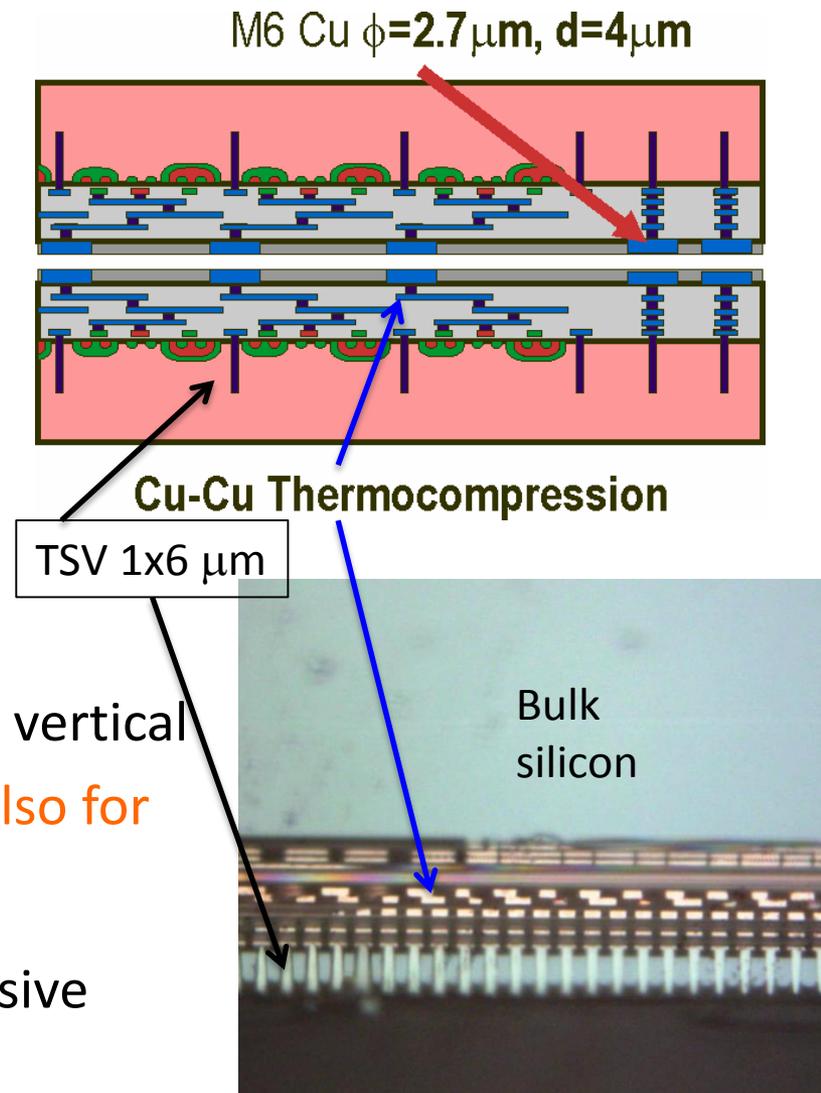
But we are dependent on commercial, large volume development



3D Integrated Circuits

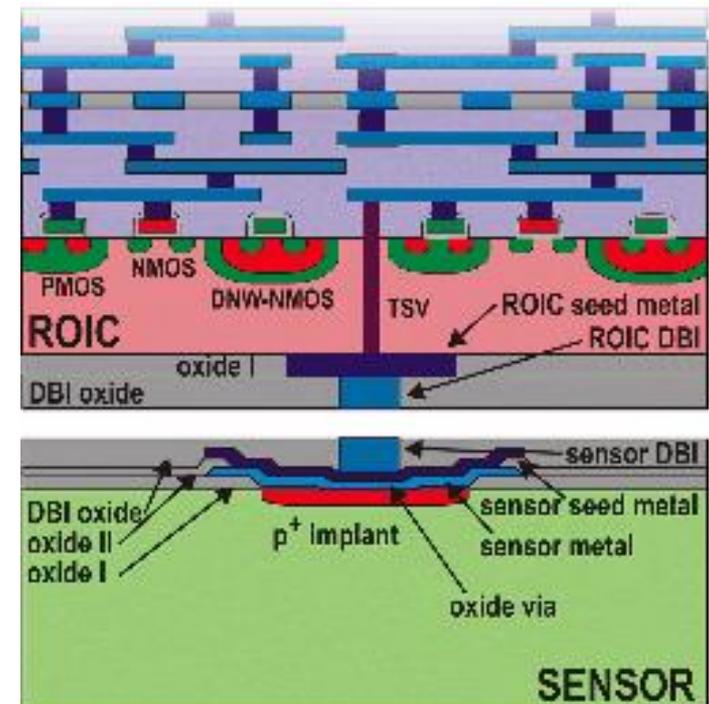
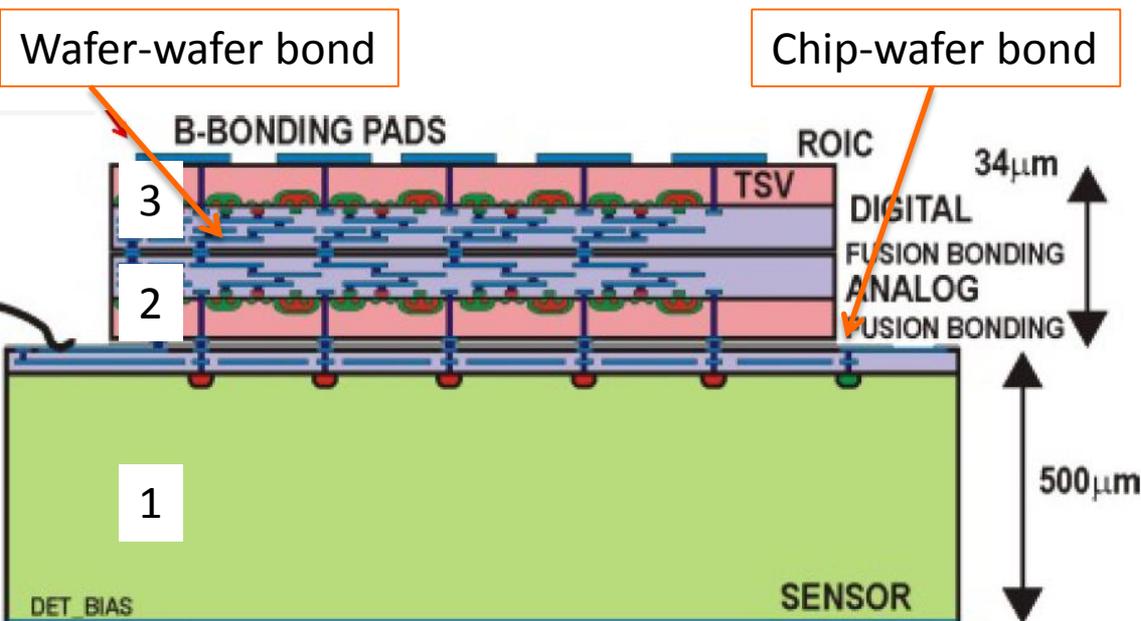
A three-dimensional integrated circuit (3D-IC) structure is composed of two or more layers of active electronic components using horizontal intra-tier and vertical inter-tier connectivity. Component Technologies

- Through Silicon Vias (TSV): small diameter vertical connectivity - **not only to build chips but also for attaching detectors to readouts**
- Bonding: Oxide-, polymer-, metal-, or adhesive
 - Wafer-Wafer, Chip-Wafer or Chip-Chip
- Wafer thinning
- Back-side processing: metallization and patterning



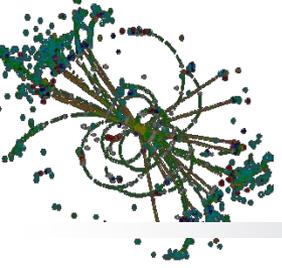
Sensor Integration – Three tier devices

- We then chip-to-wafer oxide (DBI) bonded 3D chips to BNL sensors to form three-tier integrated sensor/electronics assemblies – parts received in March
 - VIP(ILC), VICTR(CMS), and VIPIC(X-Ray) assemblies



Summary

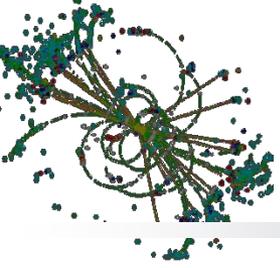
- We are now able to use 3D technology to combine optimal sensors and readout without many of the compromises inherent in other technologies
- We have demonstrated a commercial process for:
 - 3D bonding wafer-wafer bonding and post processing of two layers of commercial 0.13 micron electronics with 4 μ pitch
 - Chip-to-wafer oxide bonding to sensors with 25-80 μ pitch
 - Reduced noise relative to bump bonding
- Now focused on development of VIPIC as a x-ray focal plane
- We are studying the extension of these technologies to large area devices by combining active edge devices with 3D electronics. We now have initial tests on 8" sensor wafers.



CMOS sensors from Strasburg



- **Mark Winters leads efforts in the developing monolithic pixel devices for many years, and they have their sensors already working in many experiments.**
- **Their sensors were relatively slow, having signal integration time of about 100 μs , but remarkably low noise level ($\sim 1\text{-}2\text{ e}$).**
- **Now they are having access to technology with smaller feature size and possibility to create deep p-wells.**
- **They are reducing integration time and adjusting design for use in ILC conditions. Currently they have pixel size $\sim 36 \times 36\ \mu^2$ (which gives point resolution of $\sim 5\ \mu$). They hope to reduce pixel size to $\sim 20\ \mu$ and reduce integration time to few μs . They plan to save time stamps not inside each pixel, but in the external memory, only for hit pixels. This memory will be created in the same monolithic process on the same piece of silicon with pixels.**



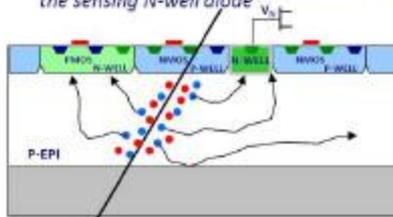
CMOS sensors developed in Strasbourg



CMOS Process Transition : STAR-PXL \rightarrow ALICE-ITS

■ Twin well process: 0.6-0.35 μm

- Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode



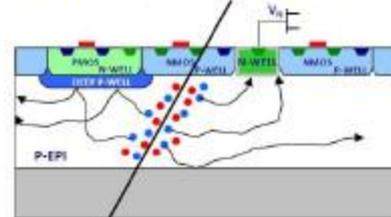
- Limits choice of readout architecture strategy
- Already demonstrate excellent performances
 - STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 μm process
 - $\epsilon_{\text{off}} > 99.5\%$, $\sigma < 4 \mu\text{m}$
 - 1st CPS based VX detector at a collider experiment



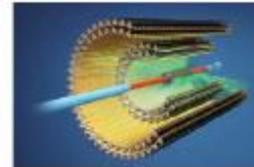
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■ Quadruple well process (deep P-well): 0.18 μm

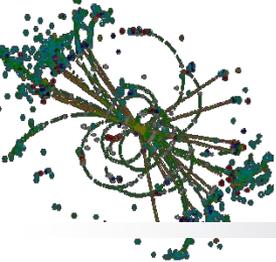
- N-well used to host PMOS transistors is shielded by deep P-well
- Both types of transistors can be used



- Widens choice of readout architecture strategies
 - Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18 μm process (quadruple well)
 - Synchronous Readout R&D:
 - proven architecture = safety
 - Asynchronous Readout R&D: challenging



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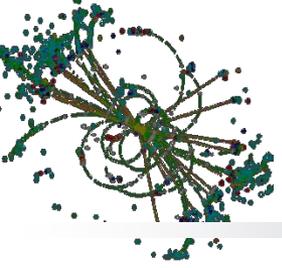
From Mark Winters talk:



SUMMARY & OUTLOOK

- Validation of CPS for high resolution vertex detectors carries on through STAR-PXL data taking campaigns : Preliminary 2014 track reconstruction results confirm high resolution DCA
- Development of CPS for a tracker (ALICE-ITS upgrade) close to final design
 - ↳ uses powerful CMOS process & well suited epitaxial layers ($\gtrsim 20 \mu m$ thick; $\sim 1-8 \text{ k}\Omega \cdot \text{cm}$)
- CMOS process used for ALICE-ITS upgrade allows deriving fast r.o. ($\sim 1 \mu s$) concept for inner layer of an ILC vertex detector \rightarrow Goal : few-bunch (1 ?) tagging while keeping $\sigma_{sp} \sim 3 \mu m$
- Next steps :
 - finalise ALICE-ITS sensor prototyping in 2015
 - ↳ MISTRAL-O submission in June/July
 - start deriving CPS for VXD in 2016/17

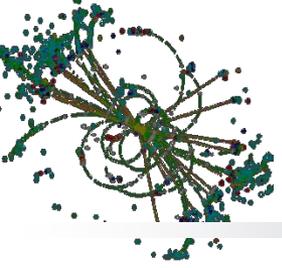
Layer	σ_{sp}	t_{int}
ILD-VXD/In	$< 3/4 \mu m$	30-40/1 μs
ILD-VXD/Out	$\sim 3.5/4 \mu m$	80/120 μs



Chronopixel



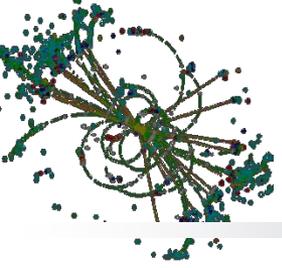
- **Very brief reminder of Chronopixel concept:**
 - ↪ **Chronopixel** is a **monolithic CMOS** pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel, and **record the time** (time stamp) **of each hit**.
- **Summary of prototypes 1 and 2 tests.**
- **Changes for prototype 3**
- **First results of prototype3 tests**
 - ↪ main problem discovered in prototype 2 is **solved** !
 - ↪ noise, calibration, etc.
- **Results discussion**
- **Summary and plans**



Prototype 1 summary



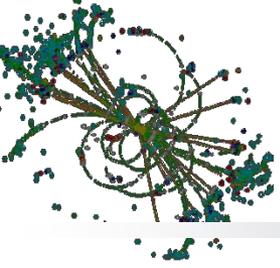
- Tests show that general **concept is working**.
- Noise figure with “soft reset” is within specifications ($0.86 \text{ mV}/35.7 \mu\text{V}/e = 24 \text{ e}$, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is **2.7 times larger** required (250 e).
- Sensors leakage currents ($1.8 \cdot 10^{-8} \text{ A}/\text{cm}^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz .
- No problems with **pulsing analog power**.
- Pixel size was $50 \times 50 \mu\text{m}^2$ while we want $15 \times 15 \mu\text{m}^2$ or less.
- However, CMOS electronics in prototype 1 could allow high charge collection efficiency only if encapsulated in **deep p-well**. This requires **special process, not available for smaller feature size?**
- **Digital comparators offset compensation circuit limited our ability to reach required accuracy**



Prototype 2 features



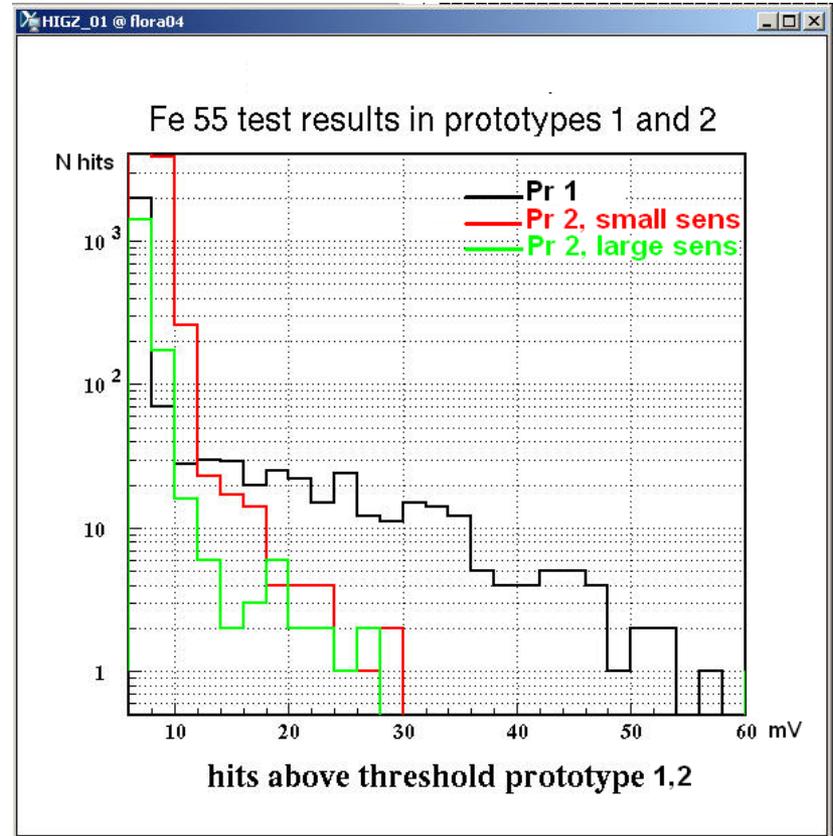
- Design of the next **prototype** was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all **electronics inside pixels** only from **NMOS** transistors. It can allow us to have **100% charge collection without** use of **deep P-well** technology, which is expensive and rare. To reduce all NMOS logics power consumption, **dynamic memory cells design** was proposed by SARNOFF.
- **New** comparator offset compensation (“**calibration**”) scheme was suggested, which **does not have limitation in the range** of the offset voltages it can compensate.
- We agreed **not to implement sparse readout** in prototype 2. It was already successfully tested in prototype 1, however removing it from prototype 2 will save some engineering efforts.
- In September of 2011 Sarnoff suggested to build next prototype on **90 nm** technology, which will allow to reduce pixel size to **25 μ x 25 μ**
- We agreed to have **small fraction** of the electronics **inside pixel** to have **PMOS** transistors. Though it will reduce charge collection efficiency, but will **simplify comparator** design. It is very **difficult** to build good comparator with **low power** consumption on **NMOS only** transistors.

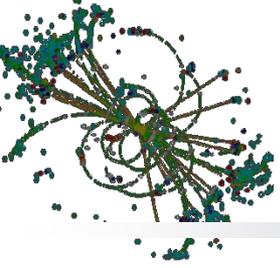


Prototype 2 test results – sensor capacitance

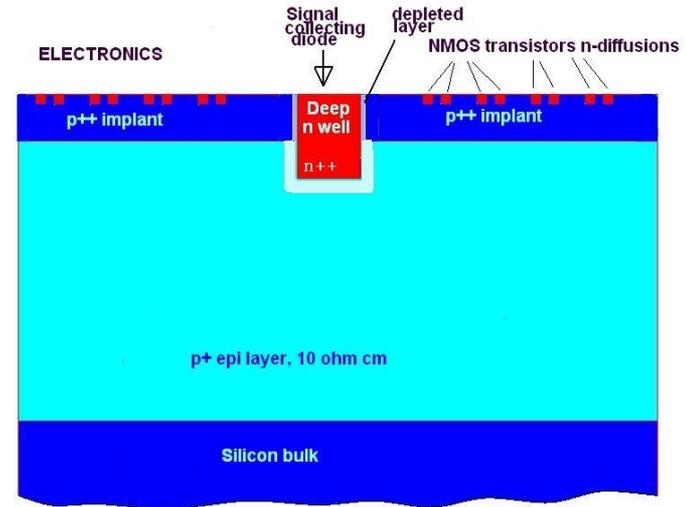
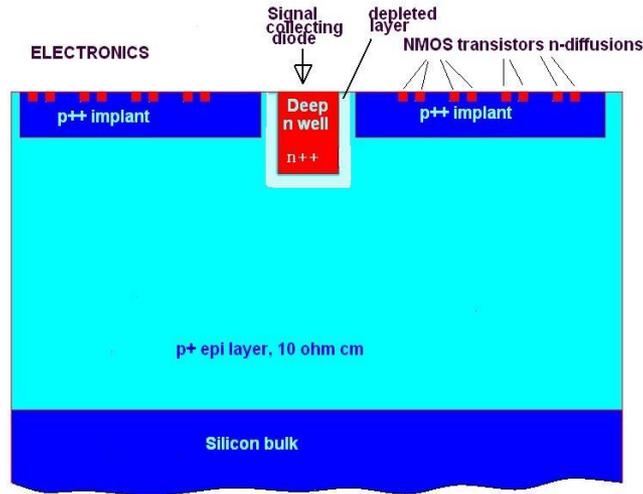


- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Sensor diode size in prototype 1 was $\sim 100 \mu^2$. Prototype 2 has 2 sensor size options – $9 \mu^2$ and $22 \mu^2$ (“small” and “large” on the plot). The maximum signal value is slightly larger for sensor of smaller size, as one would expect, though we would expect larger difference in maximum signal values here. **But capacitance** of the sensor from this measurements (~ 9 fF) appeared **much larger** than our expectation (~ 1 -2 fF).

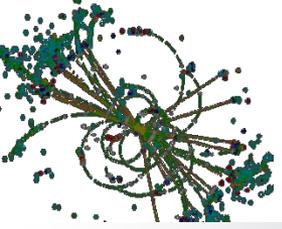




What got wrong?



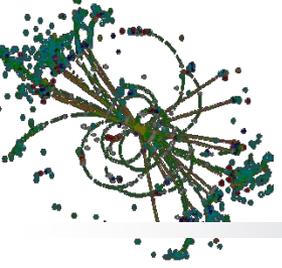
- We **hoped**, that pixel cross-section will look like what is **shown on left** picture. But it appeared, that in 90 nm design rules it is **not allowed** to have window in the top p++ implant **around deep n-well**, which forms our sensor diode. Resulting pixel cross-section is shown on **right** picture. **Very high** doping concentration of p++ implant leads to **very thin depletion layer** around side walls of deep n-well, which creates additional **large capacitance**.



Summary of prototypes 1 and 2 tests



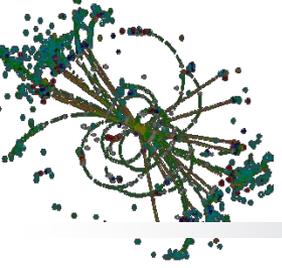
- From both, first and second prototype tests we have learned:
 - ↵ 1. We **can** build pixels which can record **time stamps with 300 ns period** (1 BC interval) - prototype 1
 - ↵ 2. We **can** build readout system, allowing **to read all hit pixels** during interval between bunch trains (by implementing **sparse readout**) - prototype 1
 - ↵ 3. We **can** implement **pulsed power** with 2 ms ON and 200 ms OFF, and this **will not ruin** comparator performance - both prototype 1 and 2
 - ↵ 4. We **can** implement **all NMOS** electronics **without** unacceptable **power consumption** - prototype 2. We **don't know yet** if **all NMOS** electronics is **a good alternative solution** to deep P-well option.
 - ↵ 5. We **can** achieve comparators **offset calibration** with virtually **any required precision** using **analog calibration** circuit.
 - ↵ 6. Going down to **smaller feature size is not as strait forward** process as we thought. Sensor capacitance became an issue, limiting signal/noise ratio. And the **main problem** here seems to stem from 90 nm process **design rules**.



Prototype 3 wish list



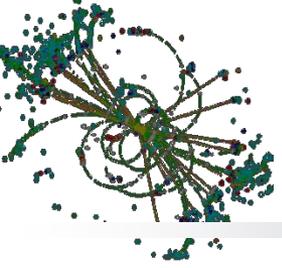
- **Wish list, accepted by Sarnoff for the next prototype:**
 - ↵ **1. Find a way to decrease sensor capacitance** (they think they know how, and their calculations show decrease by factor 10).
 - ↵ **2. Take care about crosstalk** : separate analog and digital power and ground, shield trace, connecting sensor to source follower input from busses, caring strobes and clocks (by changing metal layers designations)
 - ↵ **3. Implement 2-way calibration process**
 - ↵ **4. Remove buffering of sensor reset pulse** inside the chip. It will allow us to **control the amplitude** of this pulse, which is especially important with decreased sensor capacitance.
 - ↵ **5. Remove unnecessary multiplexing of time stamp** (pure technical shortfall of prototype 2 design, which may limit speed and increase feed through noise).
 - ↵ **6. Improve timestamp memory robustness** (right now about 1% of memory cells fail to record time stamps correctly).



Sensor options in prototype 3



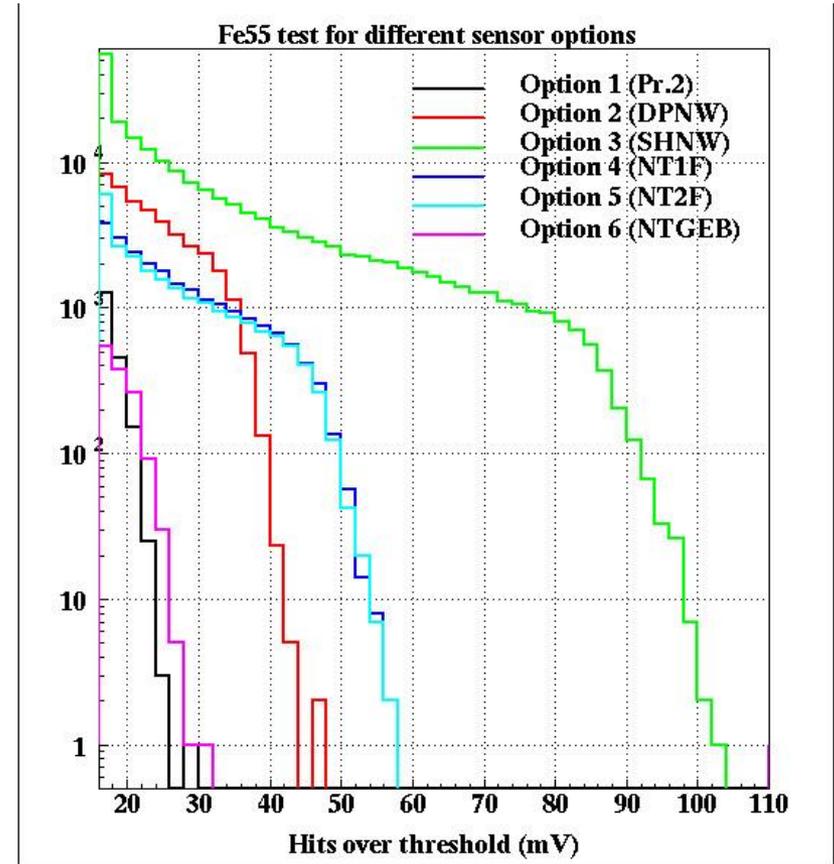
- **6 different** sensor options were implemented on the same chip – **8 column** allocated for each option:
 - ↪ **1** – same as in prototype 2 – for comparison
 - ↪ **2** – deep NWELL diode in the window in P++ layer – this **violate design rules**, but the **waver** for design rules was **accepted** by TSMC
 - ↪ **3** – shallow NWELL diode also in the window – also **violates** design rules, but **waver** was accepted
 - ↪ **4** – “Natural transistor” (NTN) **allowed by design rules** to be in the P++ layer window – transistor is formed **directly on P+ epi layer**. **Large source and drain diffusion areas**, **gate connected to both source and drain** and form sensor output
 - ↪ **5** – also NTN but with **2 fingers**, source and drain are **narrow**, gate **also connected to both**, as in option 4
 - ↪ **6** – same as **5**, however **gate is not** connected to source and drain, but connected to external bias voltage.

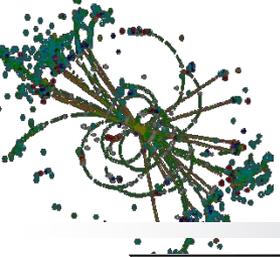


Fe55 test

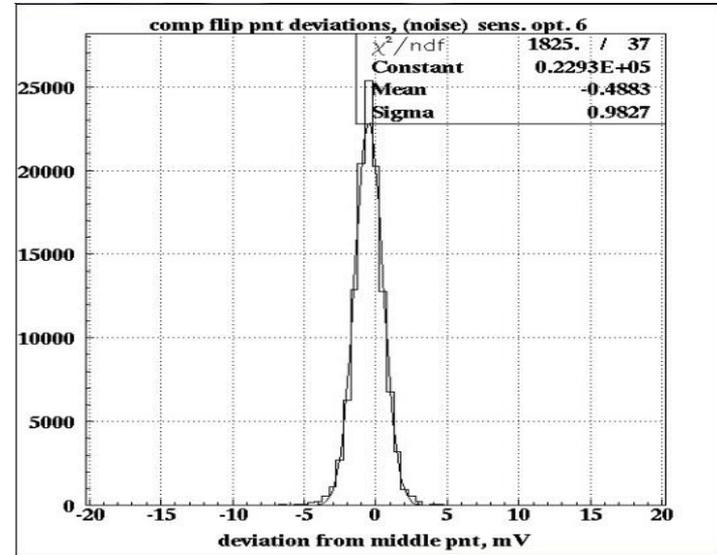
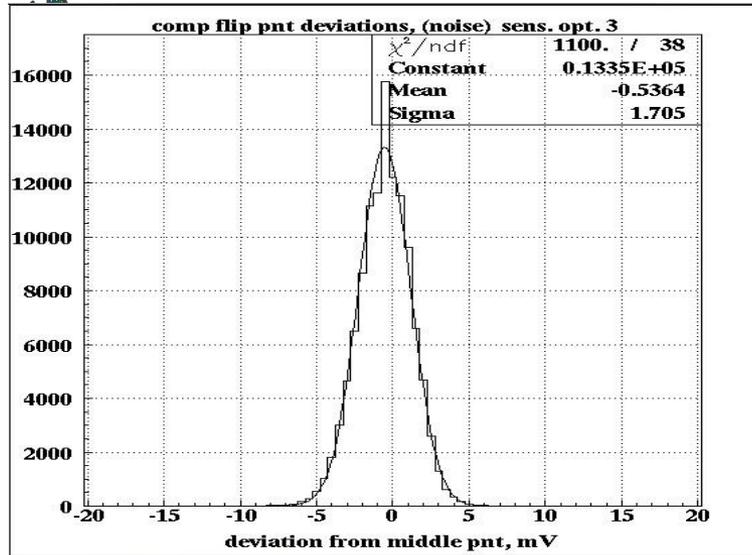


- More precise method of measuring sensor capacitances consist in the observation of signal from radioactive source Fe55. It emits low energy (5.9 KeV) X-rays. Such X-rays are absorbed in the silicon, and all their energy goes into creation of electron-hole pairs. The energy to create one such pair is well known, and is 3.66 eV for Si. So, from maximum observed signal we can calculate capacitance. Taking into account, that Fe55 has about 10% of decays with energy 6.49 KeV, we can get following capacitances:
- Opt. 1 – 9.04 fF, opt 2 – 6.2 fF, opt 3 – 2.73 fF, opt 4 and 5 4.9 fF and option 6 – 8.9 fF

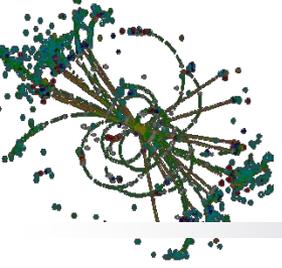




Sensor noise measurements



- Plots above show noise measurements for sensor options with minimum capacitance (option 3, $C=2.73$ fF) on left, and maximum capacitance (option 6, $C=8.9$ fF) on right. Qualitatively they agree with expectation – larger capacitance – smaller noise, but they are larger, than expected from KTC noise formula. That means, that there are additional noise pick up, and table on the next page will give you estimated values of such pick up.



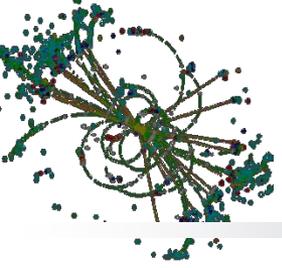
Noise observed vs expected



- **Table at the right shows measured noise values (mV) for different sensor options, and comparison with expected values from KTC noise formula and computed from Fe55 test capacitances. Interesting to notice. that extra noise pick up is largest for smallest capacitance, which is not a surprise, if pick up occurs through capacitive coupling to the sensor. Option 1 seems does not follow this rule – it has largest capacitance, but not smallest pick up. However, it can be understood from the fact, that these pixels are closest to the sensor edge, where most pulsed control signals are formed.**

Option	sigma obs.	sigma exp.	Sqrt ($\delta_{ob}^2 - \delta_{ex}^2$)
1	1.12	0.67	0.9
2	1.08	0.8	0.73
3	1.7	1.21	1.2
4	1.21	0.9	0.8
5	1.23	0.9	0.84
6	0.98	0.67	0.72

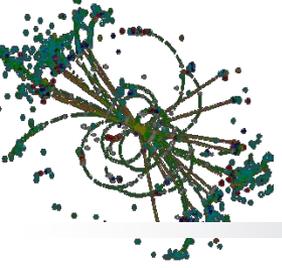
We hoped, that reduction in the photodiode reset pulse amplitude can reduce noise. However, recent tests have shown that it does not help.



Discussion



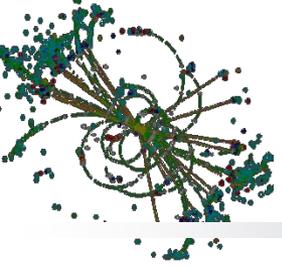
- Looks like **option 3** – shallow diode violating design rule provides best performance – smaller capacitance, larger signal. However, we should remember, that sensor area in that case is only **$2.74 \mu^2$** , while options 4 and 5 – natural transistors – have sensor (n+ diffusion area) **$19.36 \mu^2$** . And sensor **area is important** for charge collection efficiency, because we have competing n-wells in our pixels with total area of **$\sim 13 \mu^2$** . However, there may be another factors here. For example, if small sensor diode sits inside large hole in p++ implant, it is possible, that for most electrons, entered this hole probability to diffuse back and be collected by parasitic NWELLS is much smaller, **than to be collected by diode**, sitting in the hole. However, that depends on how **large is depleted region**, and will not they be **captured by oxide border**.
- In any case, we need much more tests **with minimum ionizing tracks** to find what the charge collection efficiency for different option is. And so far, native transistor option may appear as the best choice.



Summary and plans



- Chronopixel R&D are moving forward, **we have solved many** problems and proved that concept is valid.
- Looks like the problem with large capacitance of sensors in 90 nm technology **is solved!**
- Much more work is needed to fully understand details of sensor operations. We **absolutely need** to measure sensor efficiency for minimum ionizing particles.
- Cross talk issues **were addressed** in prototype 3 by separating analog and digital powers and putting small decoupling capacitors into each pixel. However, we still **see some effect of cross talks**. It is not a show-stopper, as effect is relatively small, but we need to think about minimizing it.
- Future plans depend on funding and test results. If we confirm acceptable charge collection efficiency for one of the options in prototype 3 and have enough money, next step will be making working size prototype (~1x1 cm). If efficiency appears not good enough, we need to bust signal by either increasing epi resistivity or thickness, or both.



Vertex technology readiness



- **We see, that 3 D technology reaches production readiness soon.**
- **Another option – CMOS sensors – should be ready in 2017**
- **Chronopixel looks like solved major problems, but still needs at least one more prototype of real size sensor.**
- **We certainly will have mature sensor technology before SiD detector construction starts**