



Report from CALICE DAQ Task Force

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CALICE DAQ Task Force

- Experts' meeting discussing common DAQ
- Members
 - Silicon: R. Cornat, F. Magniette, T. Suehara
 - Scintillator: J. Kvasnicka, M. Reinecke
 - Semi-digital HCAL: L. Mirabito, C. Combaret
- 2 years of mandate
- ~ 1 meeting per month
 - 4 meetings held

Targets

- Common DAQ
 - Common clock and acquisition cycle (AC)
 - Synchronized data taking and event matching
 - Common run control
 - Interface to upper control (TLU?)
- Combined testbeam
- Minimize total work by sharing tasks

Past meetings

1. 10 Dec 2014

- Task overview
- Select coordinator

2. 19 Jan 2015

- Overview each subsystem

3. 4 Mar 2015

- Discussion on clock

4. 10 Apr 2015 (wo/ Si experts)

- Discussion on BX, Acq#, Run, Timestamp etc.

Indico

<https://agenda.linearcollider.org/category/156/>

Public

CALICE DAQ Task Force







Tuesday, 7 April 2015 from 15:00 to 16:30 (Europe/Zurich)

Manage ▾

Description Video room:

<https://vidyoportal.cern.ch/flex.html?roomdirect.html&key=ERLczis1pbQLtvCUW1Sb4d40Xk>

Tuesday, 7 April 2015

- | | |
|---------------|---|
| 15:00 - 15:10 | SiECAL news 10' ▾
Speakers: Dr. Taikan Suehara (Kyushu University), Dr. Remi Jean Noel Cornat (CNRS/IN2P3/Laboratoire Leprince-Ringuet (LLR)), Dr. Frédéric Magniette (LLR, CNRS) |
| 15:10 - 15:20 | AHCAL/ScECAL news 10' ▾
Speakers: Mr. Jiri Kvasnicka (Institute of Physics, ASCR), Jiri Kvasnicka (Acad. of Sciences of the Czech Rep. (CZ)), Mr. Mathias Reinecke (DESY)
Material: Slides   |
| 15:20 - 15:30 | SDHCAL news 10' ▾
Speakers: Laurent Mirabito (Institut de Physique Nucleaire de Lyon (IPNL)-Universite Claude), Mr. Christophe Combaret (IPNL)
Material: Slides   |
| 15:30 - 16:30 | Discussion - Clock, Run/Readout no, Busy etc. 1h0' ▾
Speaker: Dr. Taikan Suehara (Kyushu University)
Material: Slides   |

Master clock

- 'Master CCC' will provide clocks to each CCC
- 5 MHz is the basic clock corresponding to BX (or go into the real ILC BX period??)
- Need 50 MHz for Silicon because no PLL in Si-CCC (maybe done in master CCC)
- Scintillator and SDHCAL can produce their clock from the master clock
- Clock will be communicated via either HDMI or LEMO

Synchronization (Tentative)

- BX synchronization
 - Each detector has different inactive time after the start_acq
 - **Master CCC sends start_acq**
(via either fast command or LEMO)
with configurable delay (set by PC)
to each port to synchronize livetime of each
- Busy
 - Treated by Master CCC to determine stop_acq and next start_acq
 - Should be sent from each subsystem

Synchronization (2) (Tentative)

- Acquisition cycle (or readout cycle)
 - Use AC counter from each subsystem to check the synchronization
 - Start from 0 at each run
 - Cross-check of 'Spill' sync by time-stamping (at lowest possible level of each subsystem)
- Run
 - Common run number notation: XXXYYYYY, XXX is the common TB number
 - No limit for the run length
typical run period should be O(1h) - O(1d)

Who provides 'Master-CCC'?

- Scintillator
 - Zedboard with Xilinx Zync (FPGA + ARM CPU) (commercial, ~300 EUR/board)
 - + Mezzanine (can be provided by DESY/Mainz)
 - Firmware is in active development (DESY / Mainz? / possibly Kyushu?)
- SDHCAL
 - No manpower
- Silicon
 - ?

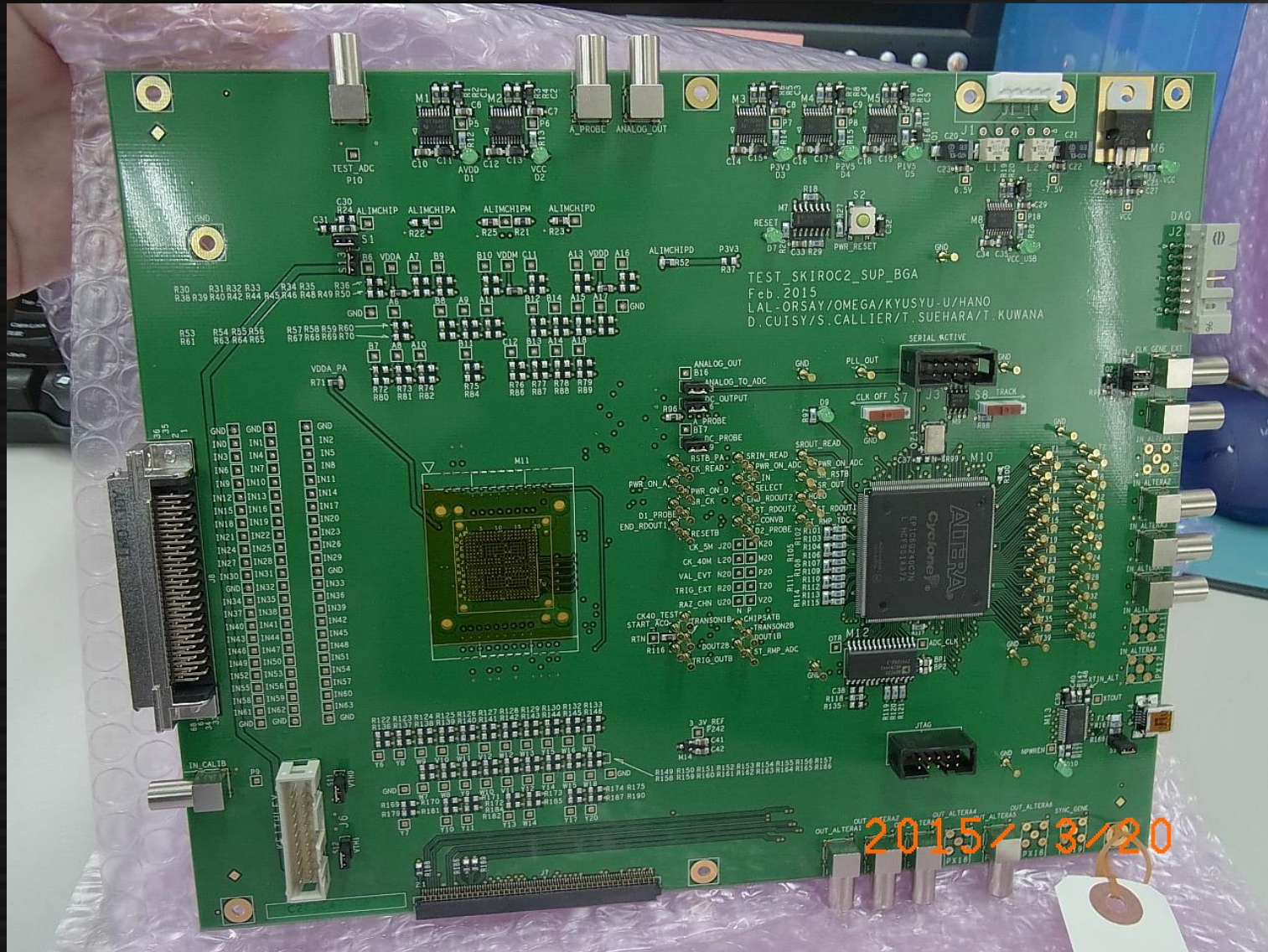
Software

- No discussion yet
- EUDAQ
- LCIO
- etc.

Current priority to specify baseline design of hardware of common DAQ

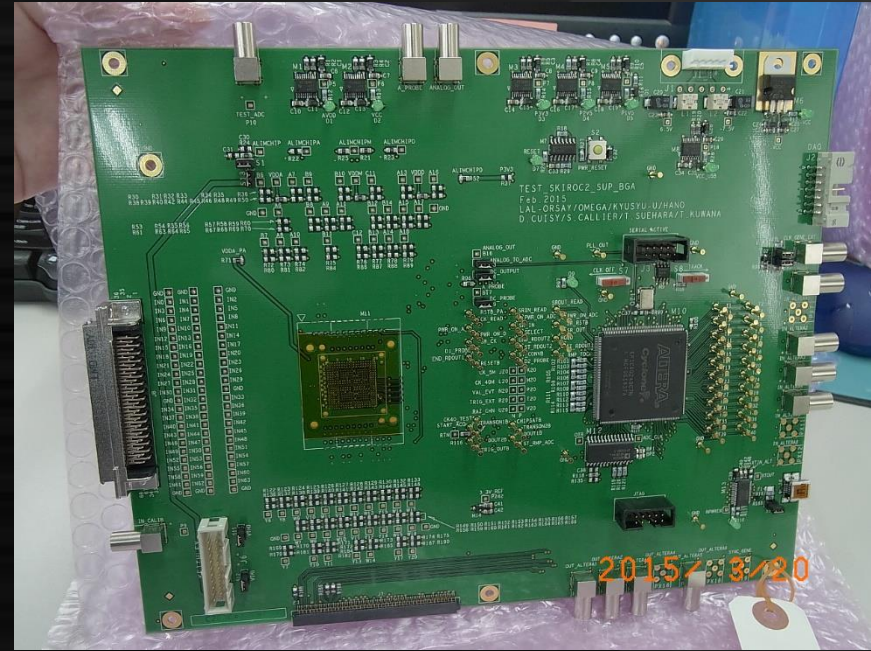
A few word about recent Kyushu activity

SKIROC2 BGA testboard



SKIROC2 BGA testboard

- Delivered at March
 - Two boards on 1st batch one is in modification
- Based on OMEGA TB
 - QFP → BGA
 - Two kind of sockets Ironwood & SER (jp)
 - Connector for sensor
- Two interface
 - Readout by OMEGA FPGA (worked last Friday!)
 - Readout by Silicon DIF (not tested yet)



DAQ activity plans in Kyushu

- Testbeam analysis (H. Hirai's talk)
- Investigate various characteristics of BGA SKIROC with the testboard
- FEB11 production (in plan)
- Combined DAQ
- Online monitor
- Automatic test of sensor/electronics
 - Laser, RI (for crosstalk, gain etc.)
- ...