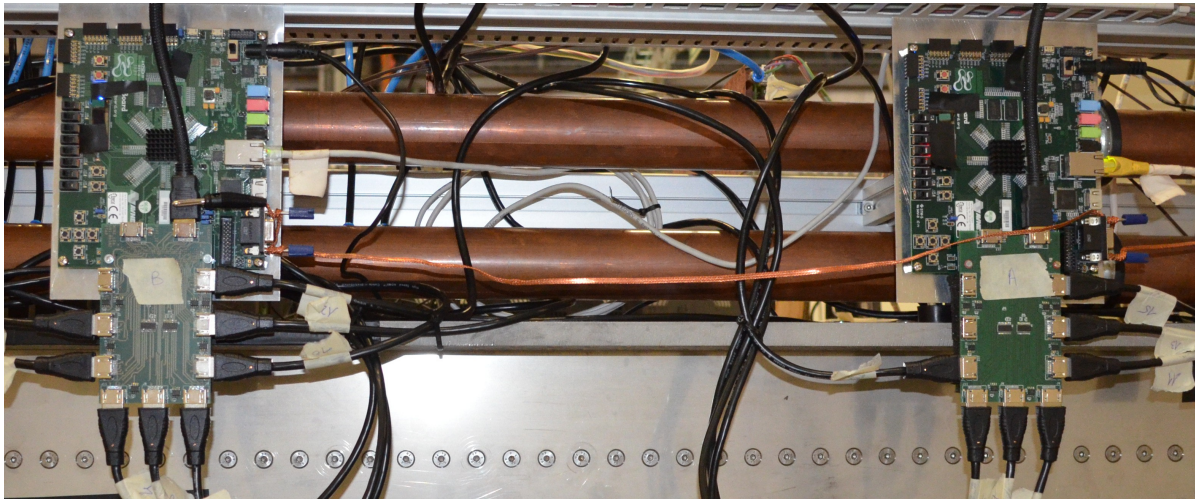
ScCAL Data Acquisition System

Hardware insight

- DIF modifications
- LDA implementation
- Common running timing
- Timing + upgrade scenarios
- Beam interface (BIF)
- Plans



© Picture Ali

Jiri Kvasnicka

CALICE AHCAL main meeting combined with electronics and DAQ
DESY HH, 16.12.2014

Calorimeter for ILC

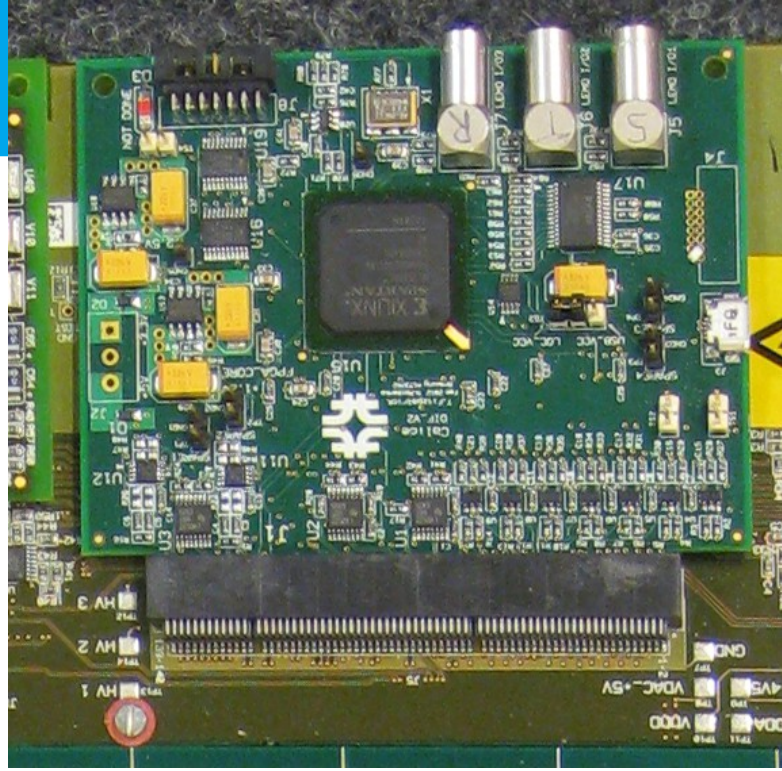
HELMHOLTZ ASSOCIATION

Universität Hamburg

Fyzikální ústav Akademie věd ČR, v. v. i.

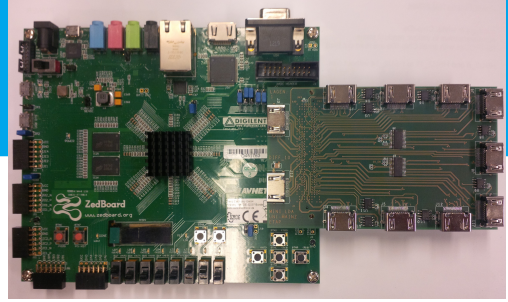
DESY

DIF Modifications (firmware)

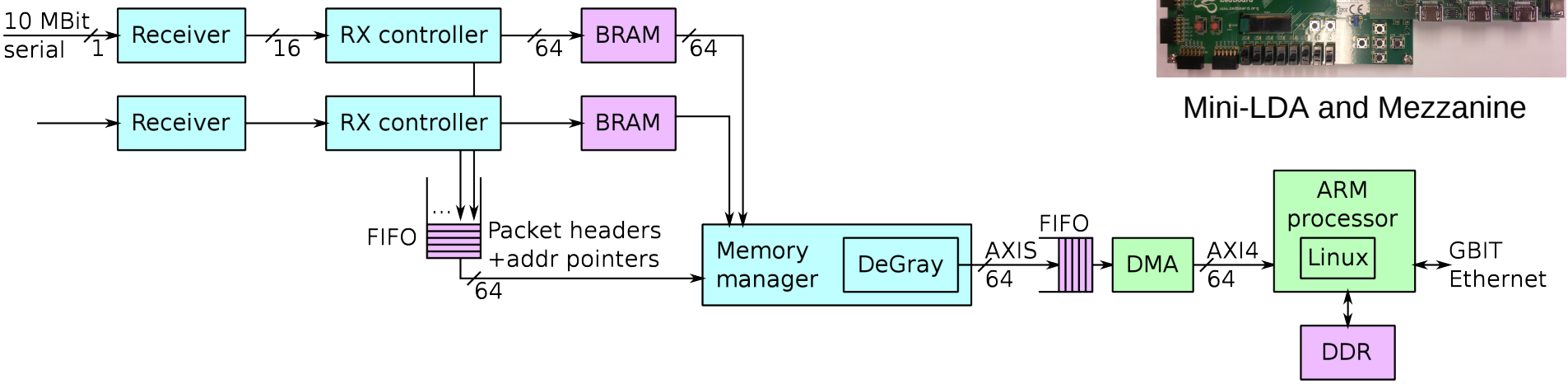


- LVDS repeaters (covered by Mathias)
- Switched to HDMI
  - Links at 10 Mbit/s, UART-like (1 start bit, 16 bit data, 2 stop bits). Oversampled by 40MHz in reception
  - Dynamic switch between USB and HDMI – both interfaces can be used simultaneously
  - HDMI readout speed up by factor ~2.5 (omit delays in USB FTDI handshakes) => reaching 10Mbit/s
- Dynamic master clock selection (40 MHz)
- HDMI derived clock (5 MHz) synchronization
- No start on sill signal anymore => use Fast Commands (FC)
- **Start of acquisition**: upon Fast Command receive
- **Stop of acquisition**: RAM full / timeout / stop FC receive
- **Start of data transfer** (ASIC → DIF, DIF → LDA): upon slow command
- Bugs fixed (i.e. 13 memory cells, packet lengths)
- Now 2 persons are able to make DIF modifications (Frantisek and Jiri)

LDA Architecture 1 (DIF → AXI-stream)



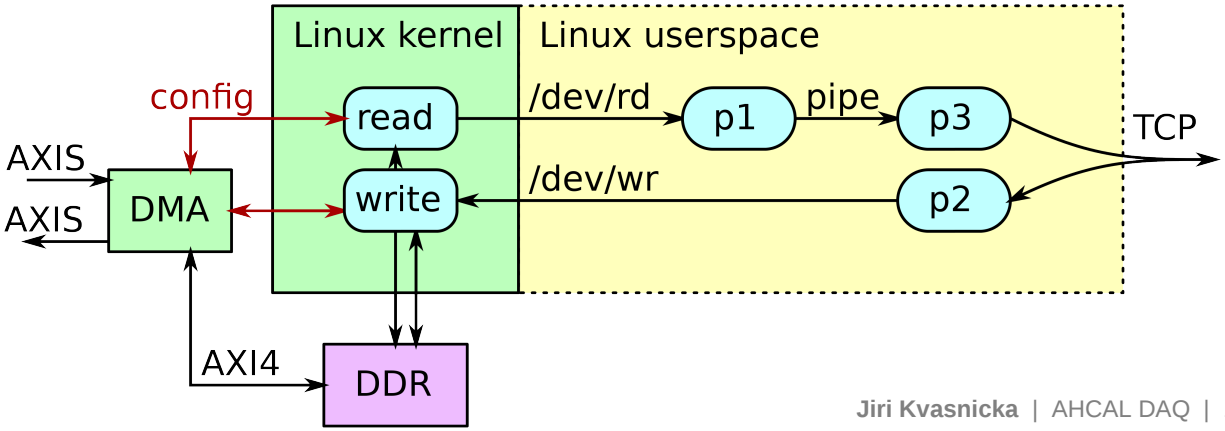
Mini-LDA and Mezzanine



- 40MHz internal operation
- Each port has enough memory to hold complete layer data
- Small packets are merged In the “ASIC” readout packets
- Packet pointer is sent to the queue
- Memory manager collects all packets according to the pointers, decodes them and sends the to a large FIFO already on AXI-Stream bus
- Xilinx DMA core controls the transfer to the main memory

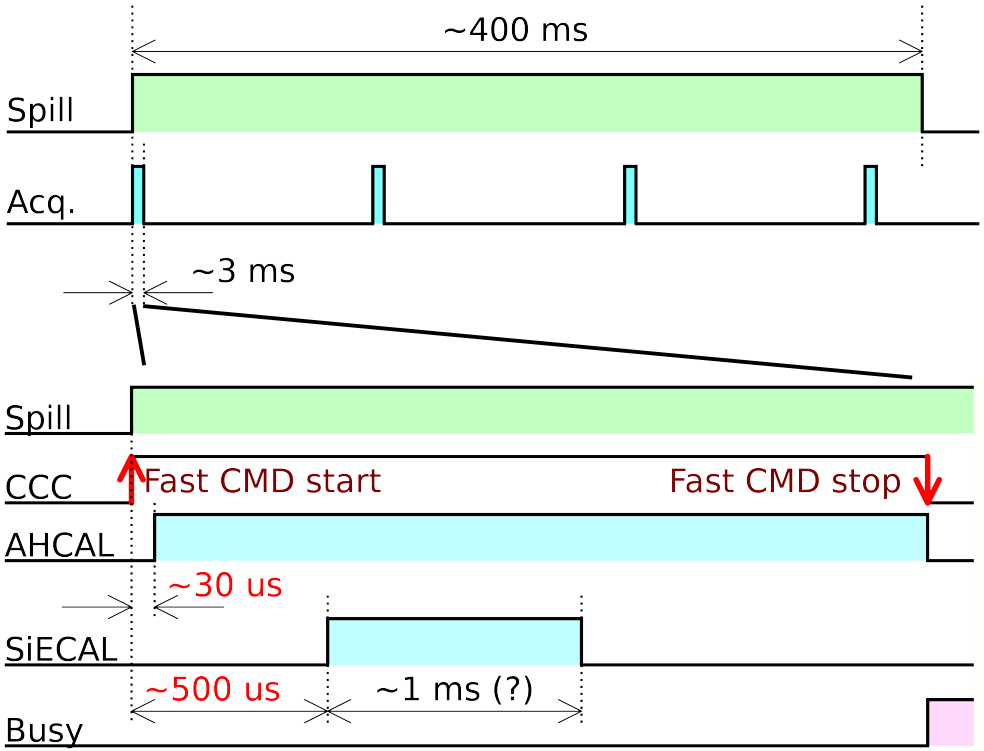
LDA Architecture 2 (AXI-stream → TCP)

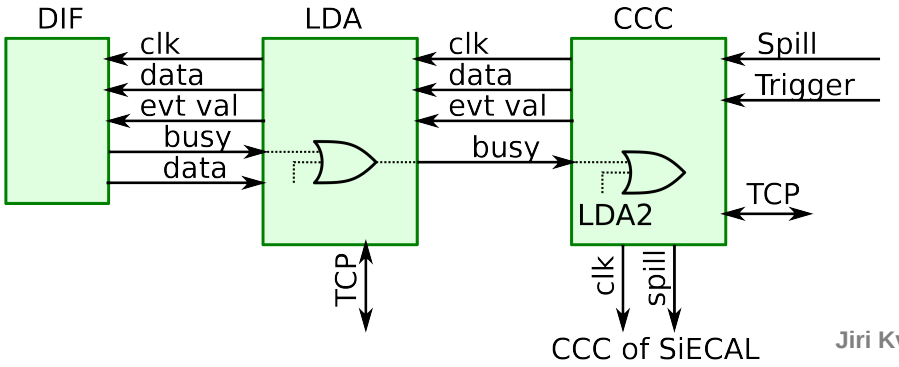
- DMA transfers are made by Xilinx DMA IP core
- First version developed with close cooperation with Mainz
- Bug in the Xilinx kernel driver observed => driver had to be rewritten
- Current version talks directly to the DMA core via IO calls from kernel
- Benchmark result
  - 210 MB/s via loopback in the FPGA and 128 kB packets (first version)
  - 13 MB/s with random packet generator (4B – 8kB)
  - 4000 transfers/s (poor performance => packets merged as much as possible in LDA)
- Performance not fine tuned, tuned for stable operation only



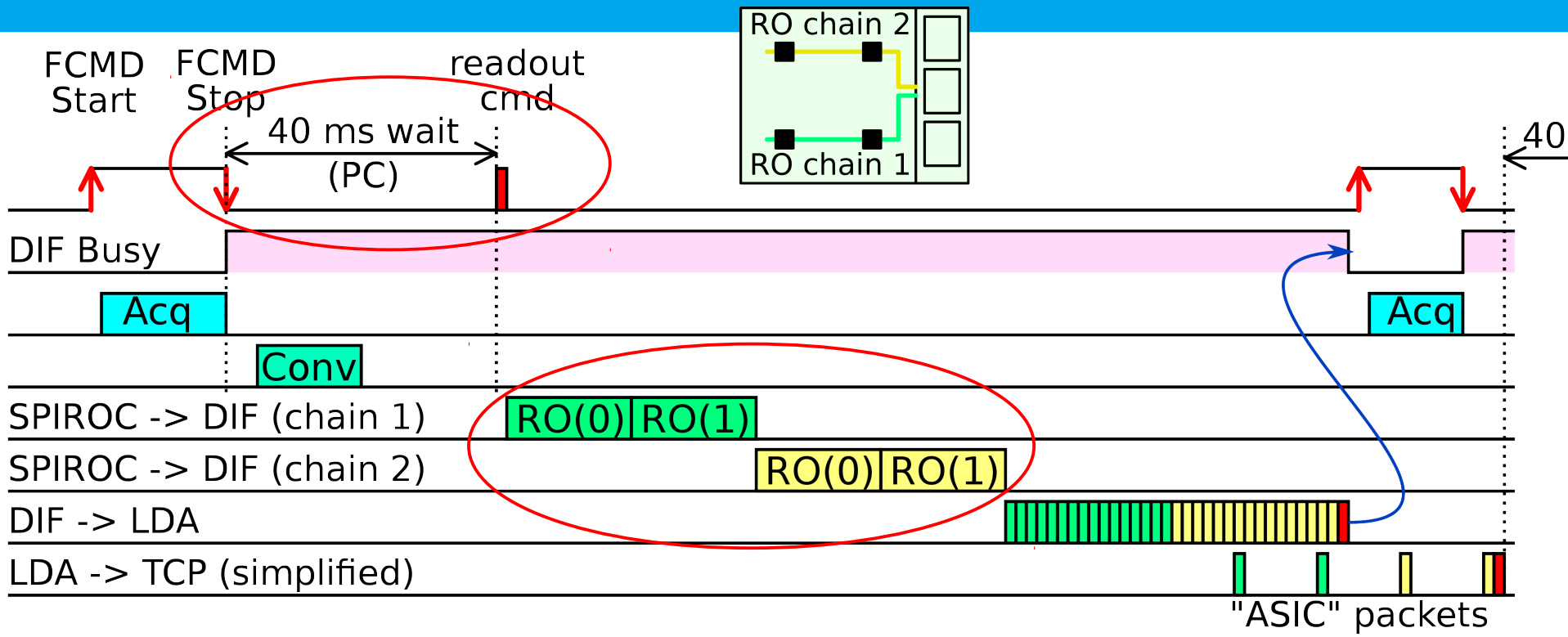
Common running timing @CERN PS

- 40 + 50 MHz clock from ScDAQ CCC
- 5MHz derived clock synchronized for ScDAQ at the beginning of each run
- Fast commands only for ScDAQ
- Busy evaluated only from ScDAQ
- Diagrams: tentative values only (rough estimates)
- RO cycle number in the data packets added by LDA



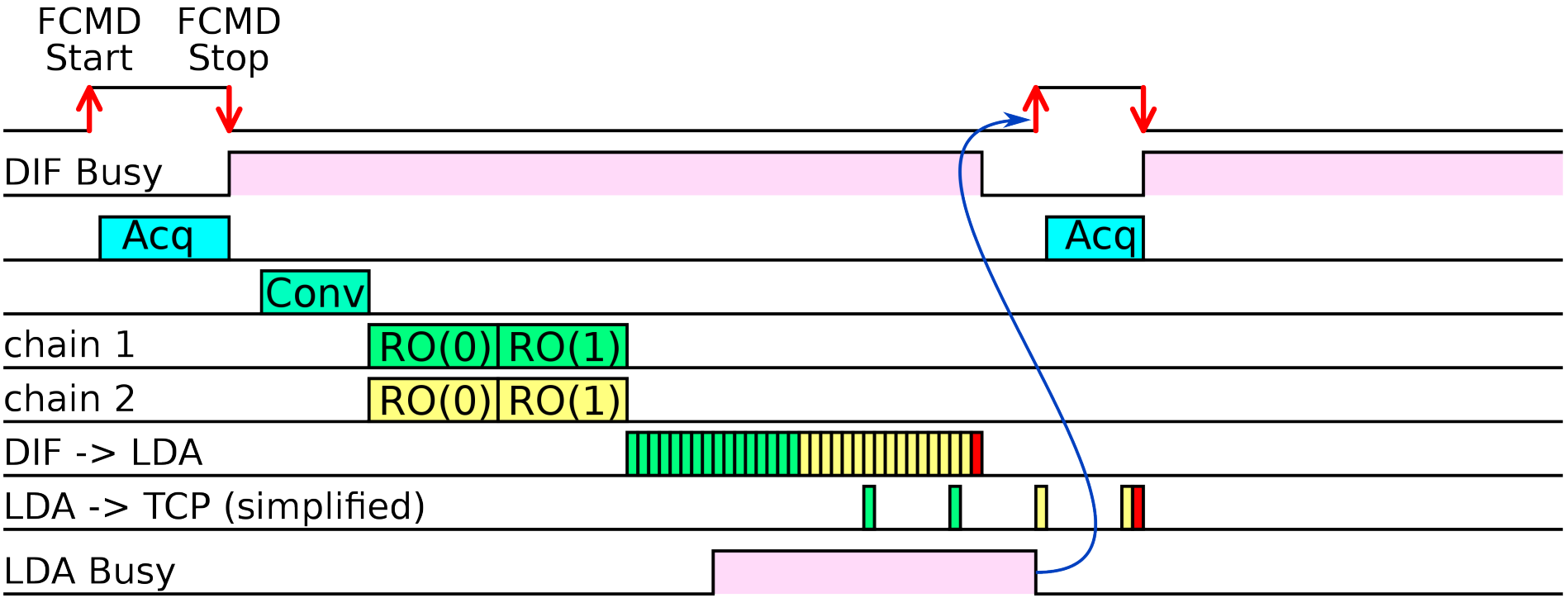


General DAQ timing



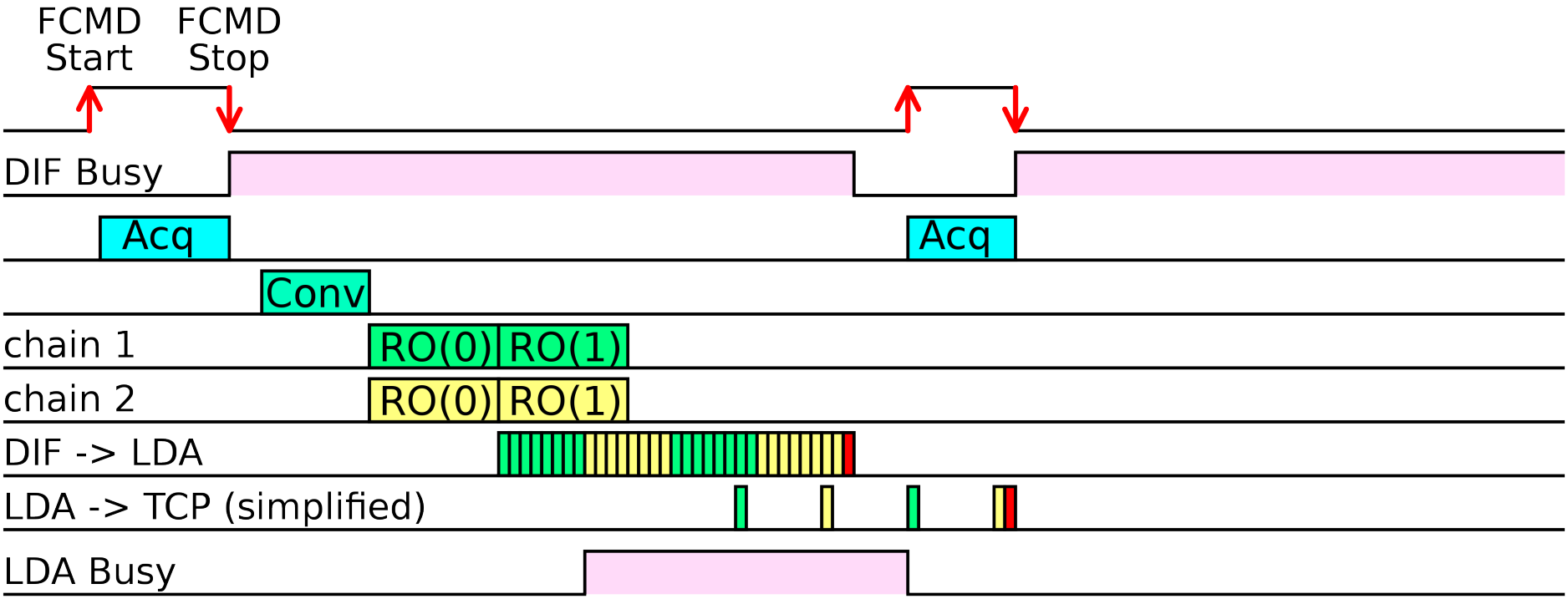
- A lot of time wasted in waiting for the readout command
- Data from SPIROCs are readout in chain sequentially
- Acquisition is started when all data are sent from the DIF, however:
- 40ms wait is counted from the last packet received from TCP

Command-less and Parallel ASIC readout



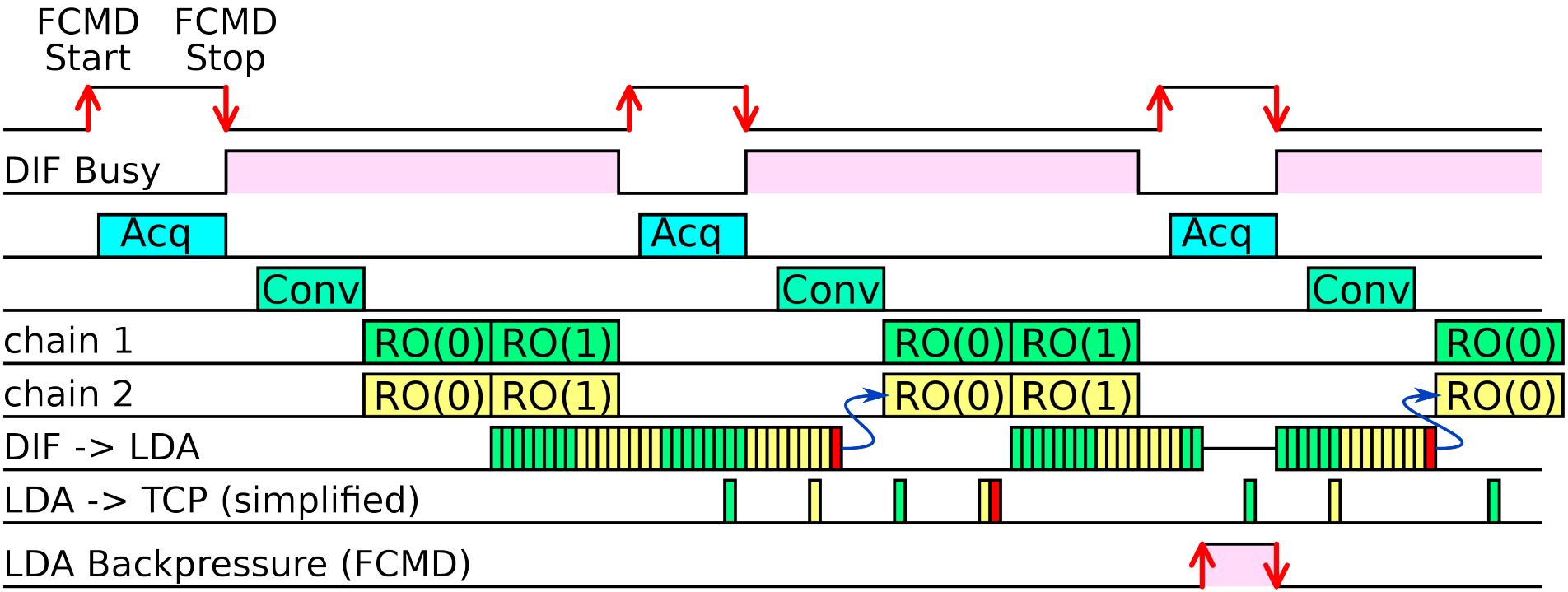
- Readout of SPIROC can start as soon as the conversion is done
- Readout of SPIROC readout chains can be parallelized
- Sending of the data from the DIF to LDA can be started automatically when the LDA is ready to handle the full readout. Easy fix: LDA contributes to the busy signal
- RO cycle number in LDA

Parallel readout and sending data



- In principle we can start sending the data from DIF as soon as there is a full ASIC data in the DIF memory.
- => needs more effort on the DIF side

Independent data sending



- We can (the DIF is capable of) start new acquisition as soon as all SPIROCs are fully read out
- DIF → LDA transfer will run in parallel (on the background)
- LDA backpressure mechanism needs to be implement
- Danger of EMC noise during acquisition
- RO cycle number has to be provided by DIFs (not LDA)

Beam interface (BIF): Signals time stamping

- **Currently**: T0 channels in SPIROC were used for timing reference from external inputs → the only information we have
- **Proposal**: Time stamping can be easily and reliably done in FPGA (It is a digital problem)
  - >= 2 ns: really simple
  - >= 1 ns precision without any enormous effort
  - <1 ns precision is possible, but more difficult.
  - Requirements for time stamping precision?
- Multiple signals can be timestamped in parallel (both Cerenkov, all trigger scintillators, wire chambers...)
- It can be made easily as a ZEDBoard mezannine with lemo inputs
- Might be interesting also for others
  - Cosmic test stand @Mainz ?
  - Any ScCAL testbeam

Next year DAQ plans

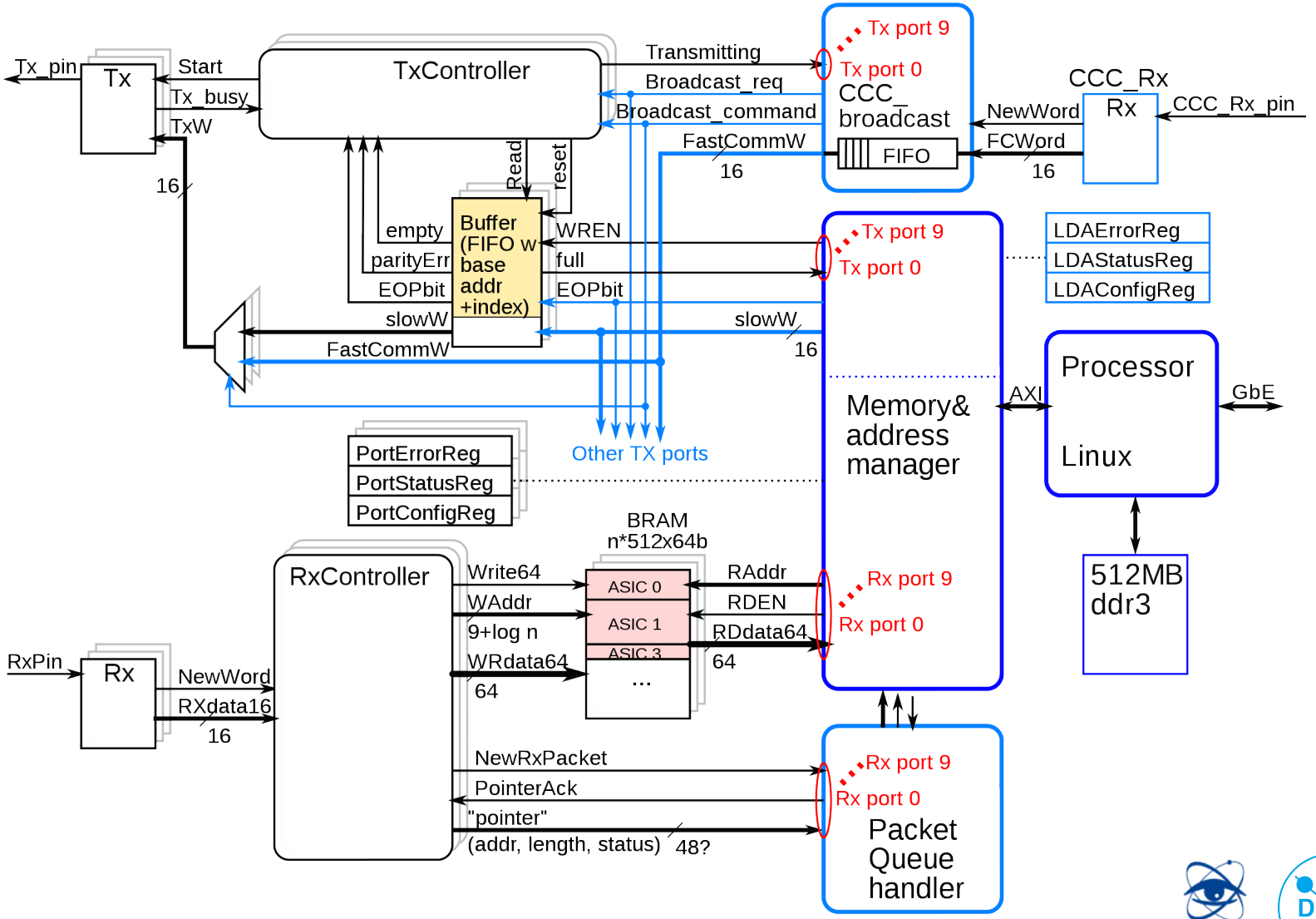
- Wing-LDA
  - Link between 2 FPGAs, Kintex on the Wing-LDA daughterboard and Zynq on the MARS module has to be designed (10 bidir diff pairs)
  - The Kintex will contain the most of the mini-lda functionality (similar design)
  - Zynq will synchronize all Kintexes and collect all data for further processing in the embedded Linux
- DIF speedup (depends on the priorities)
- 8B10B link protocol incorporation
  - We want to be maximally compatible with other DAQs
  - CCC → LDA,
  - DIF → LDA, LDA → DIF
- Software
  - Labview → ?

Summary

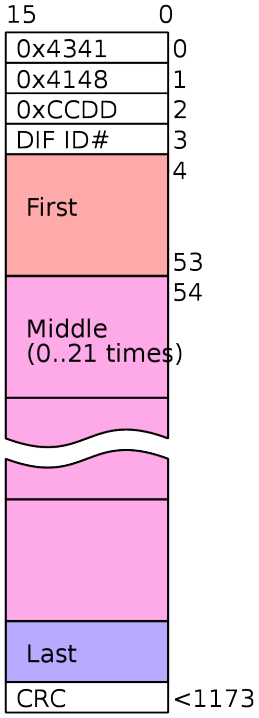
- New HDMI readout of the AHCAL + ScECAL detector was implemented
- 2 mini-LDAs used successfully during the last beamtest @PS CERN
- The full HDMI readout with LDA was running very stable (no single intervention or restart needed)
- Still big space for timing optimization left in order to squeeze maximum performance from SPIROCs during testbeams
- Versatility of the Mainz Zedboard CCC design allowed on-site adoption of the common running with SiECAL
- Still a lot of work to be done in the DAQ in terms of compatibility with other calice DAQs and common running

Backup

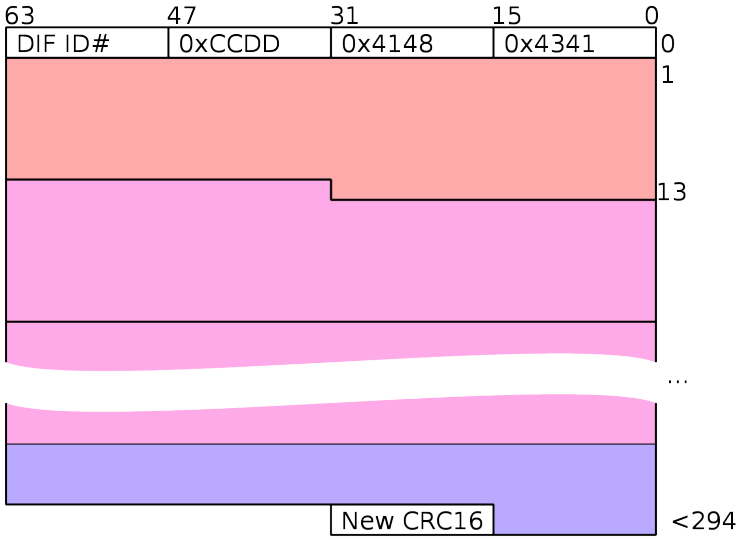
LDA concept 2014-06-24



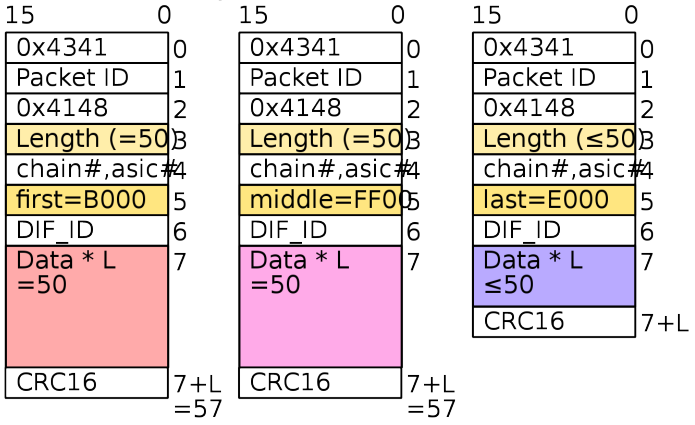
Packet merging



Merget READOUT packet: (16-bit/64bit addressing)



READOUT packets: first, middle and last



Block transfer command,ack