Status report from Lund

8.1.2015

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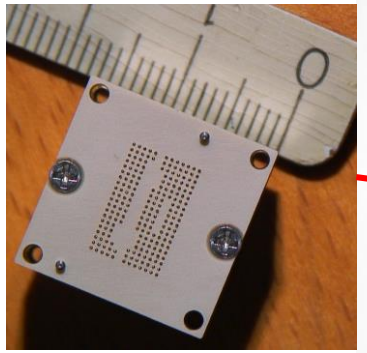
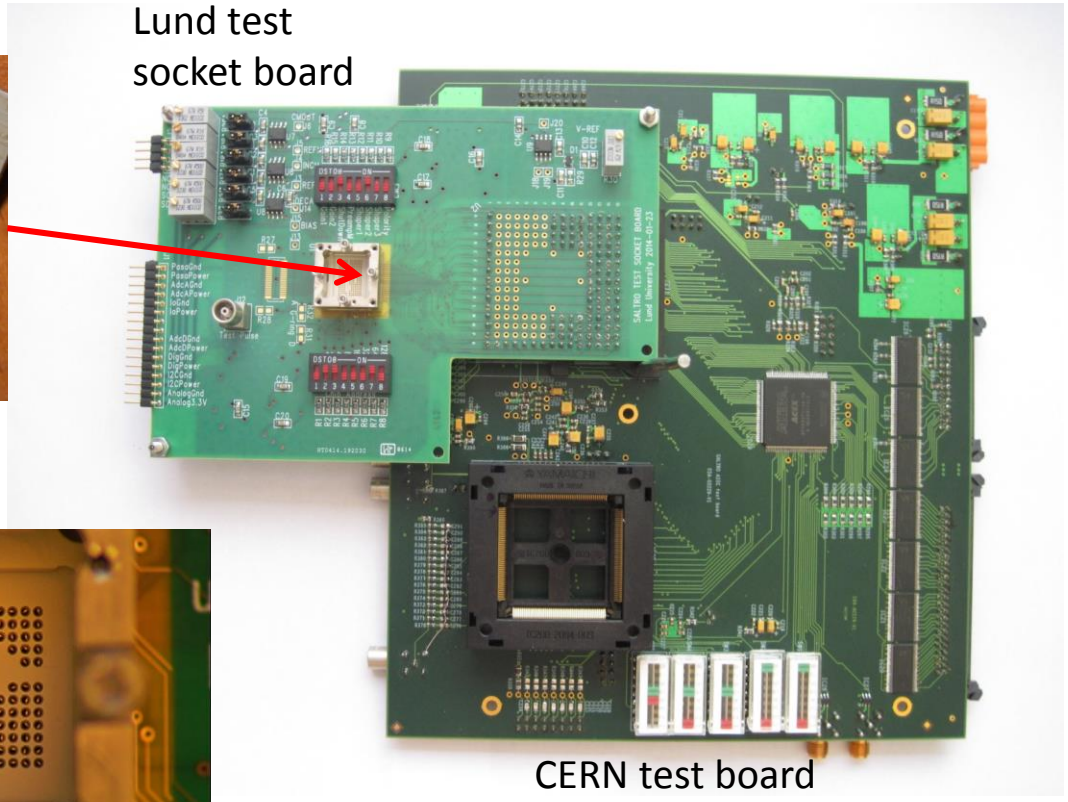
Test set-up for testing SALTRO16-chips on Carrier Boards

- The test set-up for testing SALTRO-chip mounted on Carrier Boards is assembled and we have tested the first boards.

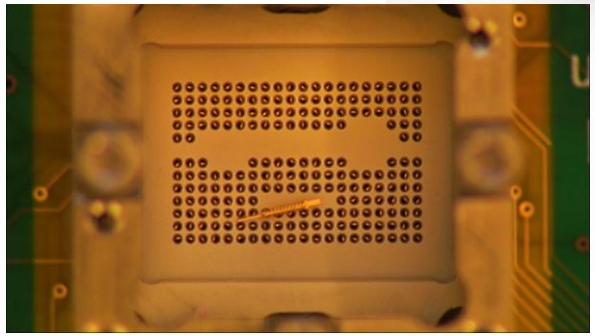
Test socket

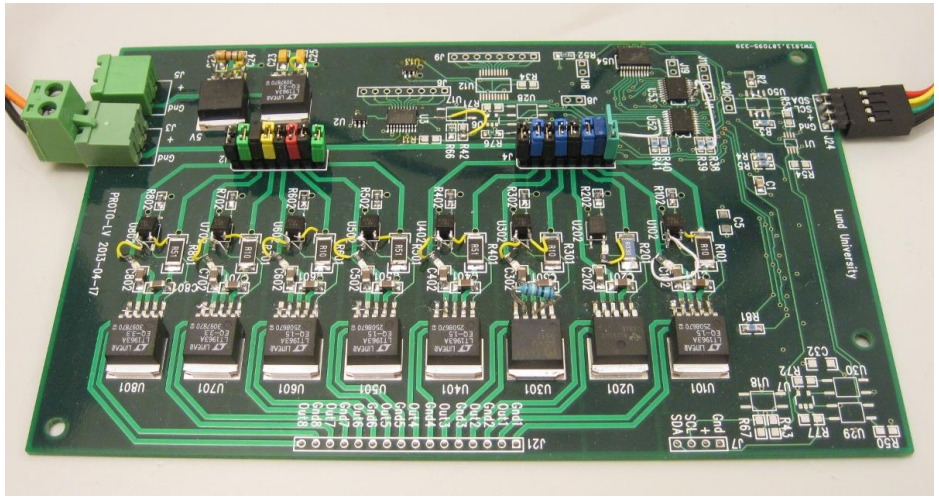


Lund test socket board



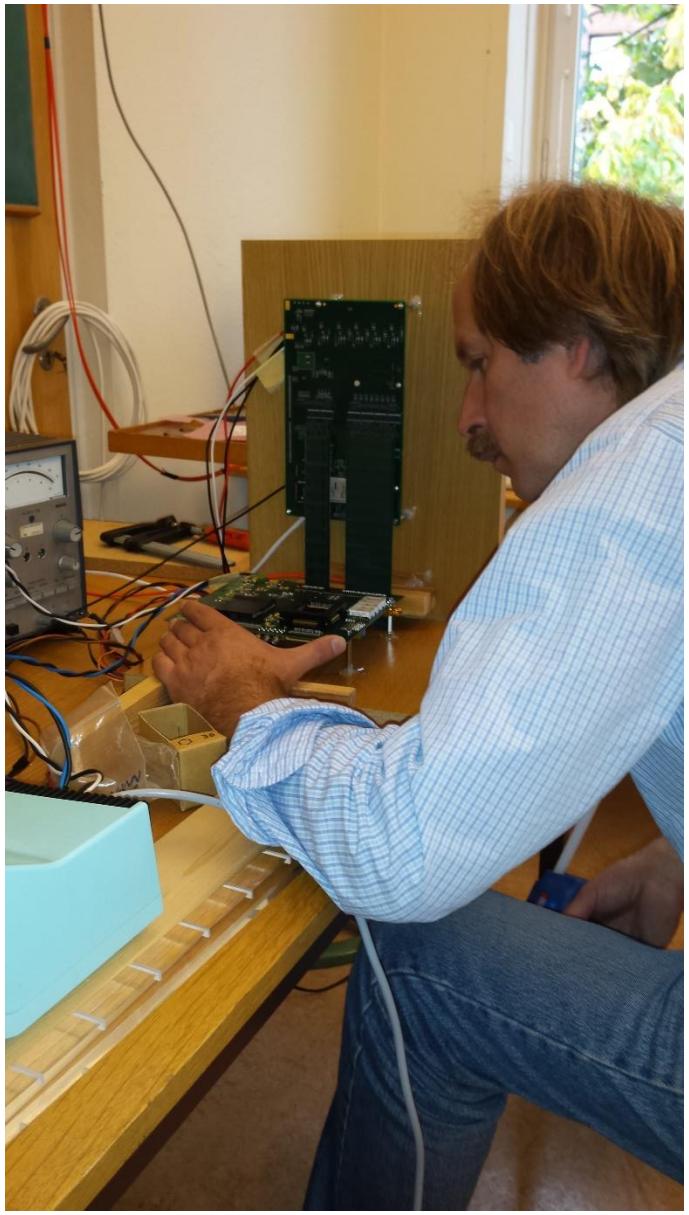
CERN test board

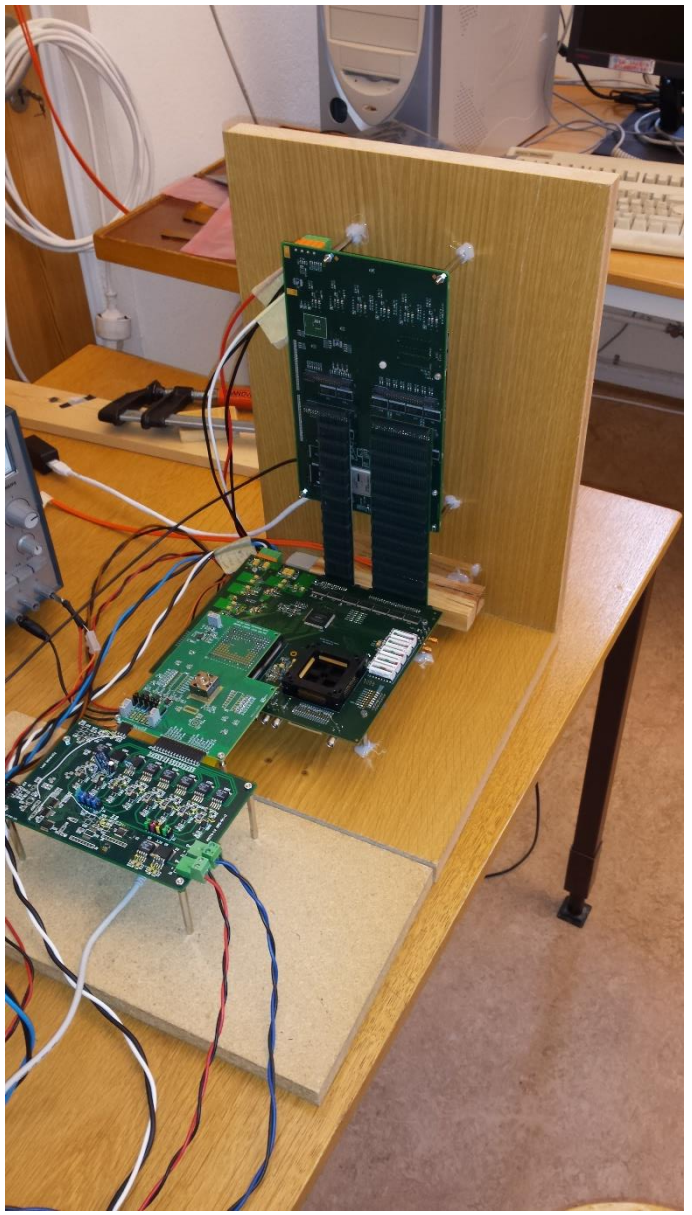




LV-prototype board

The test set-up being assembled





Tests of Carrier Boards

The preparation for tests of a carrier board include the following steps:

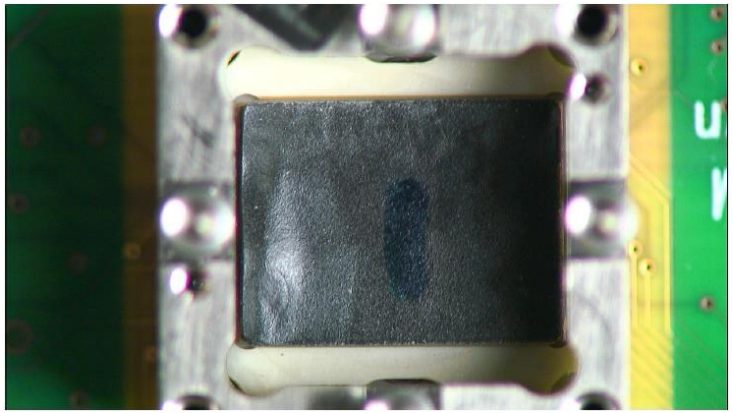
- Place the carrier board in the test socket, in which it fits very precisely, so that the sensor pins are directed towards the tin balls on the bottom side of the board.
- A fairly big force must be applied to the top surface to make sure that all pins make electrical contact to the balls.
- This require a certain flatness of the epoxy layer, applied to the top side of the carrier board.
- We might be forced to introduce some elastic material to distrbute the force more evenly over the full surface.
- Test will be made with a globbed dummy carrier board.

- An unmounted carrier board with shorted top surface will be used to test the connections of the test system

Carrier board 1

Observation:
- The glob did not have a straight edge (see the left side)
  ⇒ the board did not fit the test socket
- The upper surface was not flat

⇒ A rubber piece had to be put on top so that the pressure was more evenly distributed



- After carefully machining off the additional material the board was made to fit the test socket

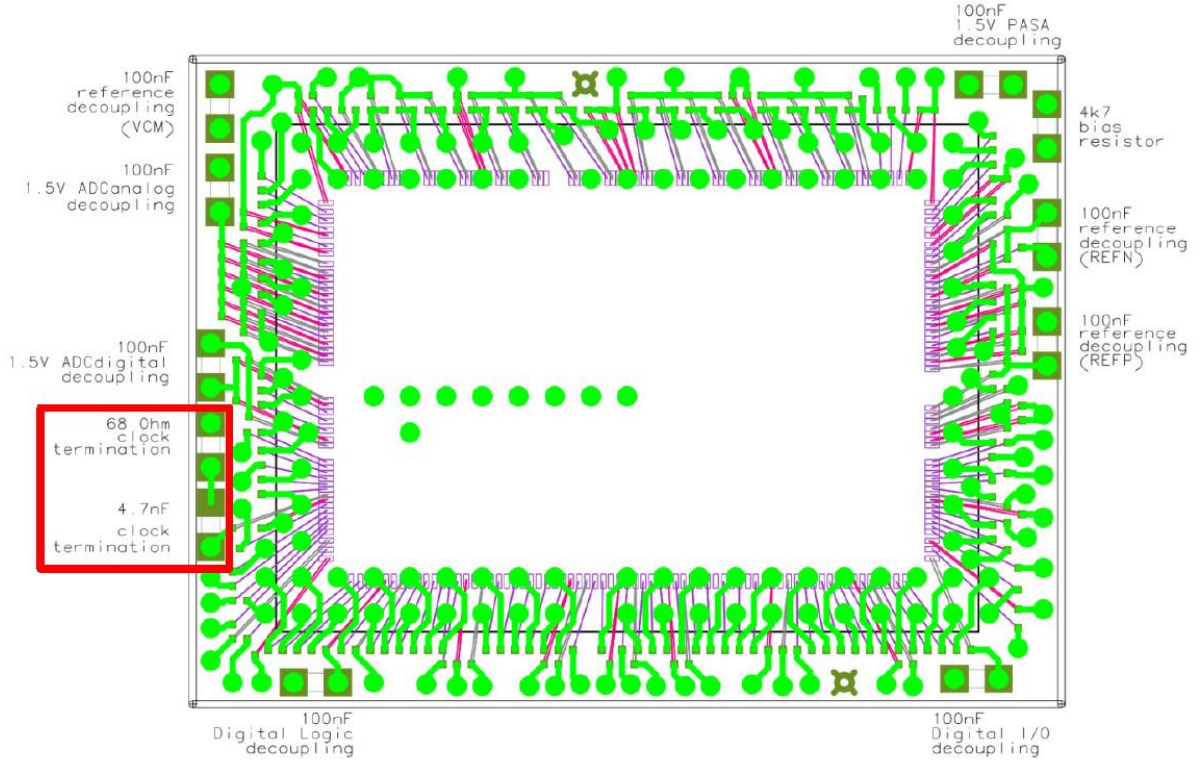
Testresults of carrier board 1

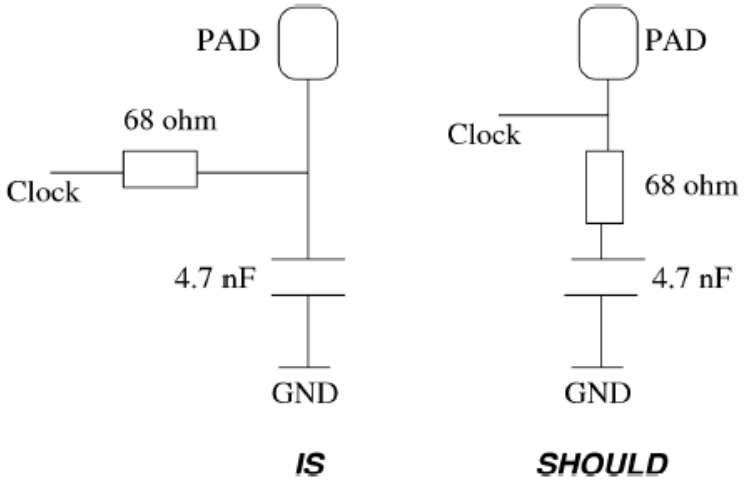
- Two shorted pair of bond wires were found
- A capacitor was wrongly mounted ⇒ the sampling clock was wrongly terminated so that the clock pulse did not appear(see picture below)

⇒ The SALTRO-chip does not work without the sampling clock

⇒ Due to the shortages the chip is going into non-usable mode i.e. a communication with the chip was not possible

⇒ Probelms with noise, the reason for which is not known





Testresults of carrer board 1

- After the tests the tin balls were inspected and one could see small marks after the sensor pins
- We don't think that this will influence the soldering procedure but this has to be discussed with the company.

Before tests

Afteer tests

Tests of carrier boards 2 and 3

After the negative test results of carrier board 1 we ordered another 2 mounted carrier boards.

Carrier board 2:

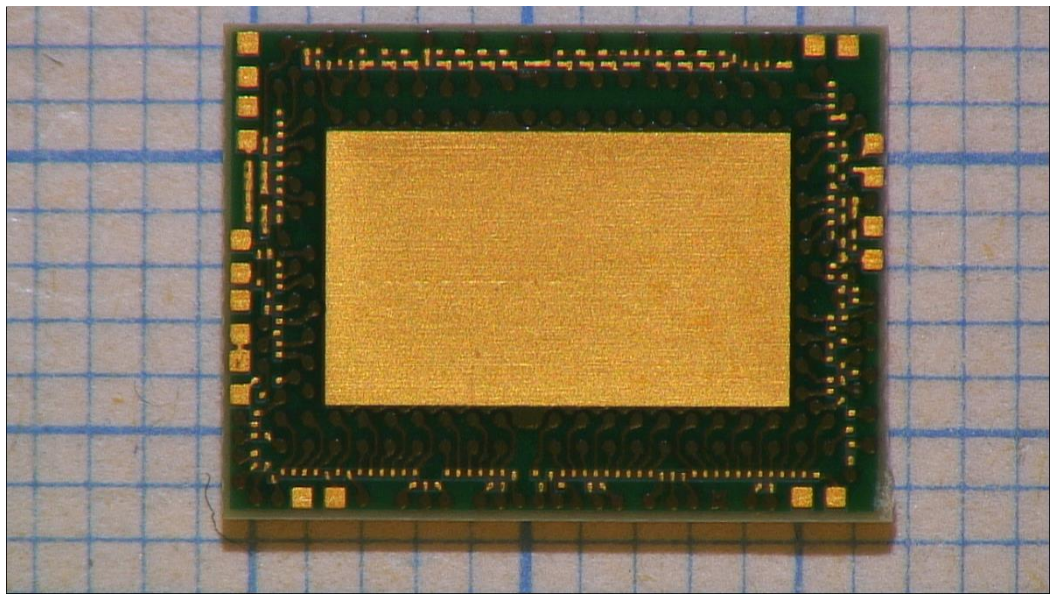
- The chip reacts on write and read commands
- Read values are default values, not written values.
- Read values not always correct (noise?).
- No sampling clock as for chip 1 $\Rightarrow$ check that the wrongly mounted capacitor has been removed
- No connection for chip address bit 5, which specifies the FEC number (probably there is no connection in the test socket or on the carrier board)
- ERROR levels don't behave as expected, it takes too long for them to change between low and high
- The current drawn by the carrier board does not behave as expected with increasing sampling clock frequency.

Carrier board 3:

- Contrary to board 2 there is connection for chip address 5
- No connection for sampling clock, transfer enable and data strobe
- There is a short between power and ground (can not test the board; probably a short in the chip itself)

Next steps

The 7th of January we received 3 naked carrier board which will be carefully investigated



- Make a list of what the various pads should be connected to and check that this is the case
- Check again carefully the design of the carrier board

Next order: require - a picture of the carrier bord after bonding (still sitting in the bonding machine)
- a picture of the carrier board after being mounted in the jig for globbing