CLICpix planar sensor assemblies

Vertex and Tracking Session
Linear Collider Workshop 2015 (LCWS15)

Whistler
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on behalf of the
CLIC detector and physics (CLICdp) collaboration

Outline

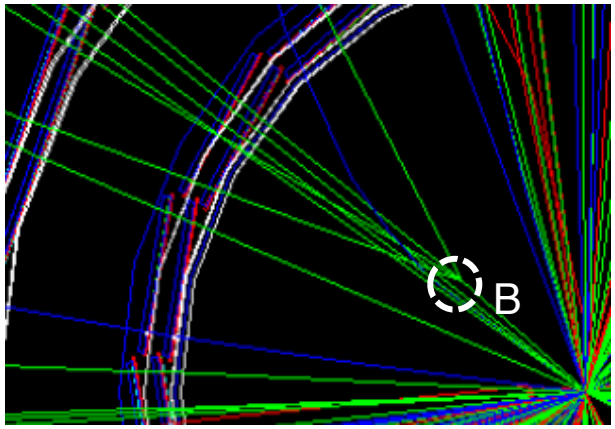
- CLICpix readout ASIC
- Production of planar sensor assemblies
- Lab and test-beam results
- Outlook: CLICpix2
- Summary

Reminder: CLIC vertex-detector requirements

- efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a \sim 5\ \mu m,\quad b \sim 15\ \mu m$$



  - → good single point resolution: σ_{SP}~3 µm
    - → small pixels <~25x25 µm^2, analog readout
  - → low material budget: X ≦ 0.2% X_0 / layer
    - → corresponds to ~200 µm Si, including supports, cables, cooling
    - → low-power ASICs (~50 mW/cm^2) + gas-flow cooling

- 20 ms gaps between bunch trains → trigger-less readout, pulsed powering
- B = 4 T → Lorentz angle becomes important

- few % maximum occupancy from beam-induced backgrounds → sets inner radius
- moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm^2/y
  - TID: < 1 kGy / year

- Time stamping with ~10 ns accuracy, to reject background
  → high-resistivity / depleted sensors, readout with precise timing

Hybrid r/o technology: CLICpix

- **65 nm CMOS hybrid r/o chip**, targeted to CLIC vertex detectors
- based on **Timepix/Medipix** chip family, synergy with HL-LHC pixel r/o projects (**RD53** collaboration on 65 nm r/o)

- **demonstrator chip** with 64 x 64 matrix
- **25 µm** pixel pitch
- simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel

→ front-end **time slicing < 10 ns**

- selectable **compression** logic: pixel, cluster + column-based

→ full chip r/o in < 800 µs (at 10% occup., 320 MHz r/o clock)

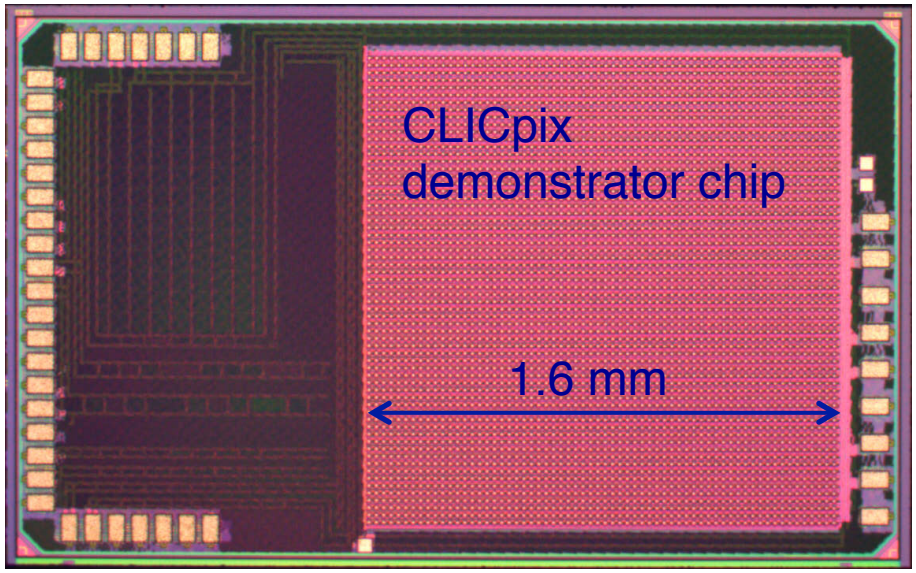
- **power pulsing scheme**

→ P_{avg} < 50 mW/cm^2

- **standalone** lab measurements

→ performance in agreement with simulations

- **test assemblies** with planar and active HV-CMOS sensors



CLICpix standalone measurement results:

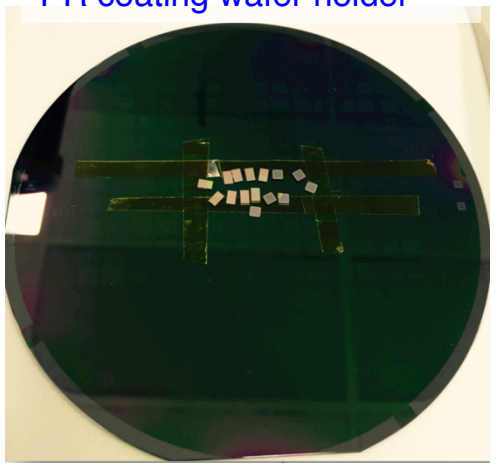
Parameter	Unit	Simulation	Measurement
Rise time	[ns]	50	-
TOA accuracy	[ns]	<10	<10
Gain	[mV/ke$^-$]	44	40 *
Dynamic range	[ke$^-$]	44 (configurable)	40 * (configur.)
Integr. nonlinearity (TOT)	[LSB]	<0.5	<0.5
ENC (w/o sensor)	[e$^-$]	~60	~55 *
DC spread σ (uncalibrated)	[e$^-$]	160	128 *
DC spread σ (calibrated)	[e$^-$]	24	22 *
Power consumption	[µW/pixel]	6.5	7

* results obtained with electrical test pulses

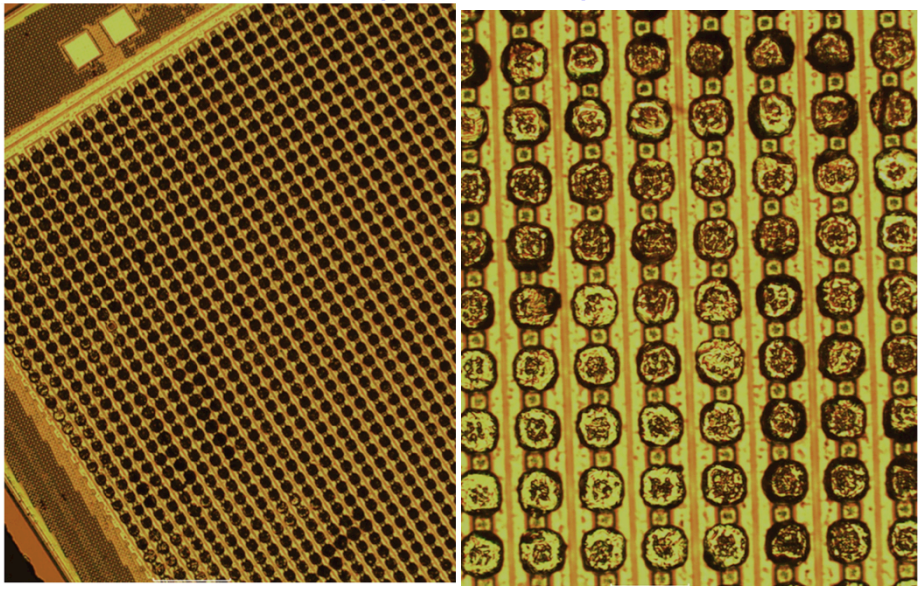
CLICpix planar sensor assemblies

- Single-chip bump-bonding process for 25 µm pitch developed at SLAC (C. Kenney, A. Tomada)
- Process flow:
  - Spin photoresist
  - Expose with contact aligner
  - Evaporator: 4 µm Indium
  - Lift-off
  - Bumping @ low temperature and force (170 °C, 2 N)
- 3 test assemblies produced with 200 µm n-in-p CLICpix sensors from Micron Velopix wafer, labeled “14”, “31”, “43”
- Next: Advacam edgeless sensors with 50-150 µm thickness

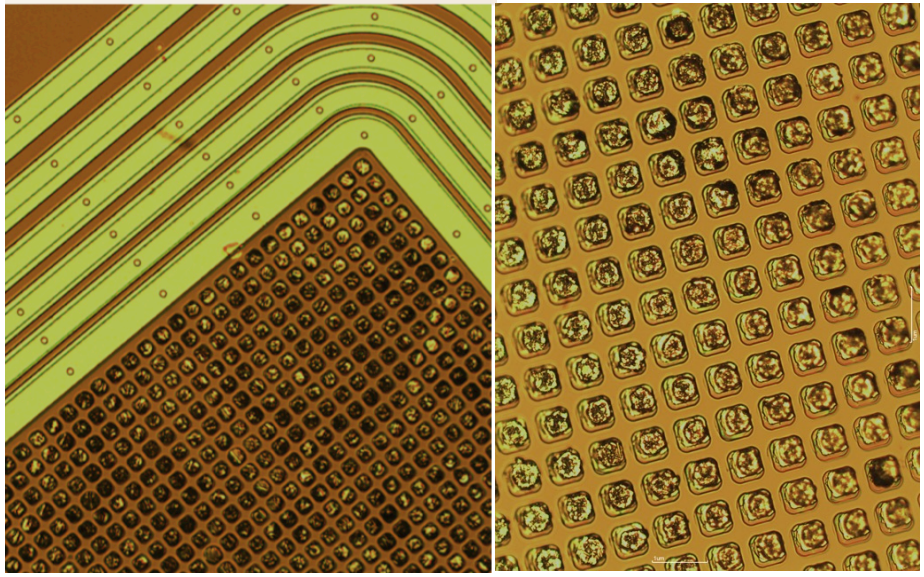
PR coating wafer holder



UBM + Indium bumps on CLICpix ASIC



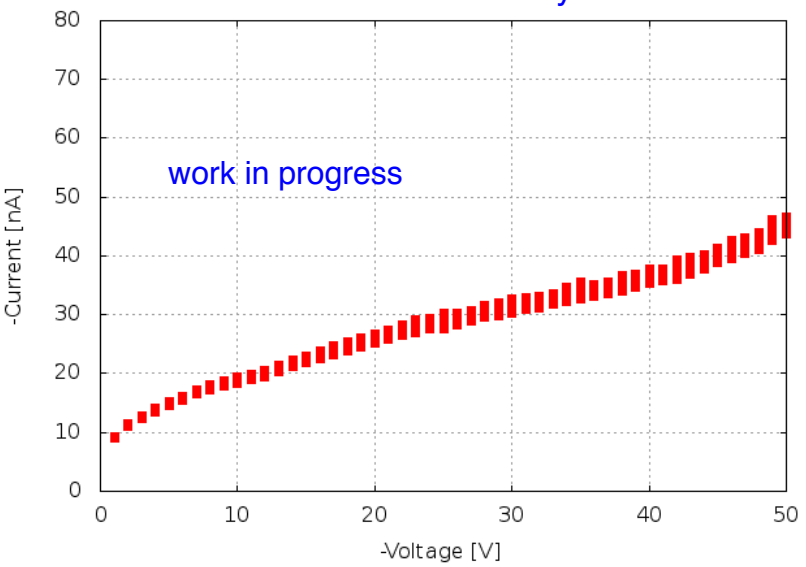
UBM + Indium bumps on Micron sensor



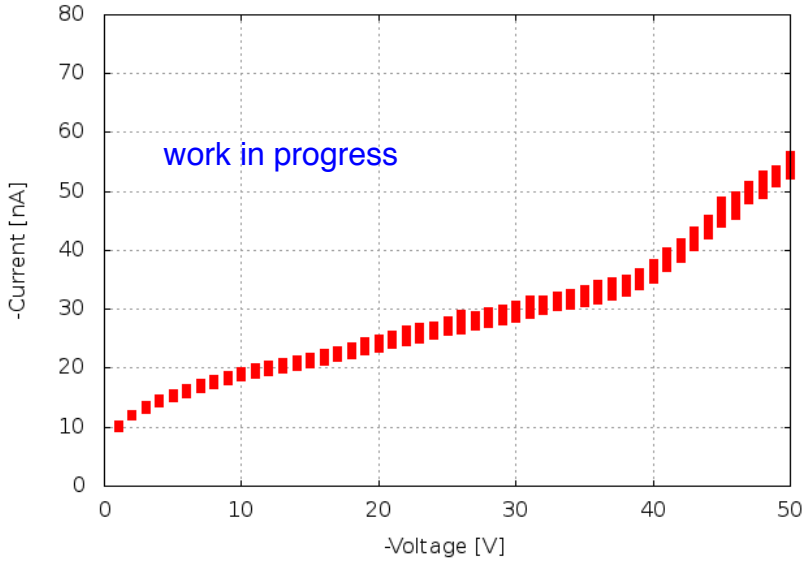
Sensor biasing

- All three assemblies could initially be biased and operated up to >200 V
- Leakage currents <100 nA @ 50 V
- Assembly 14 later showed very early breakdown and could not be operated anymore
  → possibly related to Indium solder contamination that was observed above the sensor guard rings for this assembly

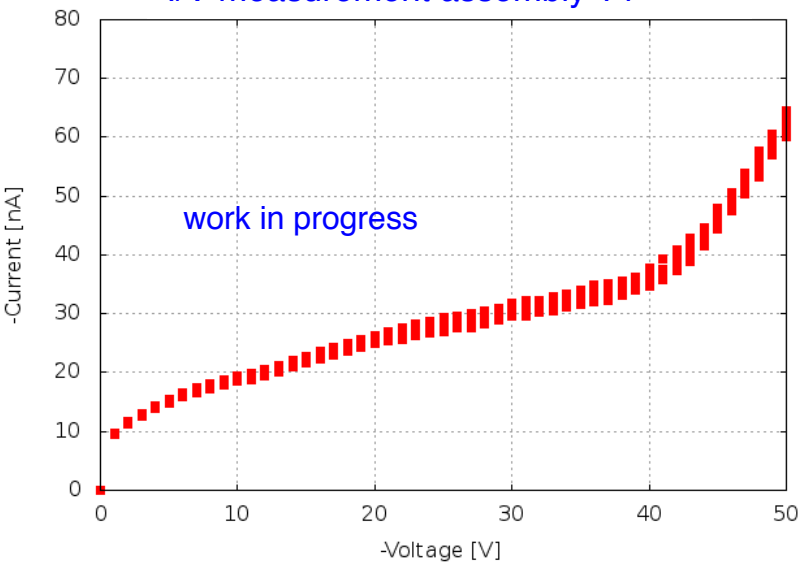
I/V measurement assembly 31



I/V measurement assembly 43



I/V measurement assembly 14



Interconnect yield

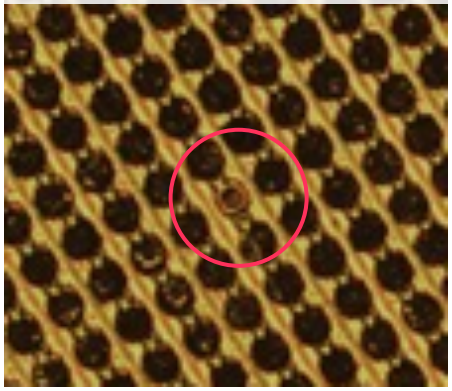
- Irregularities in bump deposition can lead to:
  - Unconnected channels
  - Shorts between channels
- Need to disentangle from ASIC problems

- Lab measurements performed:
  - Noise floor
  - Test pulse response
  - ^{90}Sr source exposition

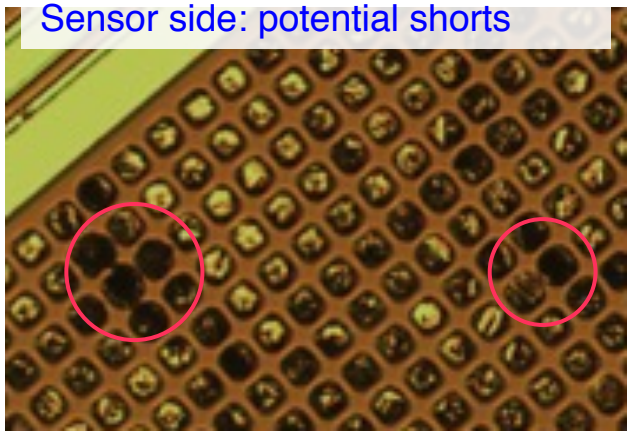
- Unconnected and shorted pixels correlated with defects visible before flipping

Pixel category	Symptom		
	Noise	**Test-pulse response**	**^{90}Sr source response**
Normal	normal	when pulsed	yes
Dead in ASIC	~0	no	no
Dead test pulse	normal	no	yes
Unconnected	decreased	when pulsed	no
Short with neighbor(s)	increased	when pulsed or neighb. pulsed, reduced amplitude	more or less hits, reduced amplitude

ASIC side: missing bump



Sensor side: potential shorts

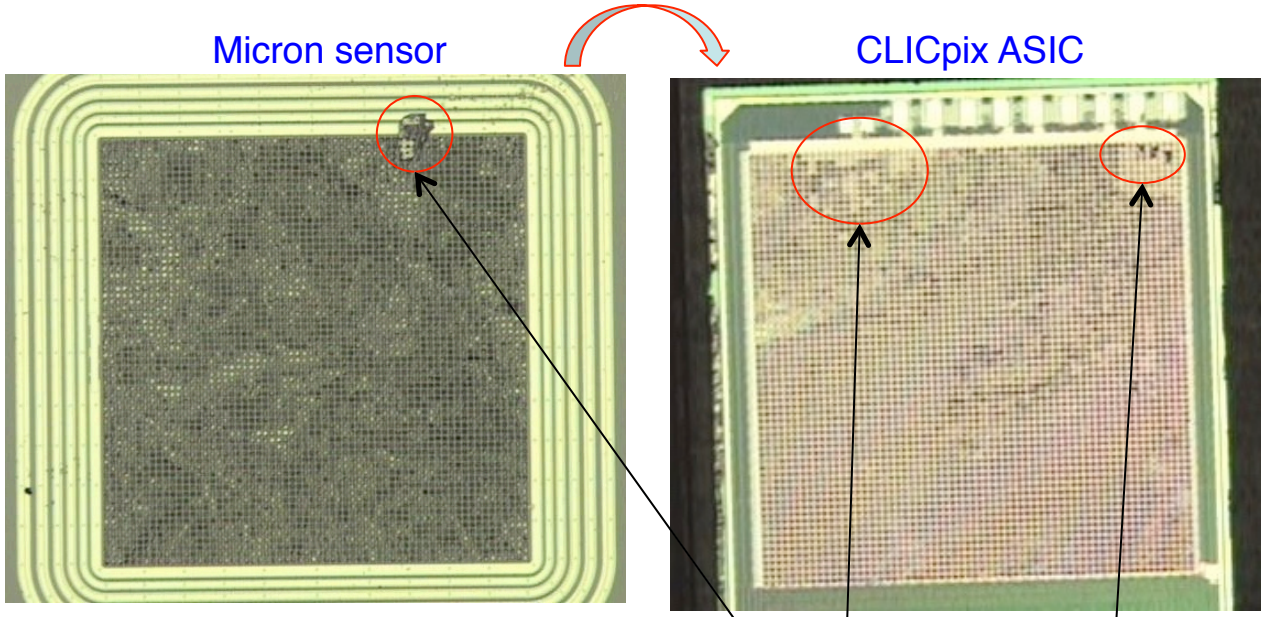


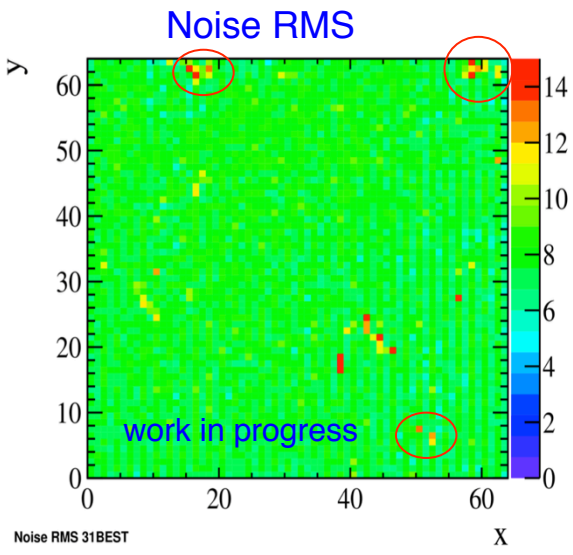
Sensor side: Indium on guard rings

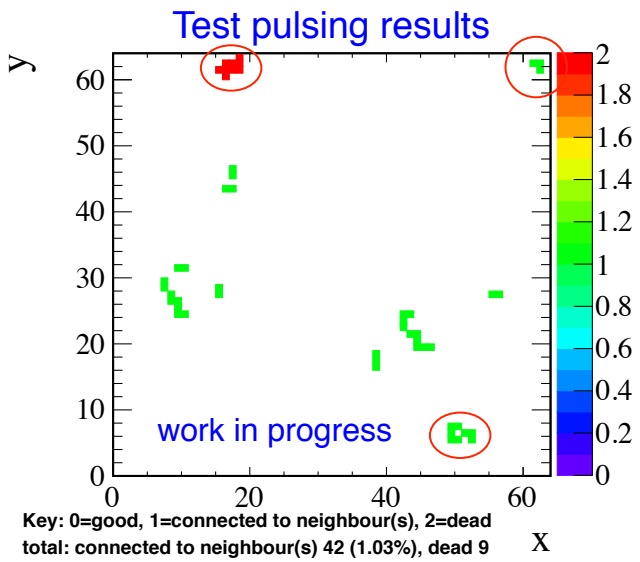
Lab measurement example (II)

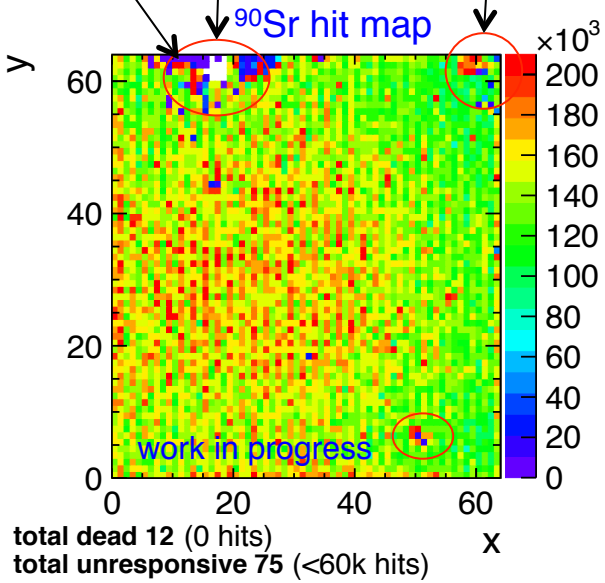
Lab results for assembly 31:

- Best of the three assemblies
- Defects visible in noise, test pulse and source maps
- Correlation of problematic channels with visual inspection results before flipping
- 42 shorts (1%)
- 12 no signal from source (0.3%)
- 75 very weak response (1.8%)









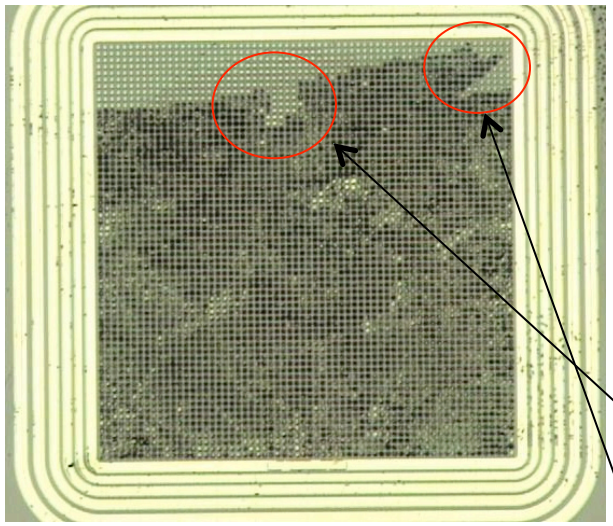
Lab measurement example (I)

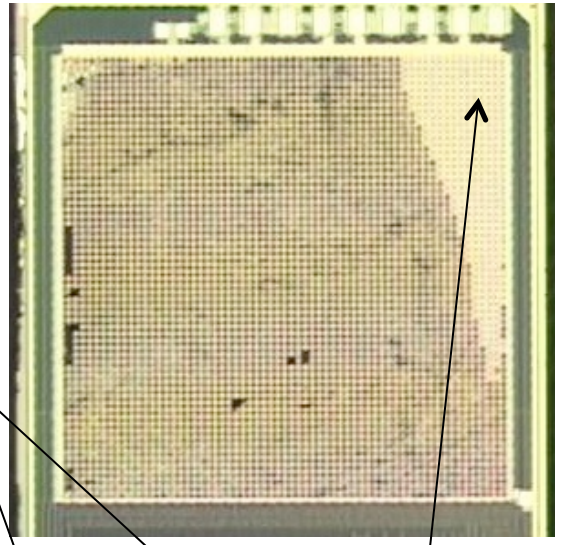
Lab results for assembly 43:

- Worst of the three assemblies
- Defects visible in noise, test pulse and source maps
- Correlation with non uniform solder deposition on chips
- Large clusters of shorted pixels may appear as dead or weakly responding, due to signal loss
- 42 shorts (1%)
- 123 no signal from source (3%)
- 921 very weak response (22%)

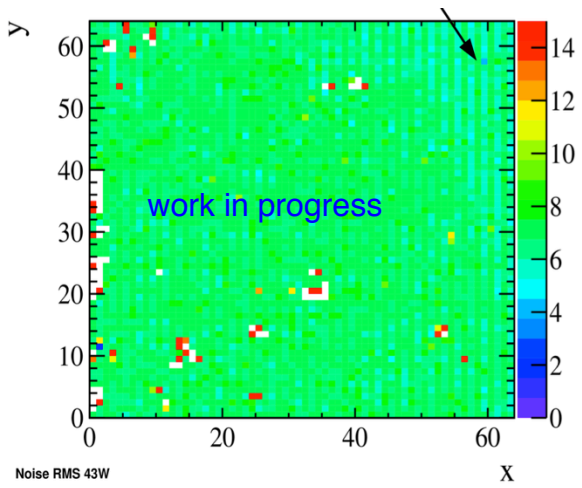
Micron sensor

CLICpix ASIC

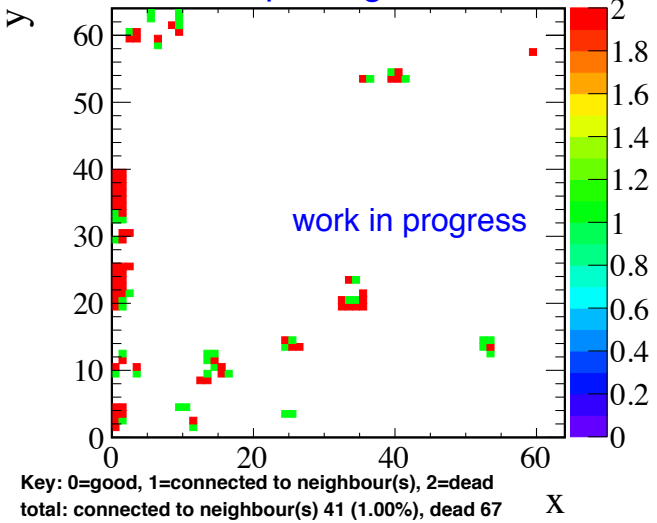




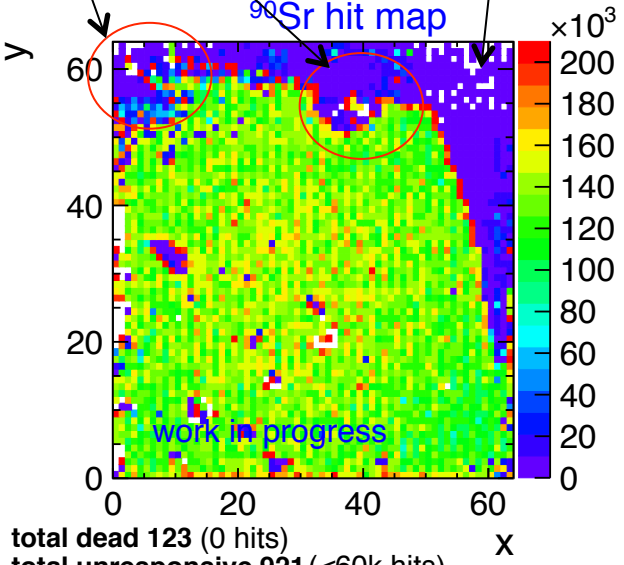
Noise RMS



Test pulsing results



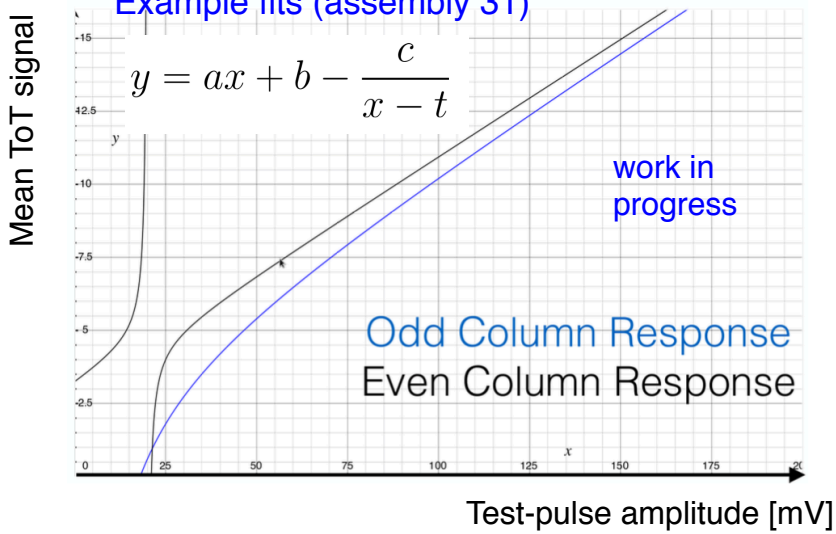
^{90}Sr hit map



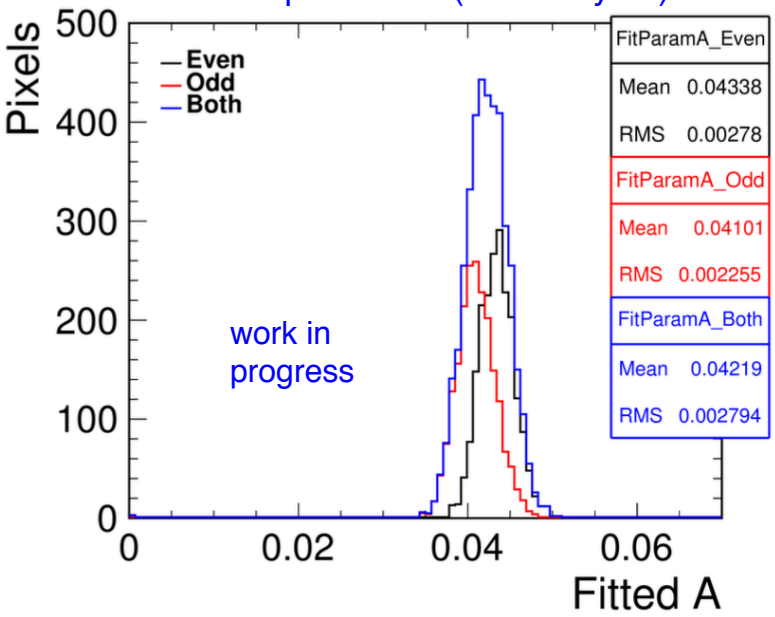
Energy response calibration

- Calibration of energy response using test pulses of known amplitude
- Per-pixel fits with surrogate function
- Different response of even/odd columns, caused by know CLICpix issue:
  - cross talk from discriminator to preamp
  → additional fixed negative charge (~625 e^-)
  - More pronounced for even columns due to superpixel layout
- Distribution of fit parameters sensitive to interconnect quality
- Spread of gain ("A" parameter) ~7%

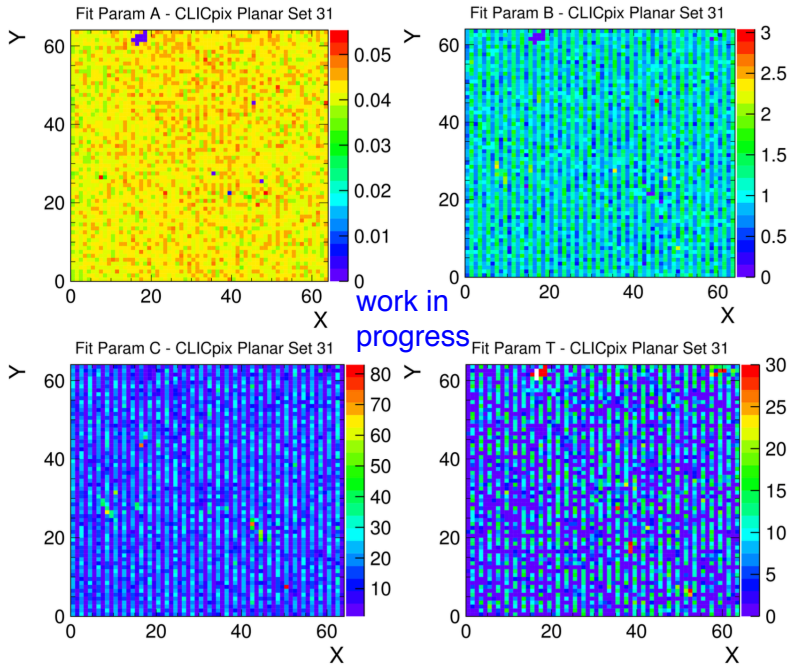
Example fits (assembly 31)



Fitted A parameter (assembly 31)



A,B,C,T parameters (assembly 31)



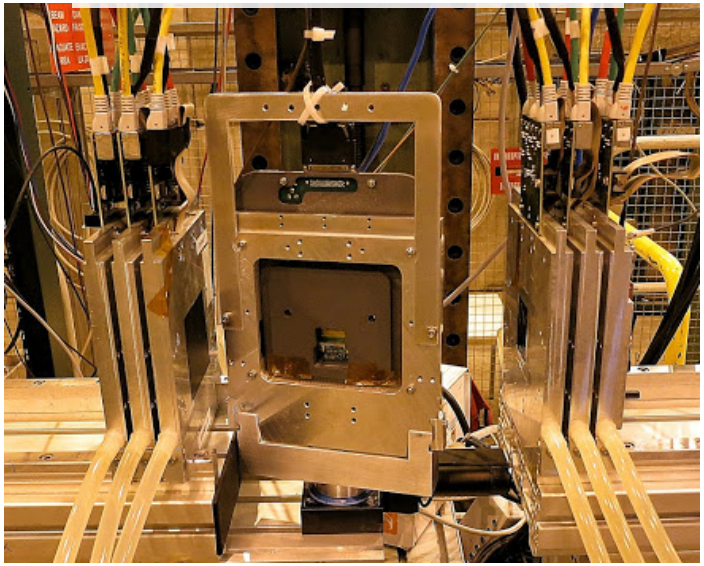
Test-beam data taking

Beam test August/September 2015 in CERN SPS

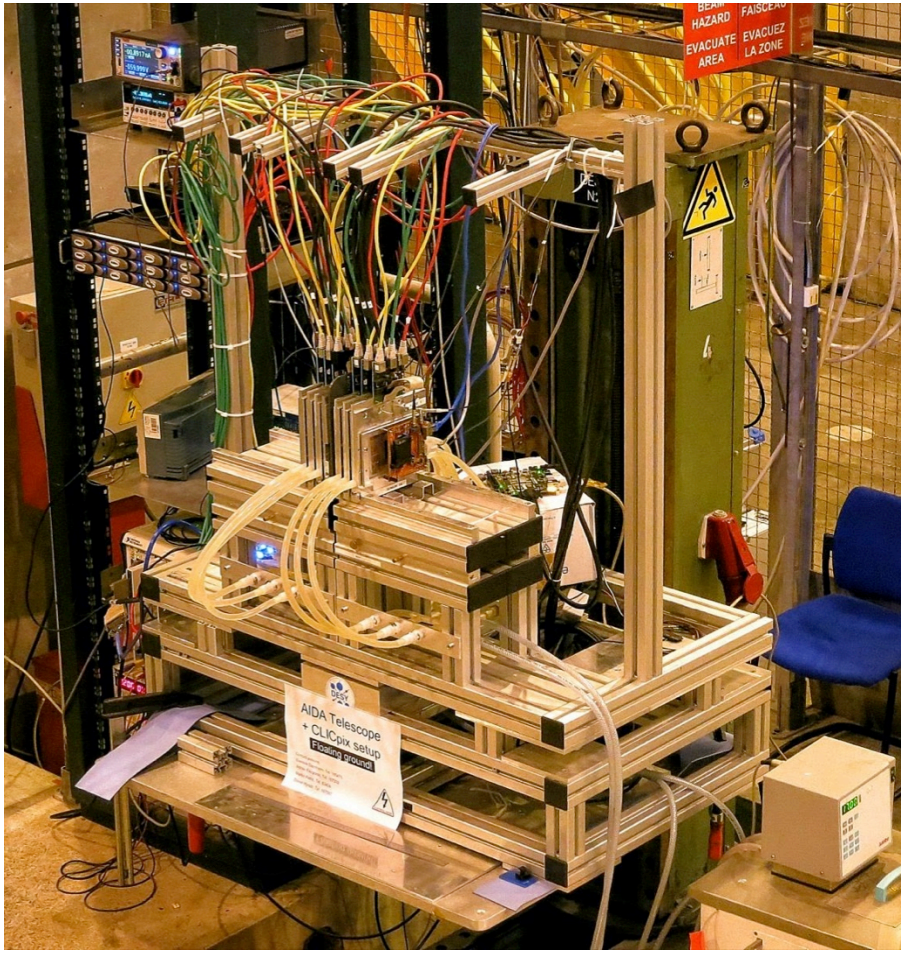
- AIDA EUDET 6-planes telescope
- DUT on rotation holder for angle scans
- Pointing resolution at DUT ~1.6 µm

- Assemblies #31 and #43 tested
- Nominal operating conditions:
  - V_{bias}=50 V (Vdep~35 V)
  - Threshold: ~900 e- (#31), ~1200 e- (#43)
- Scans of threshold, bias, rotation angle

CLICpix DUT on rotation stage



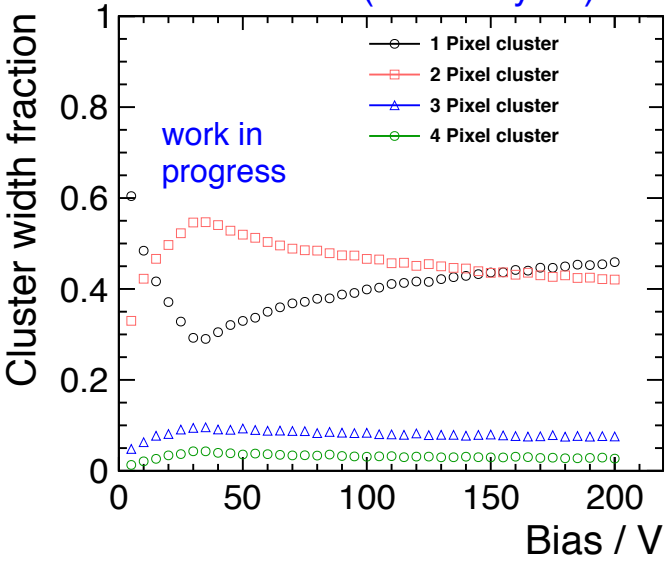
AIDA EUDET telescope in CERN SPS H6B



Clustering

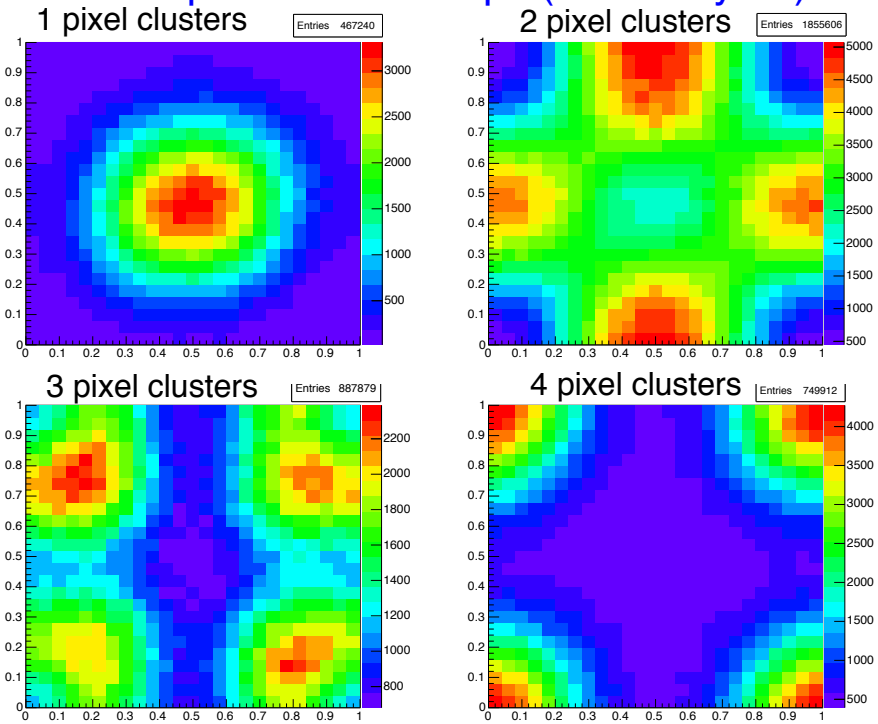
- Cluster size increases up to depletion (increased charge sharing), then decreases (higher drift)
- ~30% single-pixel clusters at $V_{bias}=V_{dep}$~35 V
- Track positions within pixels as expected for the different cluster sizes
- Cluster-size distribution across the matrix shows sensitivity to interconnect quality

Cluster width (assembly 31)

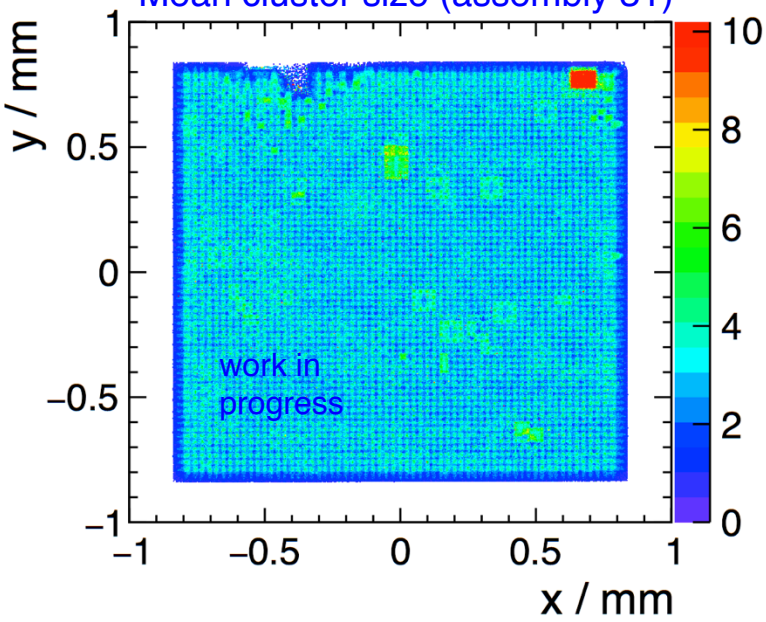


In-pixel cluster maps (assembly 31)

work in progress



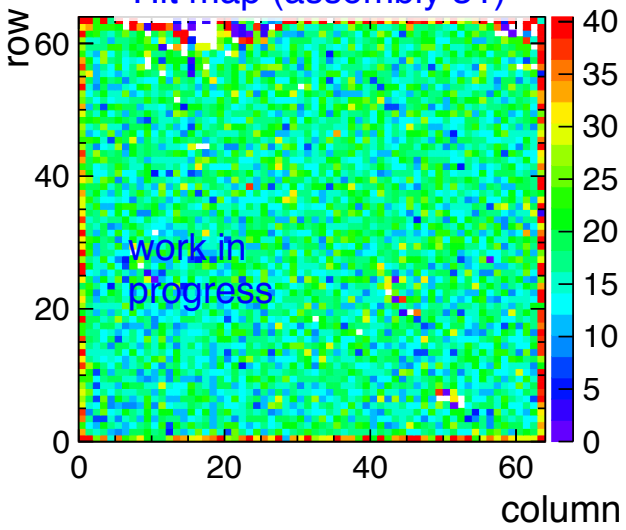
Mean cluster size (assembly 31)



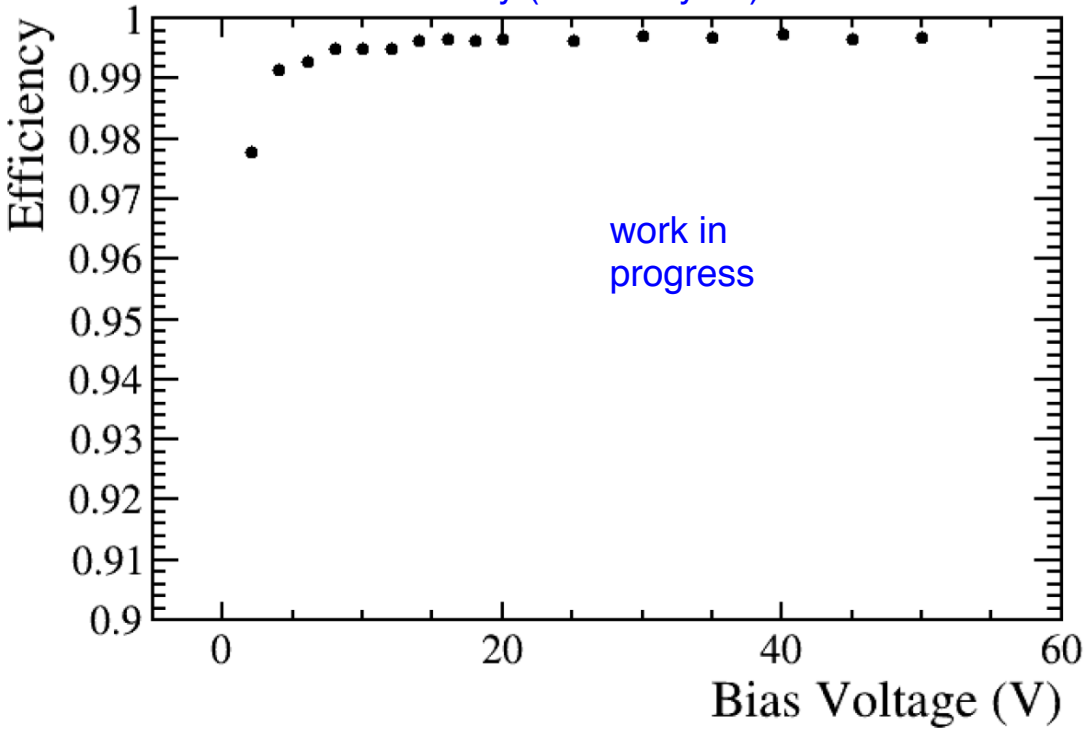
Efficiency

- Hit maps in test beam: number of associated tracks per pixel
- Efficiency determination: look for hits associated to telescope tracks (within a distance of 50 µm)
- Similar results as for source measurements: Bonding defects visible as reduced / increased efficiency
- Overall efficiency very high: >99.5% at depletion

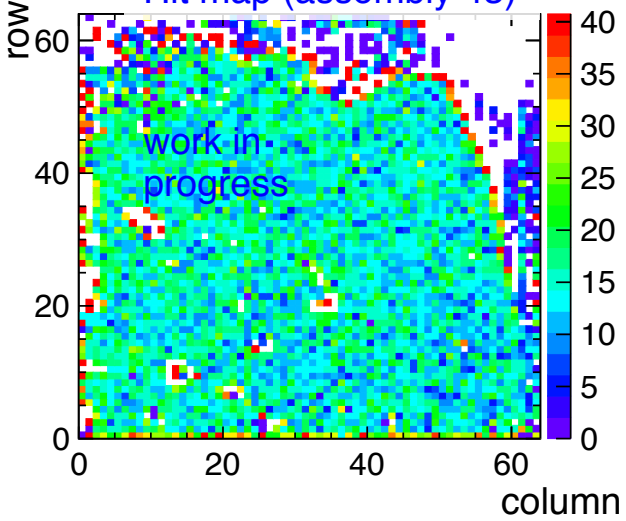
Hit map (assembly 31)



Efficiency (assembly 31)



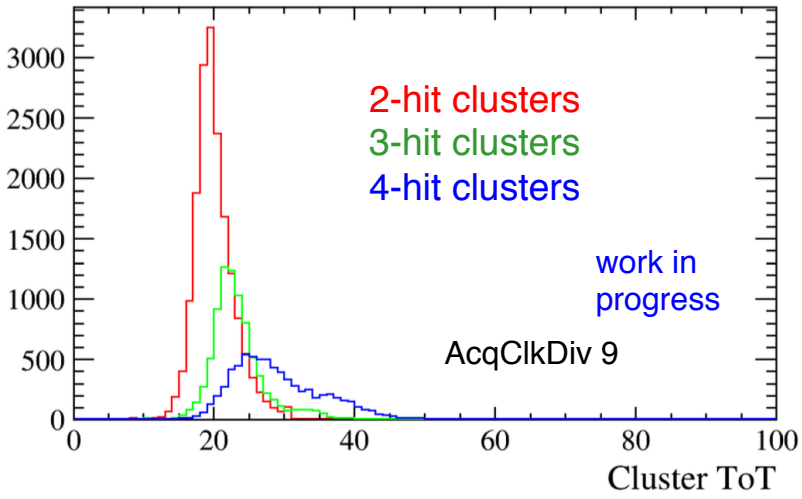
Hit map (assembly 43)



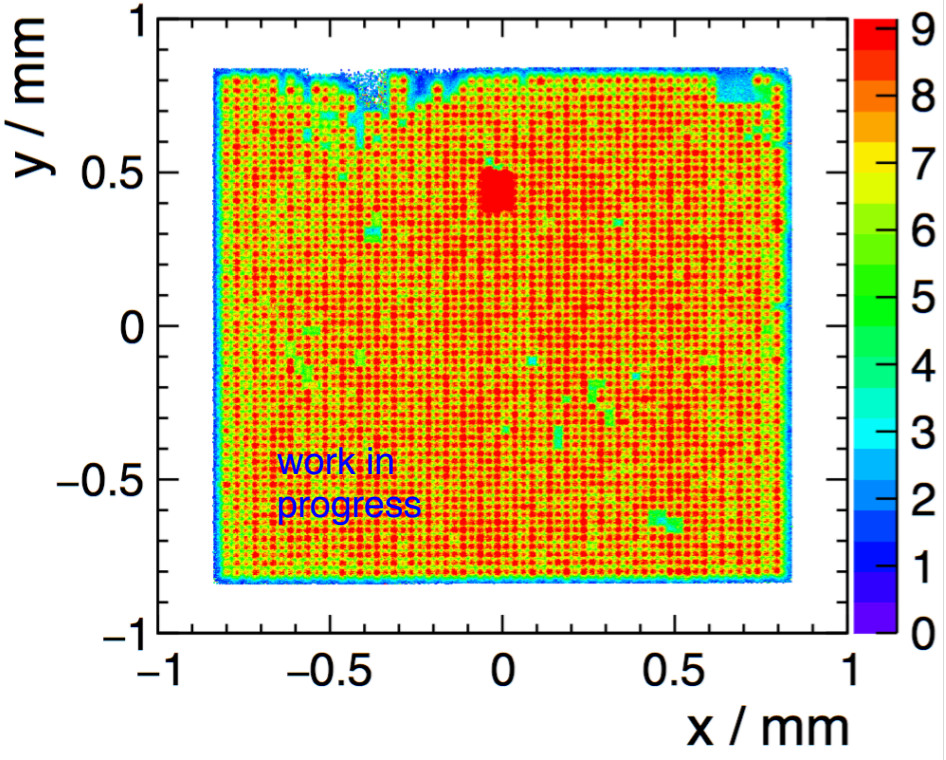
Hit-energy measurement

- 4-bit ToT measurement in CLICpix
- Landau distributions for MIP clusters
- Mean seed-pixel energy across the matrix shows sensitivity to interconnect quality

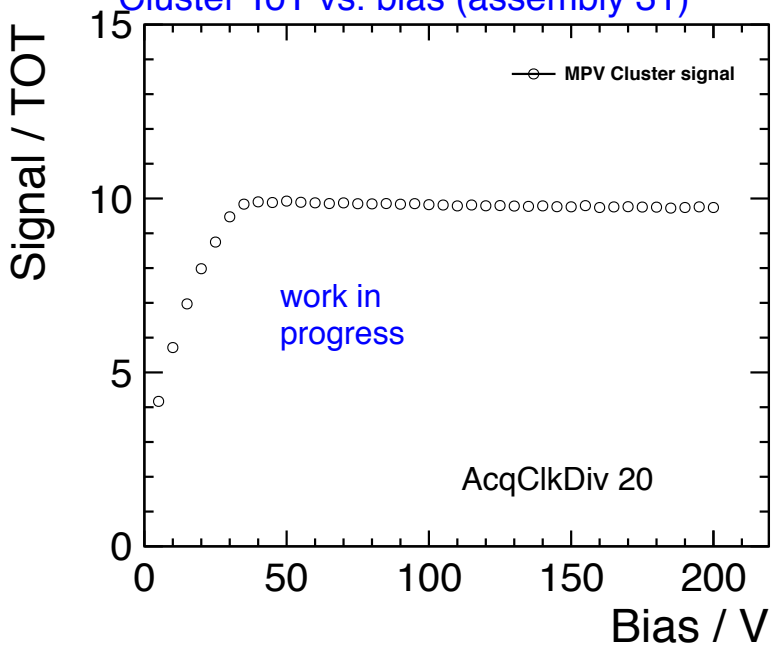
Cluster ToT (assembly 31)



Seed-pixel energy (ToT) (assembly 31)



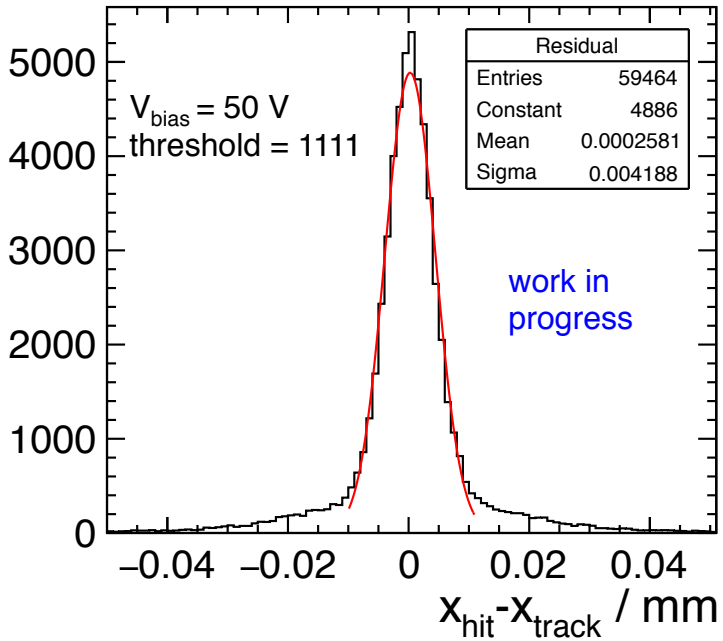
Cluster ToT vs. bias (assembly 31)



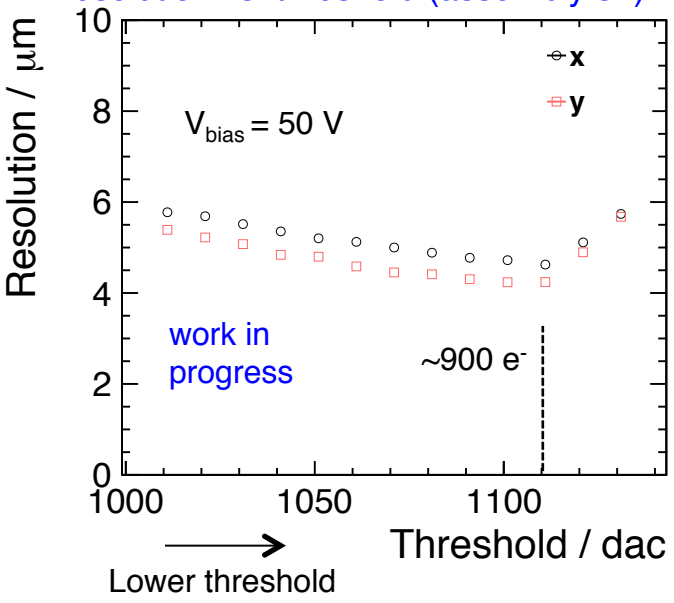
Resolution

- DUT hit position reconstructed using eta correction based on measured ToT response of pixels within cluster
- Resolution from fitted residuals of reconstructed hit positions w.r.t. track intercepts
- Telescope track resolution of ~1.6 µm not unfolded
- Optimal resolution ~4 µm for low threshold and for bias voltage close to depletion
- For very low threshold: noise increase worsens resolution
- For very high bias: reduced charge sharing worsens resolution

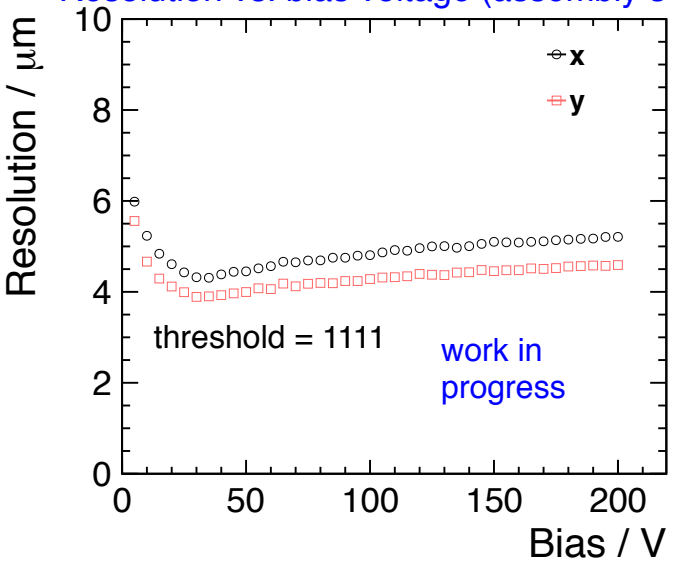
Residuals in row direction (assembly 31)



Resolution vs. threshold (assembly 31)



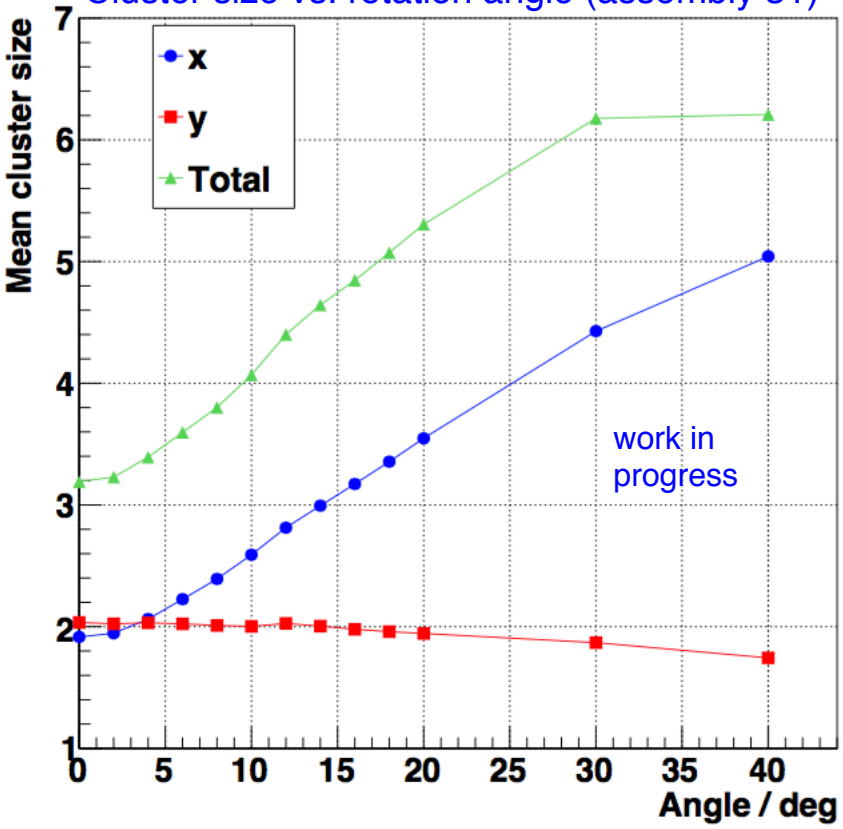
Resolution vs. bias voltage (assembly 31)



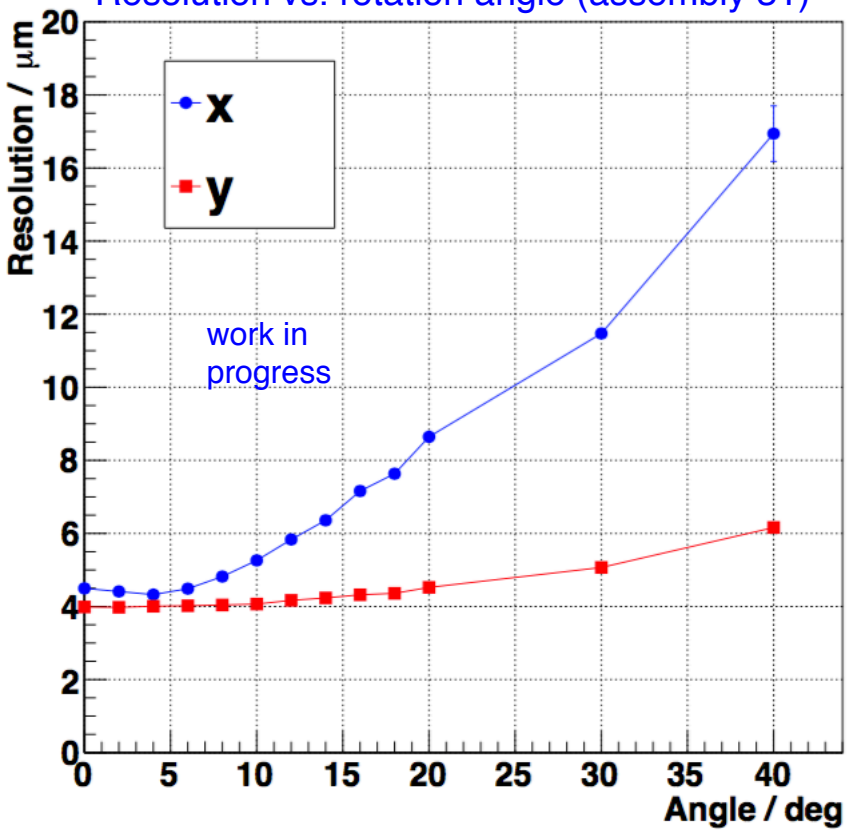
Rotation scans

- Took data with DUT rotated around x-axis: 0 degree to 80 degree
- Bias scans at each rotation angle
- As expected: cluster width increases with rotation
- Slope sensitive to depleted depth
  → possibility to extract depletion voltage from bias scan at each angle
- Analysis ongoing

Cluster size vs. rotation angle (assembly 31)



Resolution vs. rotation angle (assembly 31)



CLICpix2

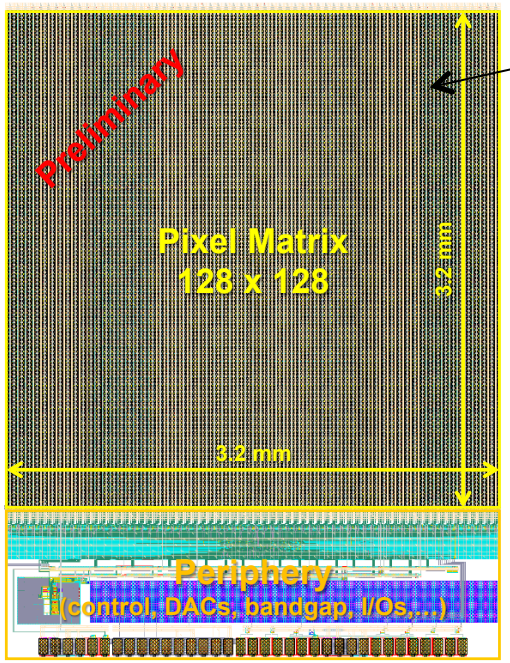
New CLICpix2 readout ASIC

- Larger pixel matrix of 128x128, 25 µm pitch
- Increased counter depth:
  - 8 bit ToA / event counting (instead of 4)
  - 5 bit ToT (instead of 4)
  - Combined mode: 13 bit ToA
- band-gap (RD53 collaboration)
- Faster readout (640 Mbit/s serializer)
- Bug fixes and general performance improvements

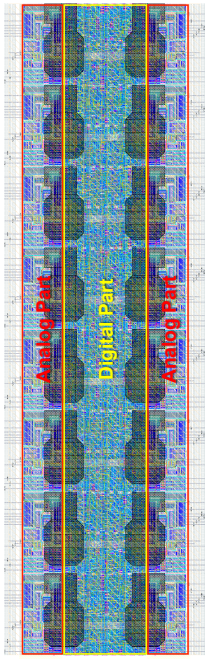
- Design almost completed
- system-level verification ongoing
- Submission till end 2015

- Sensors already produced (previous MPWs): Micron, Advacam active edge

CLICpix2 layout



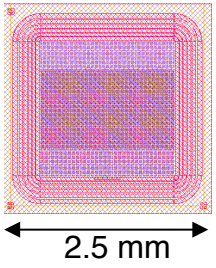
2x8 superpixel



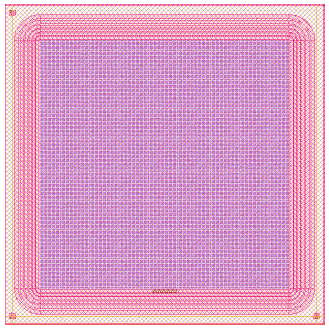
~90% fill factor!

P. Valerio, E. Santin

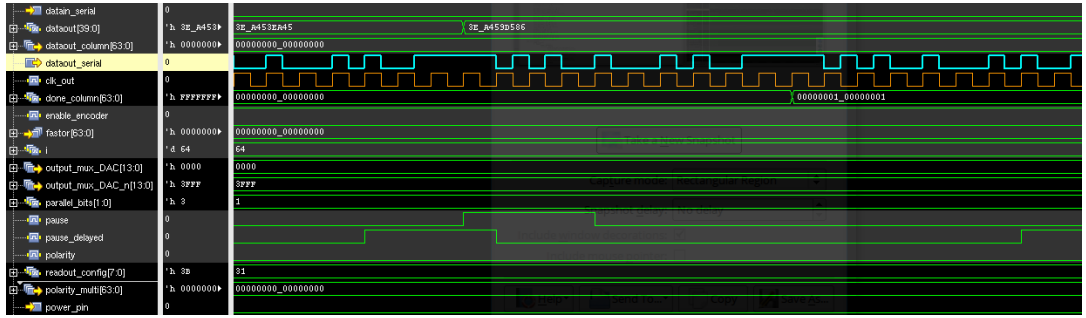
CLICpix sensor 64x64



CLICpix2 sensor 128x128



Simulation 640 Mbit/s DDR serializer

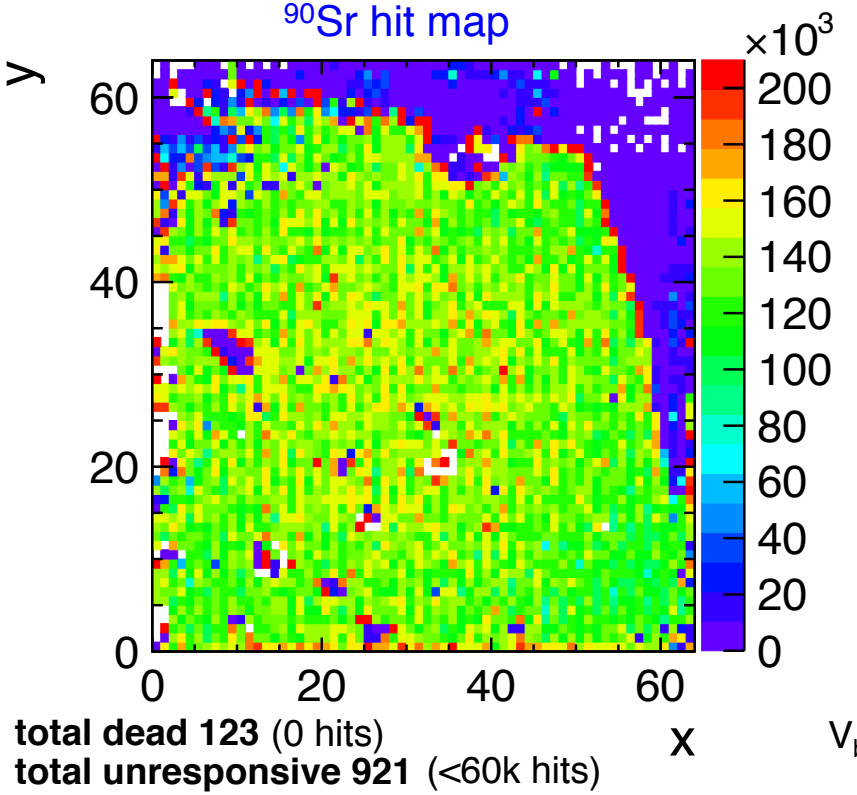


Summary

- Developed flip-chip process for CLICpix planar-sensor assemblies
- Produced three test assemblies with 200 µm thick sensors
- Lab measurements show reasonable interconnect yield and good uniformity of pixel response
- Preliminary test-beam results show very good performance:
  - >99.5% efficiency for connected pixels
  - ~4 µm hit resolution
- New CLICpix version with larger pixel array and improved performance soon to be submitted for production

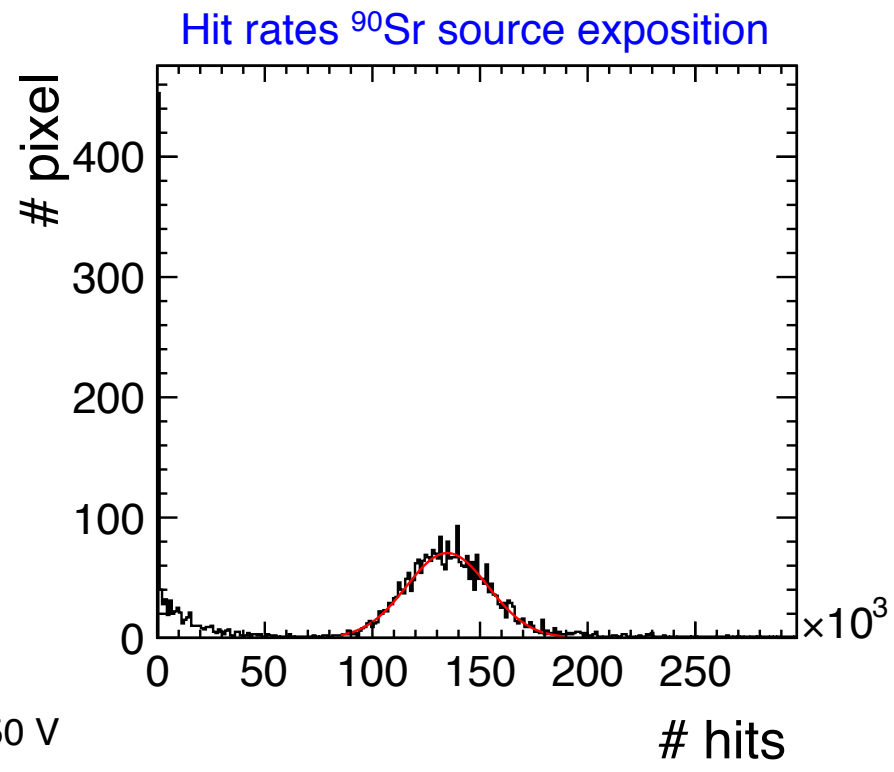
Additional material

Source response assembly 43



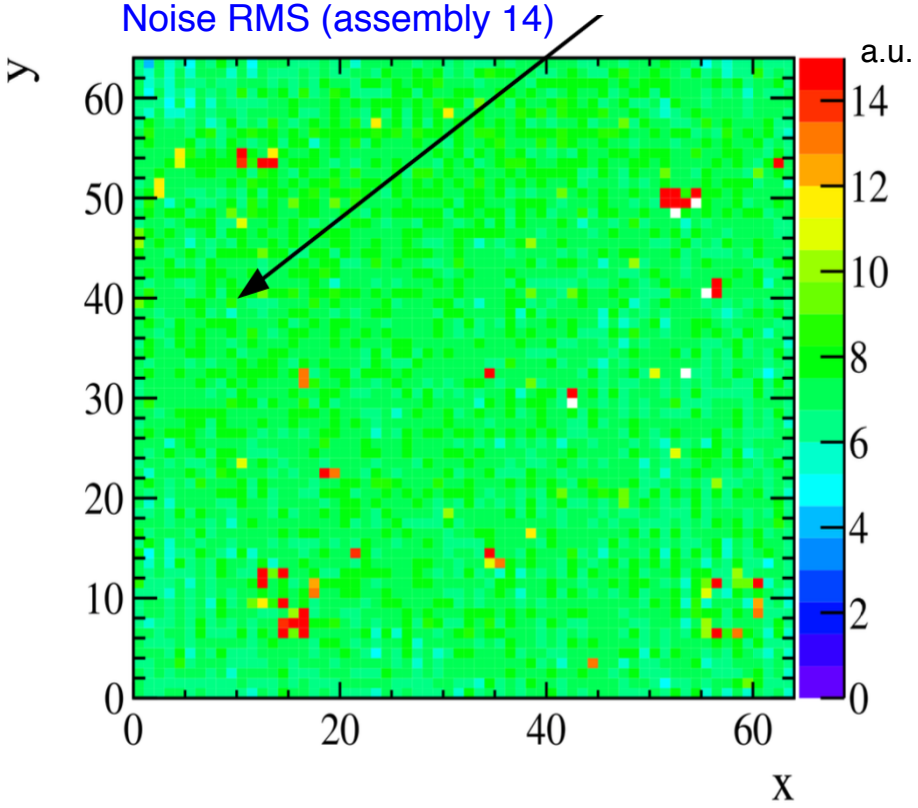
total dead 123 (0 hits)
total unresponsive 921 (<60k hits)

V_{bias}=-50 V

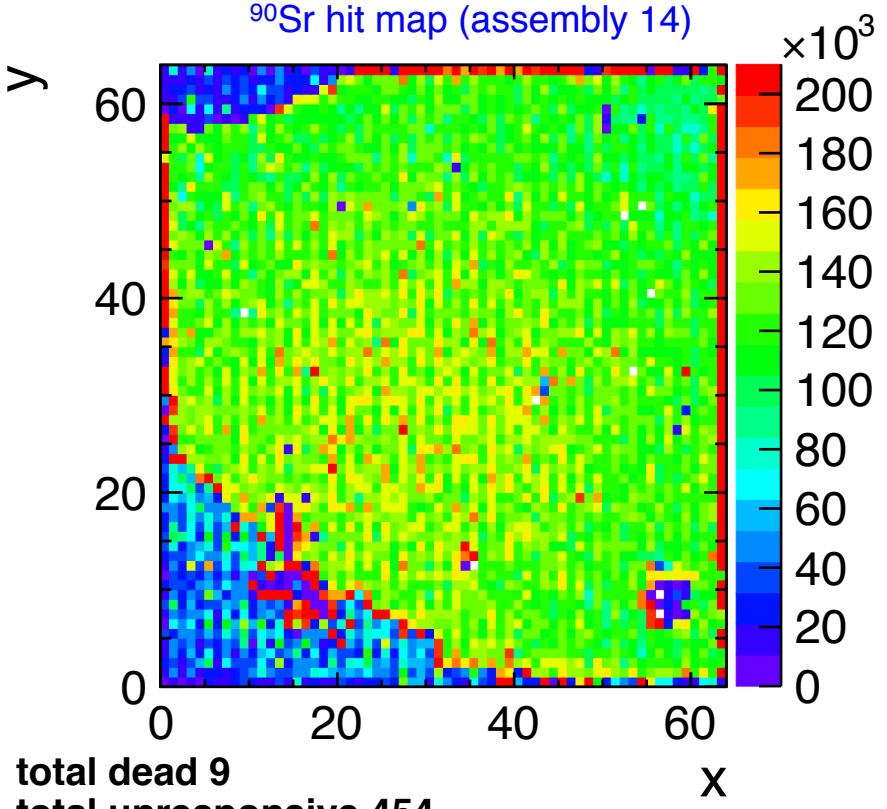


Lab results assembly 14

Noise RMS (assembly 14)



^{90}Sr hit map (assembly 14)



total dead 9
total unresponsive 454

V_{bias}=-50 V

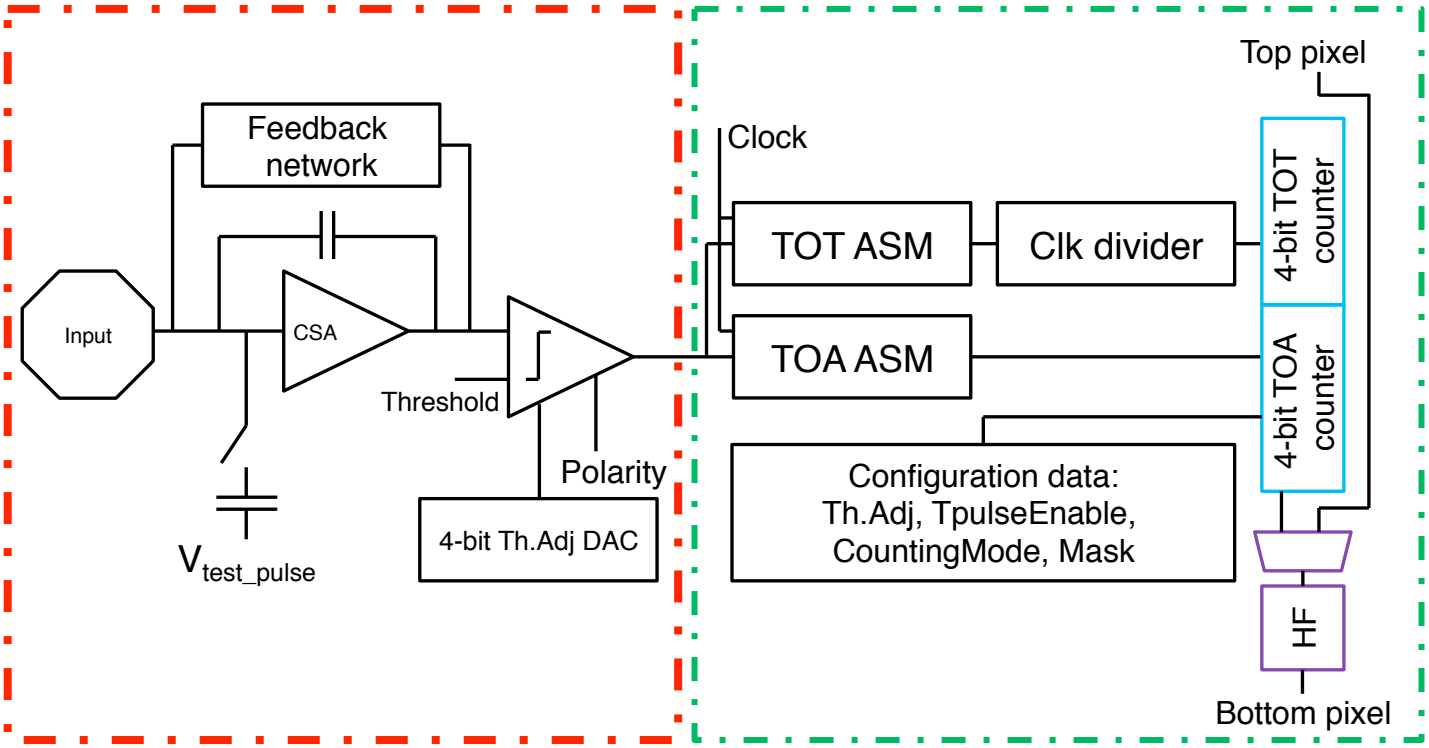
Medipix/Timepix hybrid r/o chip family

Chip	Year	CMOS Process	Pitch [μm²]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm	55x55	∫ToT or ToA or γ counting	Sequential (full frame)	HEP (TPC)
Medipix3RX	2012	130 nm	55x55	γ counting	Sequential (full frame)	Medical
CLICpix demonstrator	2013	65 nm	25x25	ToT + ToA	Sequential (data comp.)	Test chip with 64x64 pixel matrix
Timepix3	2013	130 nm	55x55	ToT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
Velopix	2015	130 nm	55x55	ToT + ToA, γ counting + ∫TOT	Data driven	LHCb (10x Timepix3 rate)
Smallpix/ Timepix4	2016	65 nm (t.b.c.)	~35x35	ToT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
CLICpix	tbd	65 nm	25x25	ToT + ToA	Sequential (data comp.)	CLIC vertex detector

ToT: Time-over-Threshold
→ Energy
ToA: Time-of-Arrival
→ Time

- Taking advantage of smaller feature sizes:
  - Increased functionality and/or
  - Reduced pixel size
  - Improved noise performance

CLICpix pixel architecture



- The analog front-end shapes photocurrent pulses and compares them to a fixed (configurable) threshold
- Selectable polarity (positive / negative signals)
- Digital circuits simultaneously measure Time-over-Threshold and Time-of-Arrival of events and allow for zero-compressed readout

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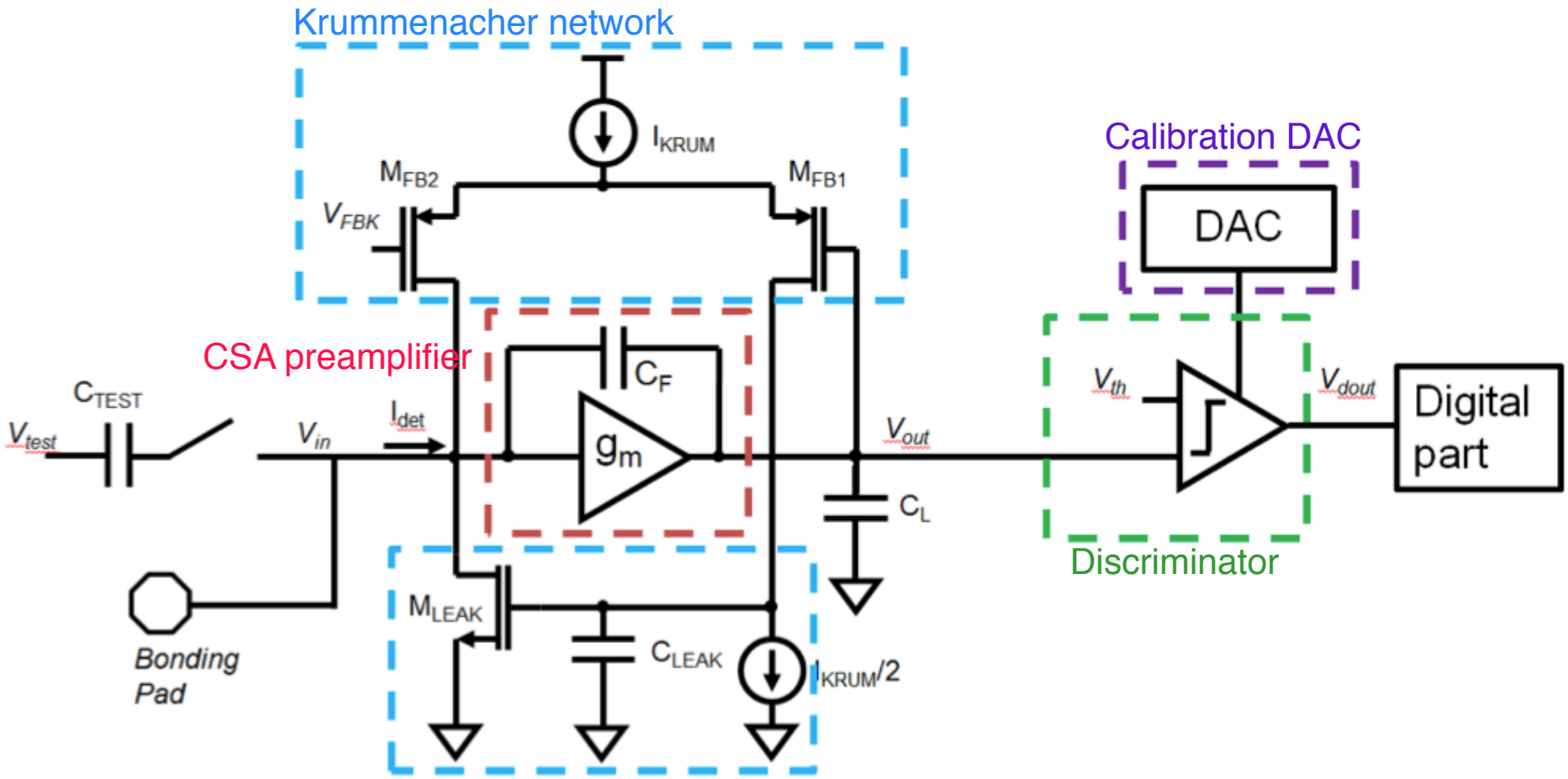
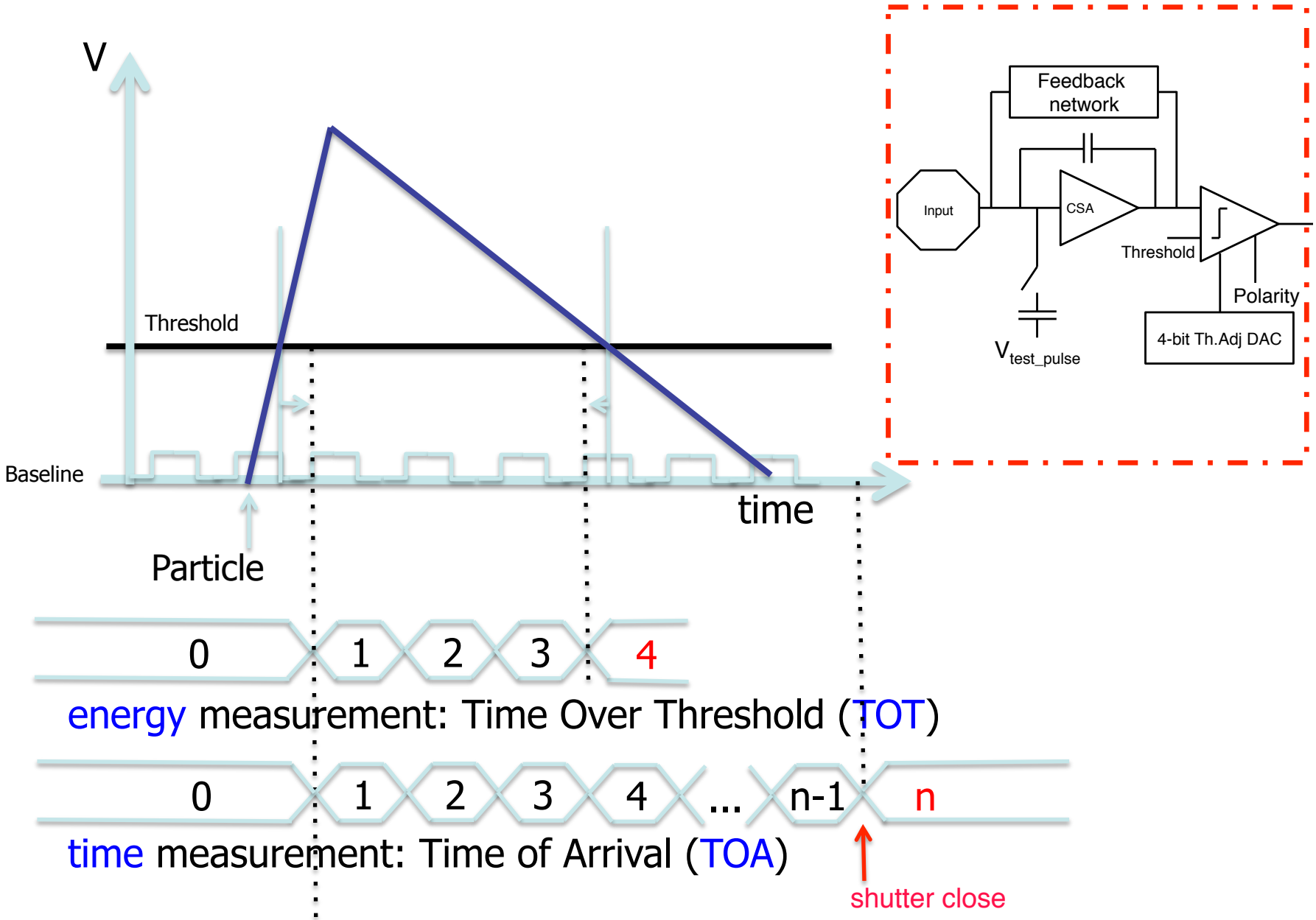
CLICpix analog frontend

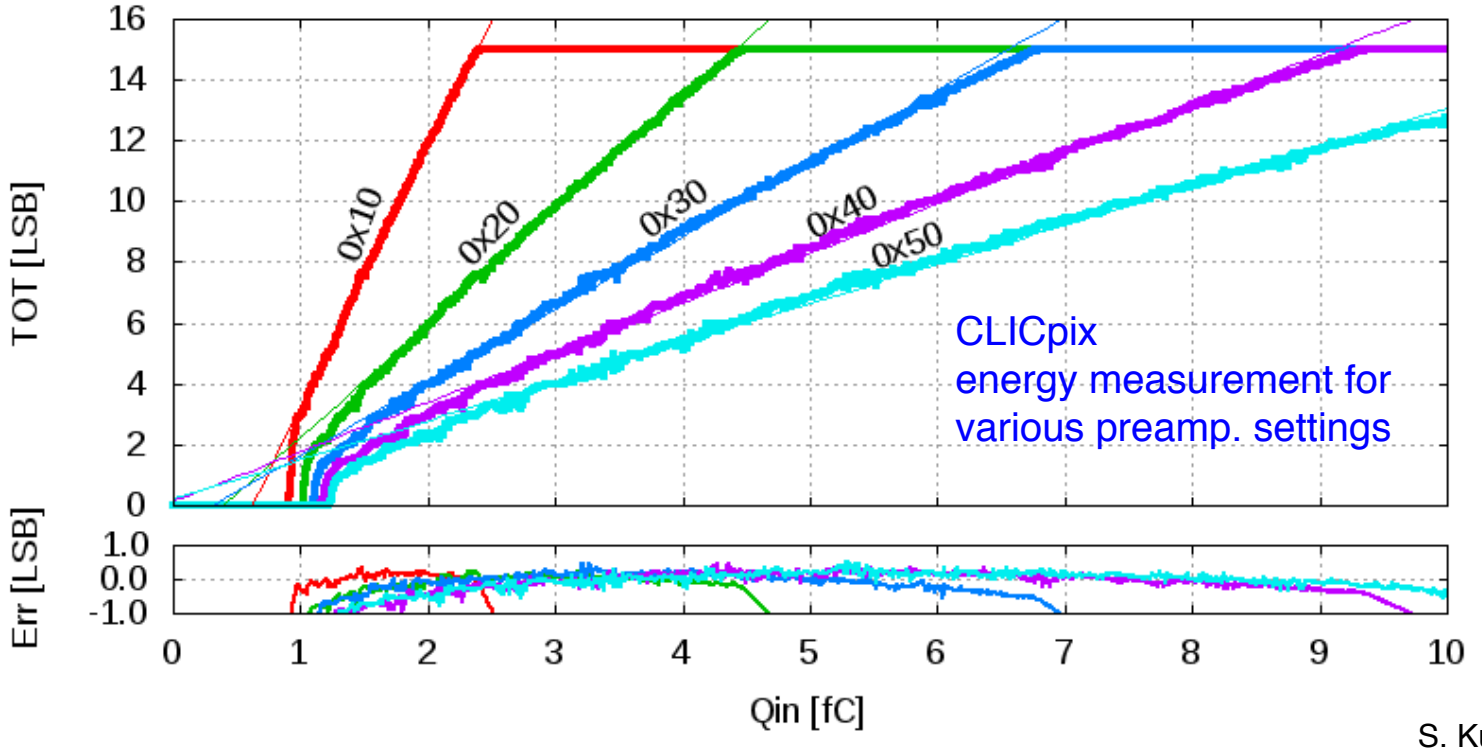


CLICpix: time and energy measurement



CLICpix: energy measurement

- Measure charge released in each pixel
  → Improve position resolution through interpolation
- Time-Over-Threshold (TOT) measurement (4-bit precision)
- Calibration measurement using external test pulser:



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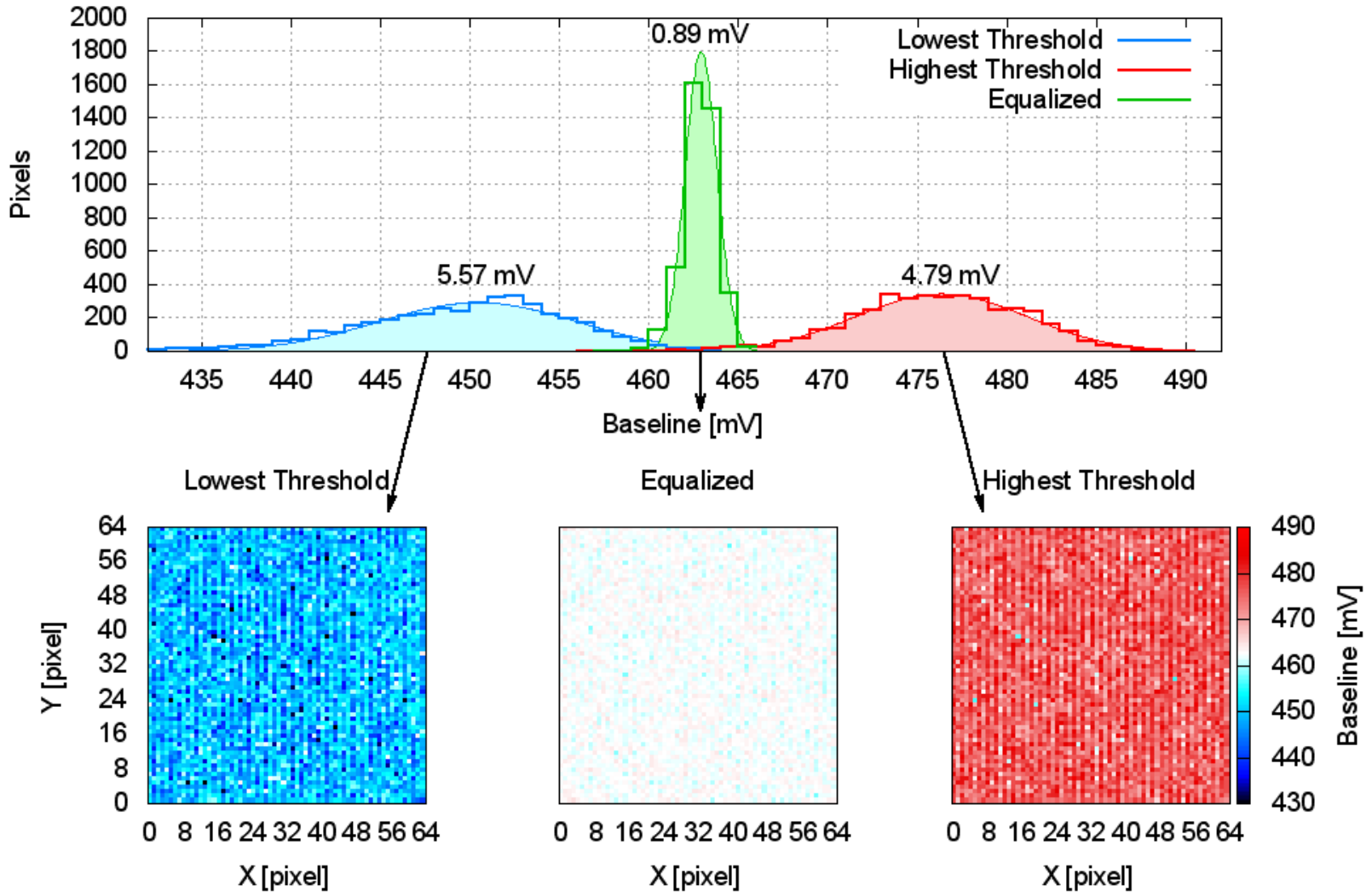
CLICpix: baseline equalization



Calibrated spread across the whole matrix is 0.89 mV RMS (~22 e^-)
For comparison: MIP signal in 50 µm silicon ~3700 e^-

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CLICpix2 analog FE requirements

Parameter	Value
Power dissipation	< 12 μW
Area	< 12x25 μm^2
Input charge	4 ke- average, 40 ke- maximum
Minimum threshold	~ 600 e-
Equivalent input noise	~ 70 e-
ToT dynamic range	up to 40 ke-
ToA accuracy	< 10 ns
Total ionizing dose robustness	1 Mrad
Input charge types	electrons & holes
Testability	in-pixel test pulse generator

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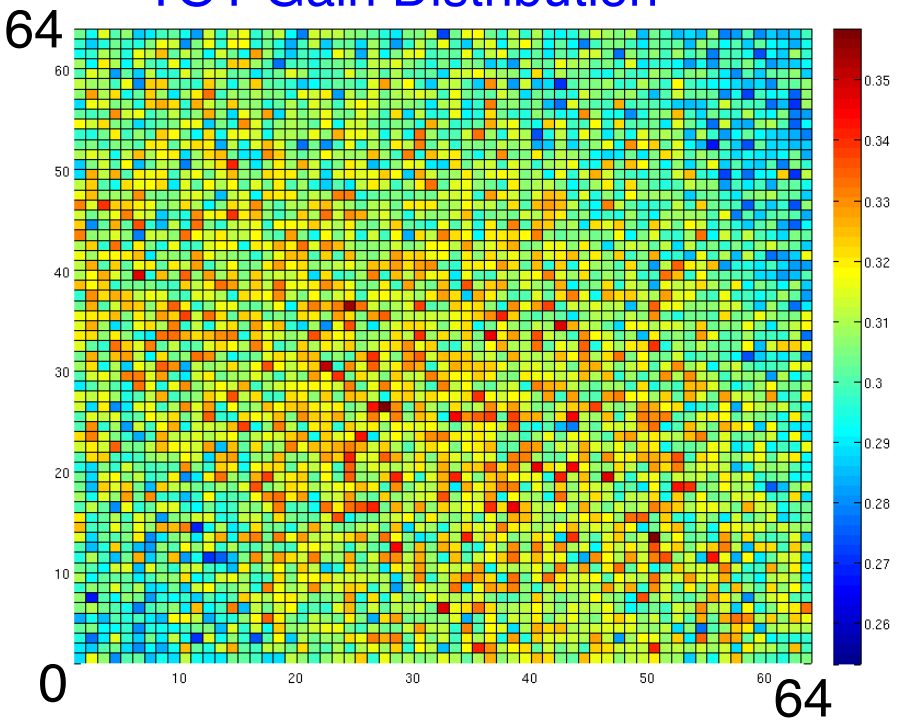
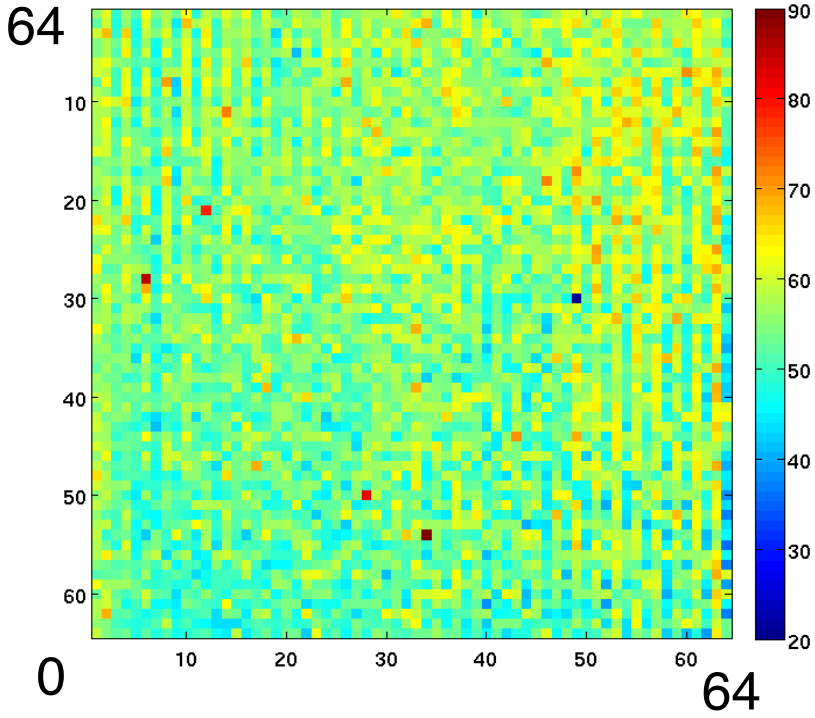
CLICpix: uniformity of gain and noise

TOT Gain Distribution



- Uniform gain across the matrix
- Gain variation ~4.2% r.m.s. (for nominal feedback current)

Equivalent Noise Charge

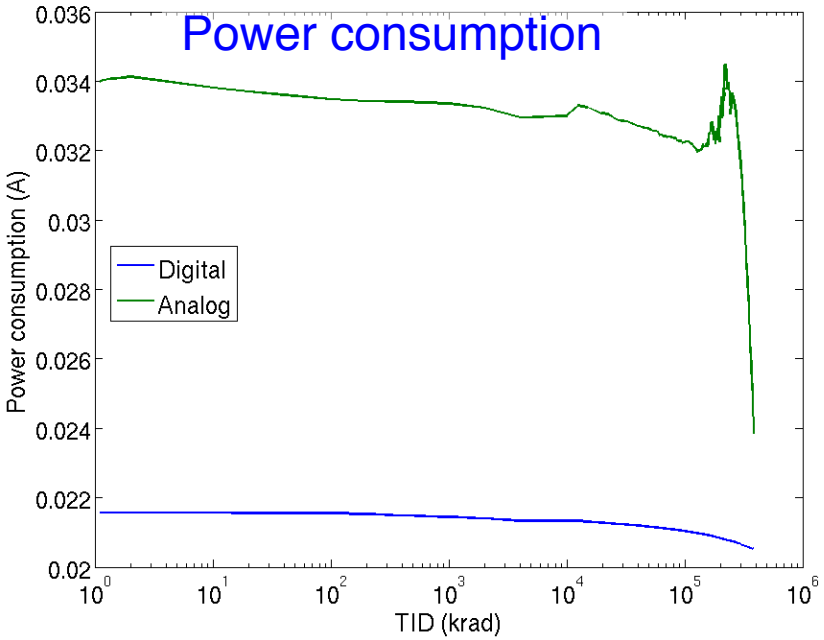


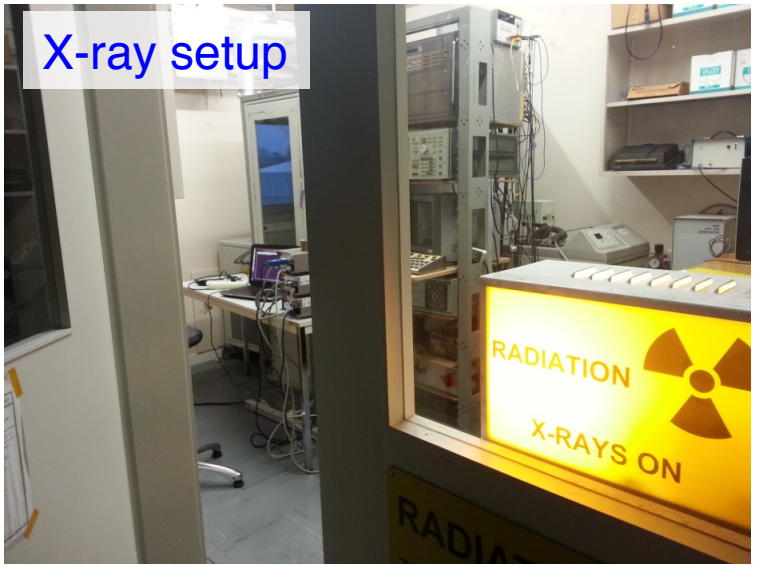
- Uniform ENC across the matrix
- Mean ENC: 55 e^-, SD: 5.7 e^- (without sensor)

CLICpix: radiation qualification

- Moderate radiation-tolerance requirements at CLIC: <100 kRad TID
- However: building blocks can be re-used for RD53 (~1 GRad required)
- Results of radiation testing useful for gaining deeper understanding of the chip

→ performed radiation test up to 1 GRad (up to 150 kRad/minute) in calibrated X-ray setup





- No significant changes observed in sub-MRad range relevant for CLIC
- For >250 MRad: PMOS switches in current mirror fail

→ Break-down of analog power (note: band gap foreseen for final chip, instead of current mirror)

- digital components kept working normally

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