Development of a pixel sensor based on SOI technology for the ILC vertex detector

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Contents

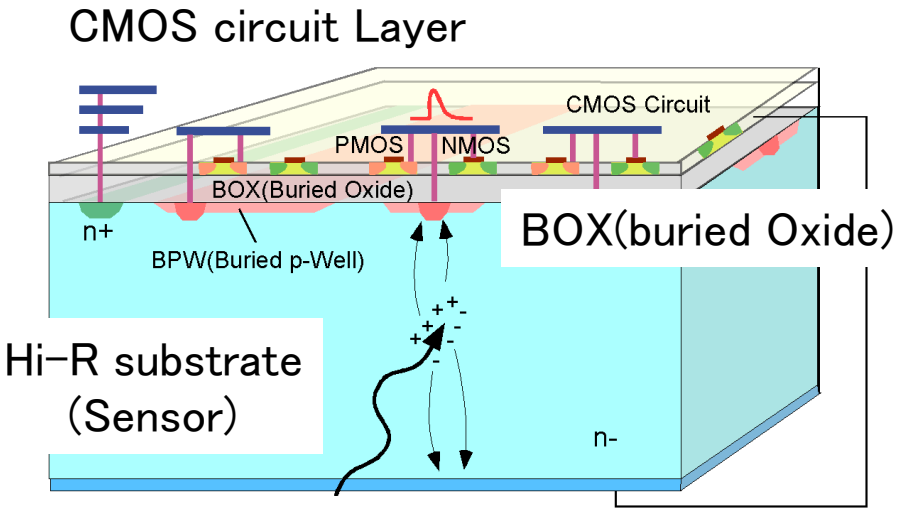
- SOI (Silicon-On-Insulator) Pixel detector
- SOFIST: SOI sensor for ILC vertex detector
  - Sensor specification and design
  - Pixel with fine position and timing resolutions
  - Technical issues
- Development of prototype sensor
  - Schedule
  - Sensor design and simulation
- Next development

SOI pixel detector

- Monolithic pixel detector by SOI technology

- SOI wafer consists of silicon substrate, Si02 layer, and top Si layer.
- The circuit has lower stray capacitance due to isolation from silicon substrate.
- Substrate layer can be used as depleted silicon sensor.

SOI pixel detector



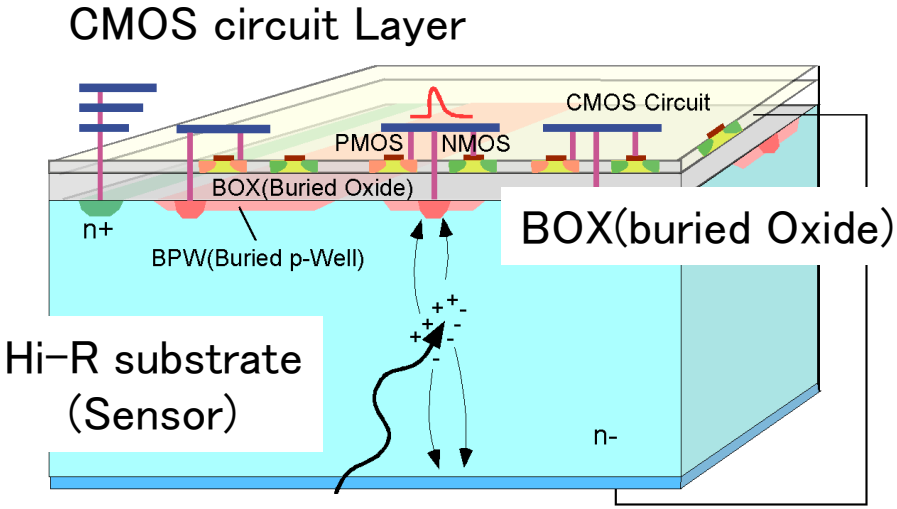
SOI pixel detector

- Monolithic pixel detector by SOI technology

SOI detector advantages

- Smaller pixel
- Low material thickness
- Low stray capacitance

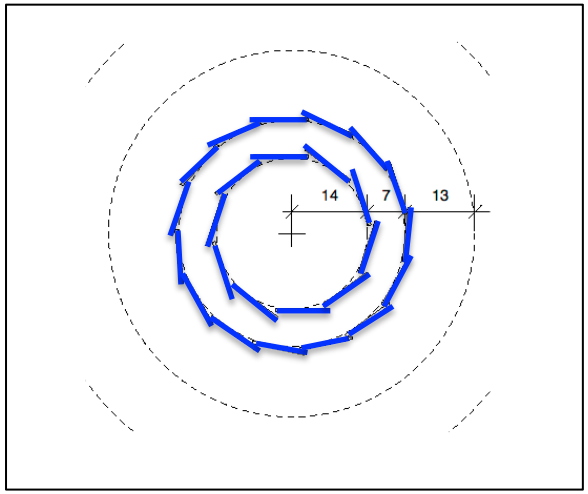
SOI pixel detector



SOI detector fulfill the requirement
of vertex detector for particle physics experiments.

Sensor requirement for ILC vertex detector

- We are developing pixel detector optimized for ILC with SOI pixel sensor
  - ➢ Innermost and second layers of vertex detector



Sensor position resolution

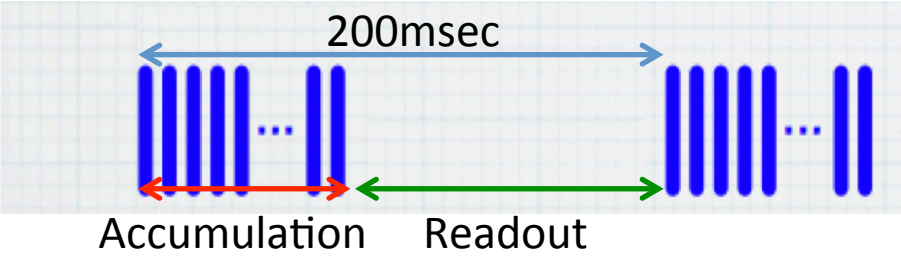
- Resolution of the decay vertex : < 5μm
  - ➢ Pixel size: 20x20 μm^2
    - Calculating hit position weighted from the charge signals spread to multiple pixels.
  - ➢ Sensor thickness : 50μm
    - Multiple-scattering reduction

Sensor resolution: < 3μm

Sensor specification for ILC vertex detector

High speed readout

- Signal readout between 2 bunch trains



Readout by column parallel ADC

Correct reconstruction of particle tracks

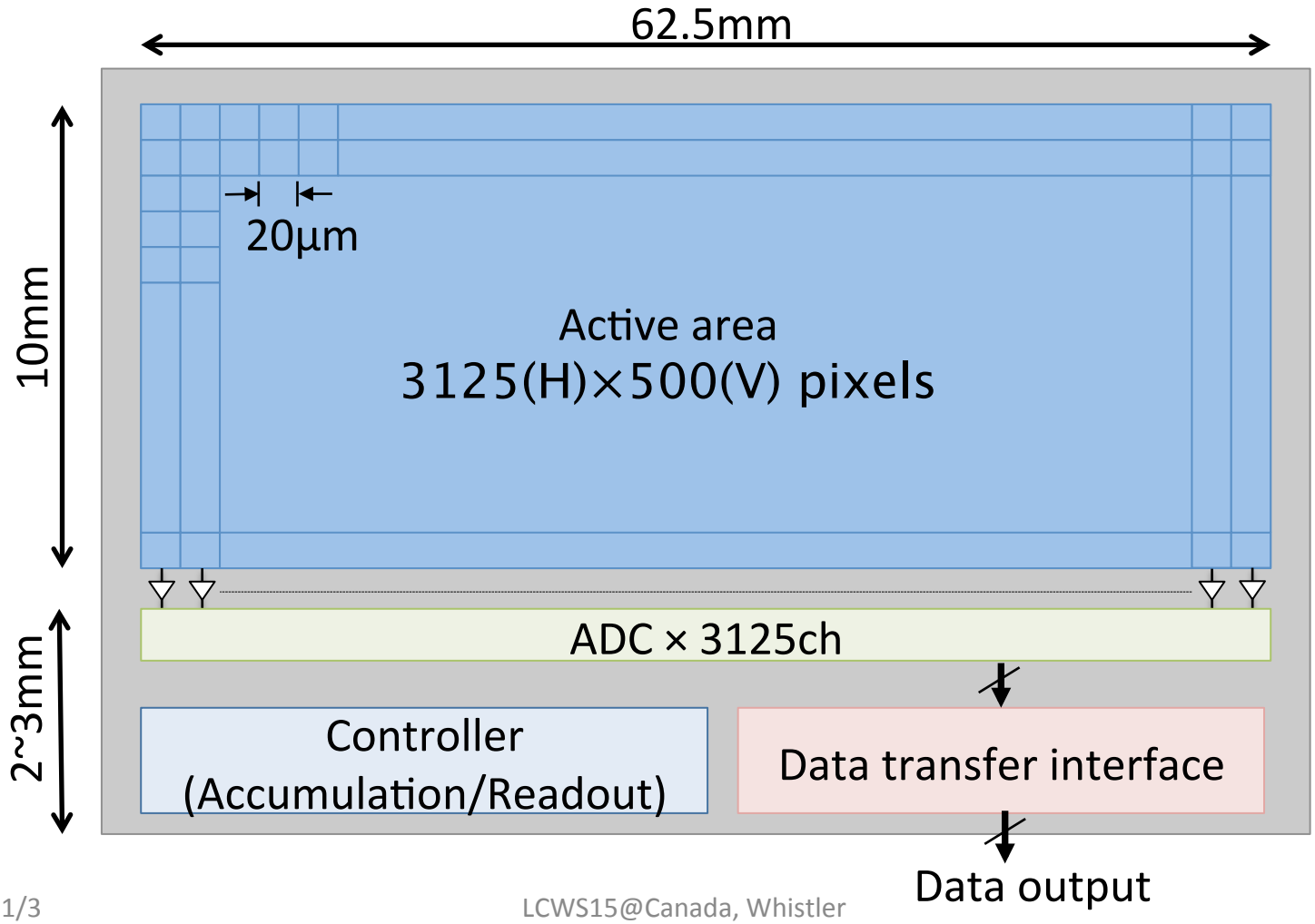
- Detector occupancy: < 2%
- Occupancy reduction
  - Separation of the events by hit timing
  - Detection of hit timing by time stamp circuits within pixel

Analog buffer and time stamp circuit in each pixel

SOI detector enables to integrate these circuits on the sensor

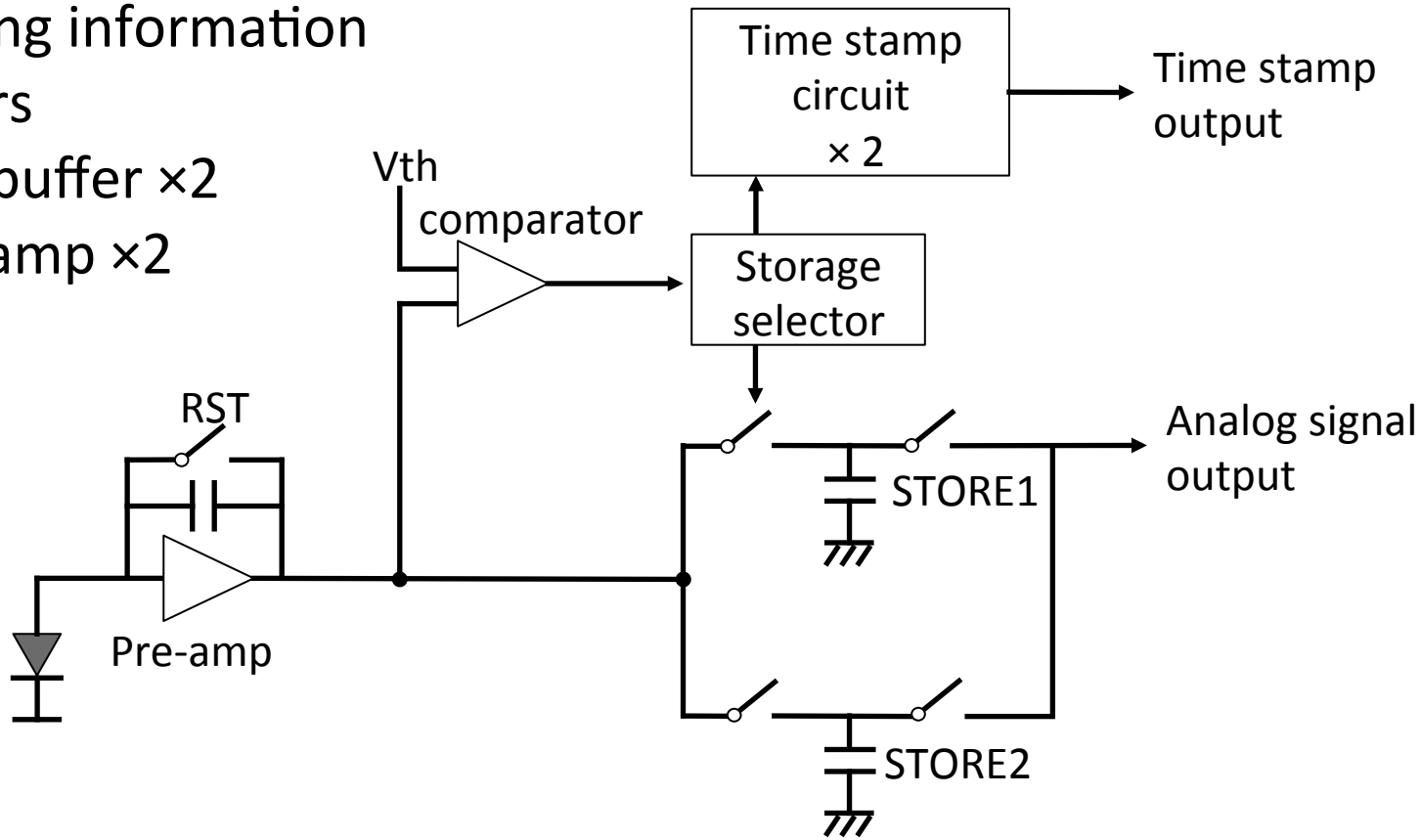
SOI sensor for ILC: SOFIST

- SOI sensor for Fine measurement of Space and Time



SOFIST pixel architecture

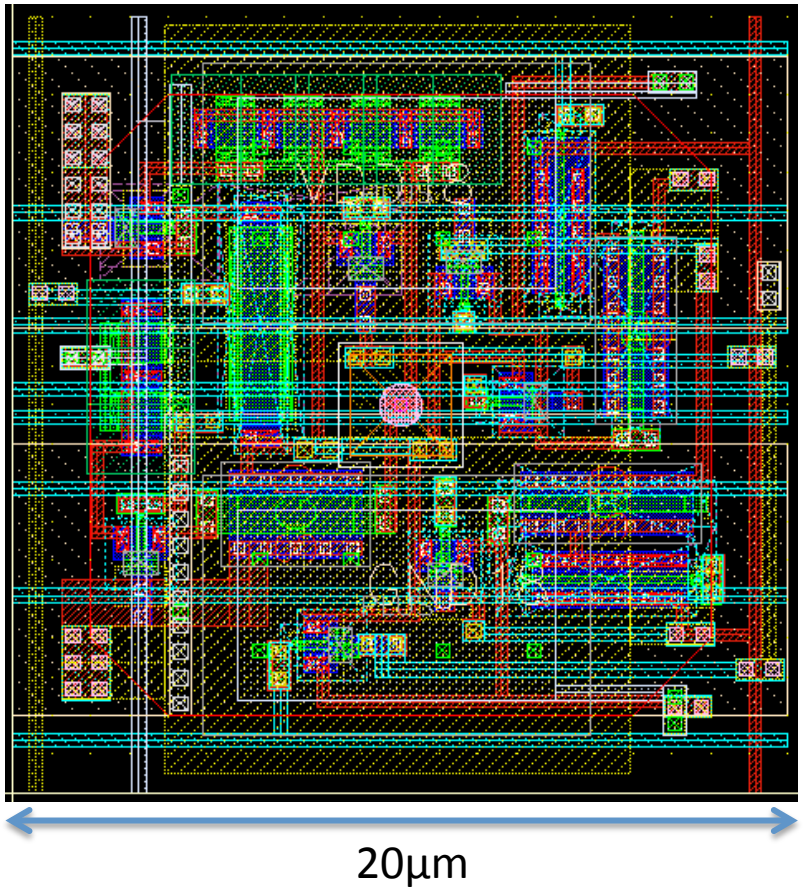
- Storage
  - Charge signal generated by particle
  - Hit-timing information
- Multi buffers
  - Analog buffer ×2
  - Time stamp ×2



Analog signal buffer × 2

Technical issues
(Layout of the pixel circuit)

- Pixel layout
  - Size: 20x20μm^2
- Internal circuits:
  - Pre-amplifier, Analog buffer ×2, Comparator, Storage selector, Time stamp ×2



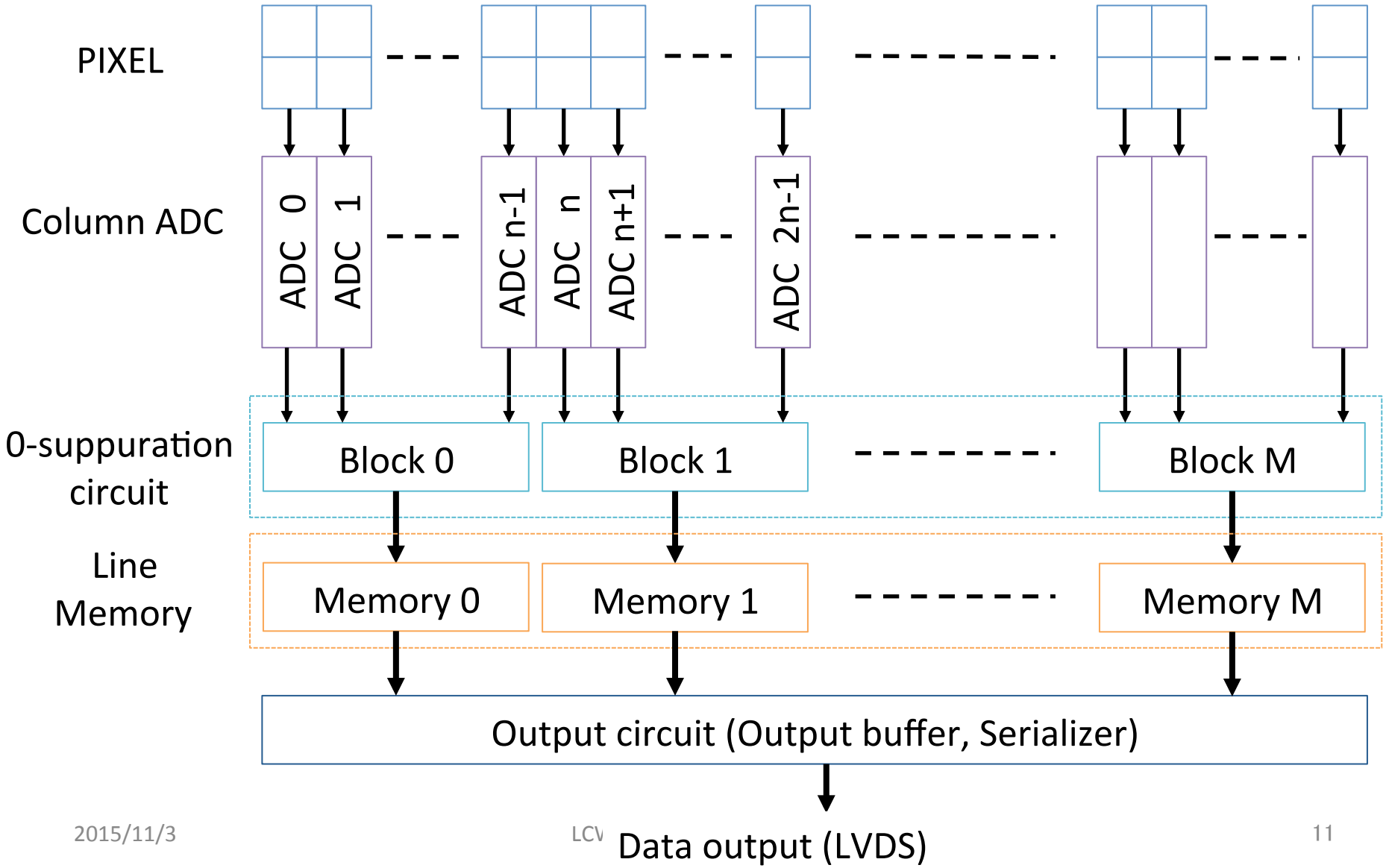
- Minimization of each circuit layout.
- Studying the 3D integration technology (stacking circuit layers)

Technical issues
(Signal readout speed)

- Data size
  - The pixel data have to be readout until next beam injection.
  - Total amount of the pixel data in SOFIST: ~50Mbit/frame

- Data compression (0-suppression)
  - Pixel data are discriminated by hit detection after ADC.
  - Only hit pixels are transferred to the backend.
  - Readout speed: 40Mbps

Pixel data stream



Development plan

- Development plan of SOFIST prototype sensor
  - Ver.1: Pixel with analog signal readout, Column-ADC circuit
  - Ver.2: Pixel with time stamp、0-suppression logic circuit
  - Ver.3: Pixel integrated both analog signal readout and time stamp.

Current status of the sensor development

SOFIST Ver.1 chip

- 2014.10~ : Start of the design
- 2015.5 : Completion of the chip design and layout
- 2015.11~ : The first prototype chip is planned to be delivered.

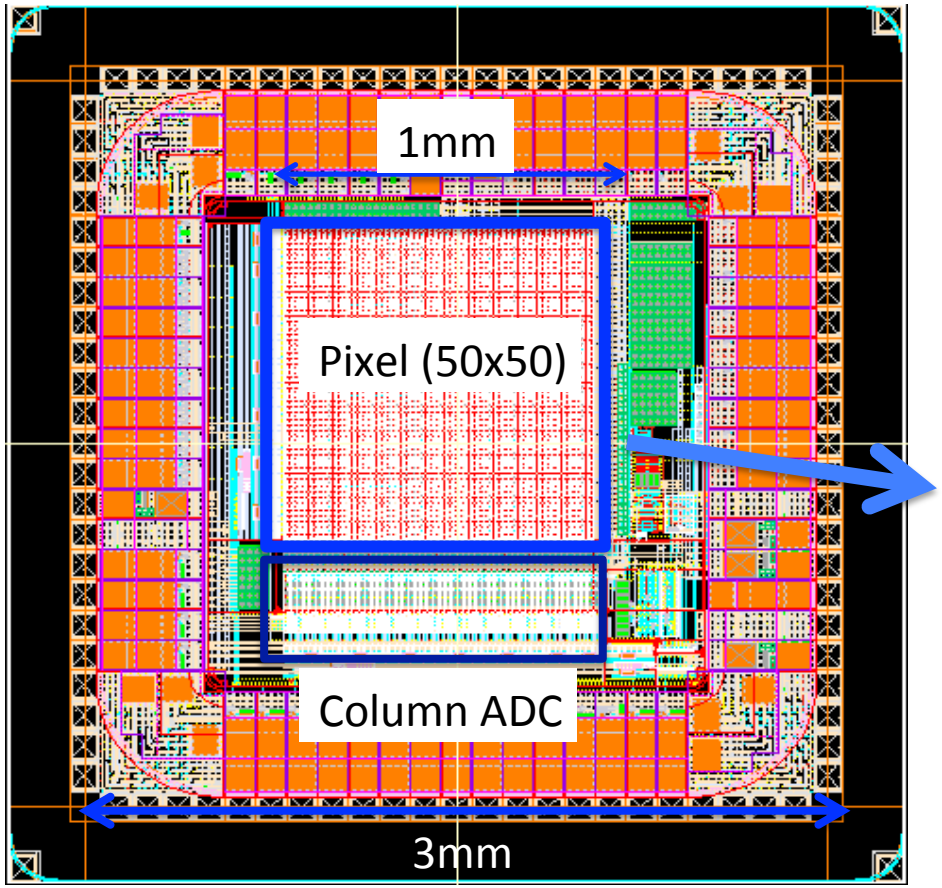
  Start of the sensor evaluation

SOFIST Ver.2 chip

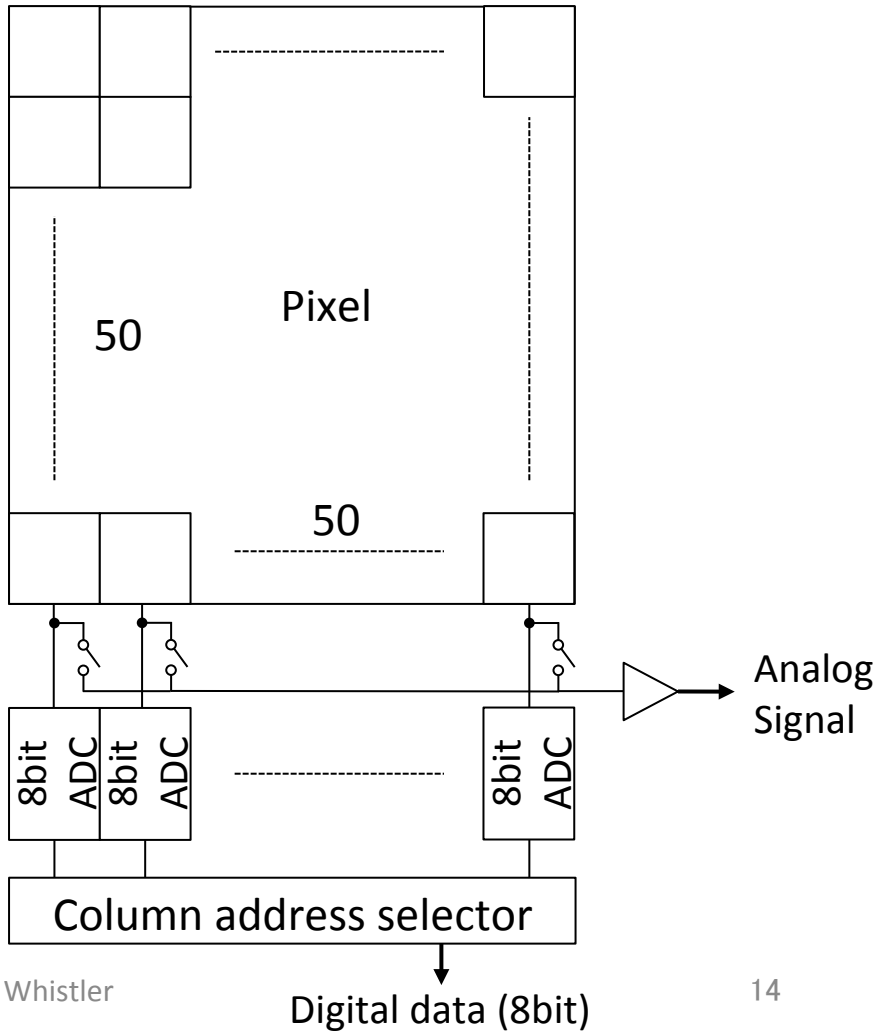
- 2015.10~ : Start of the design
- 2016.3 : Completion of the chip design and layout

SOFIST Prototype chip (Ver.1)

Prototype chip layout

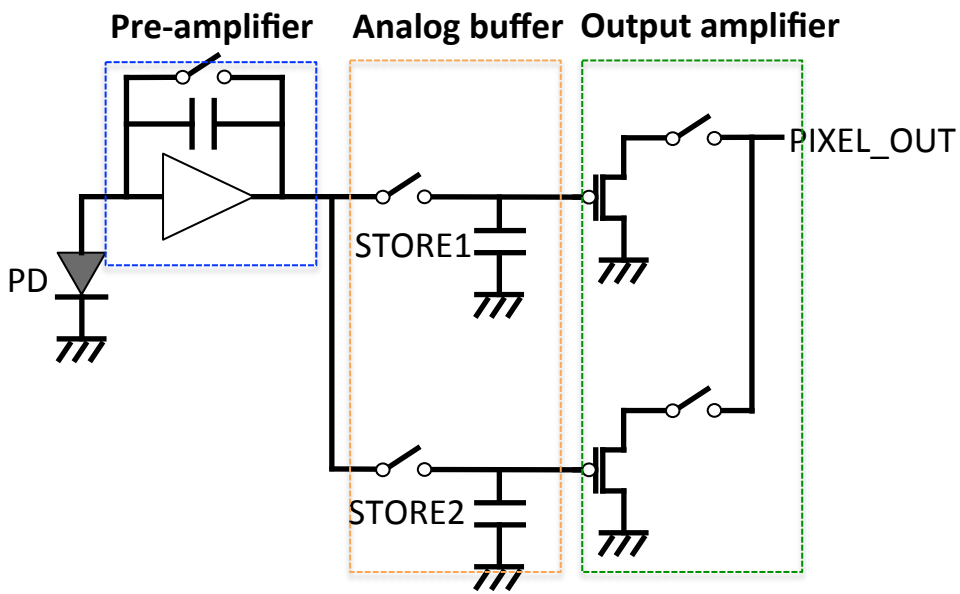


Pixel & column ADC schematic

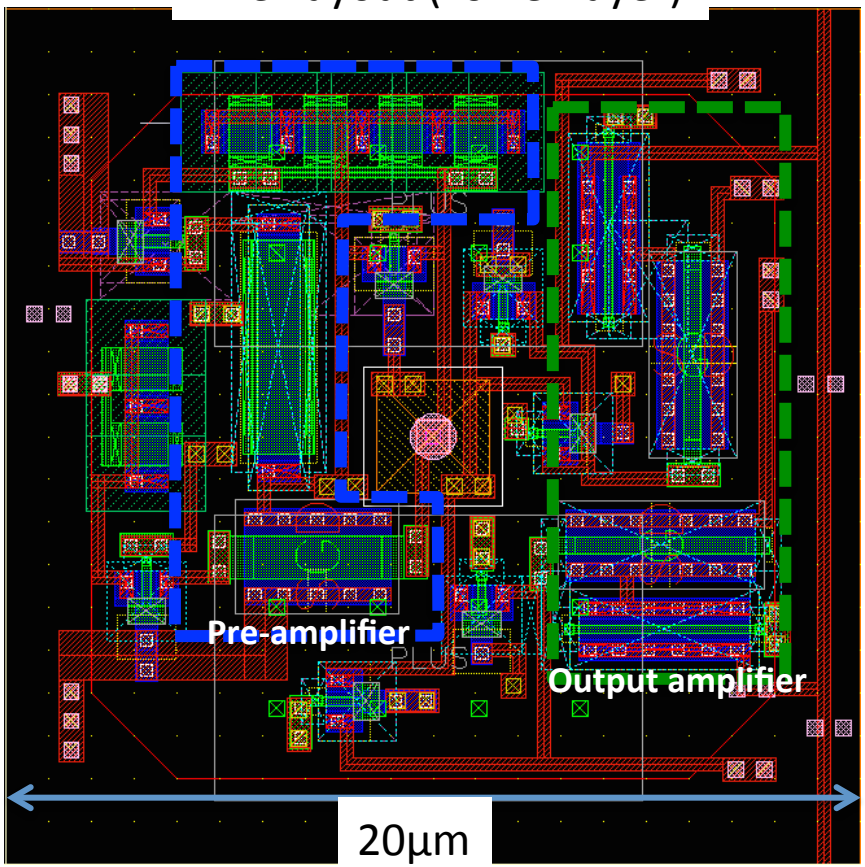


Pixel layout

- Pixel circuit schematic and layout



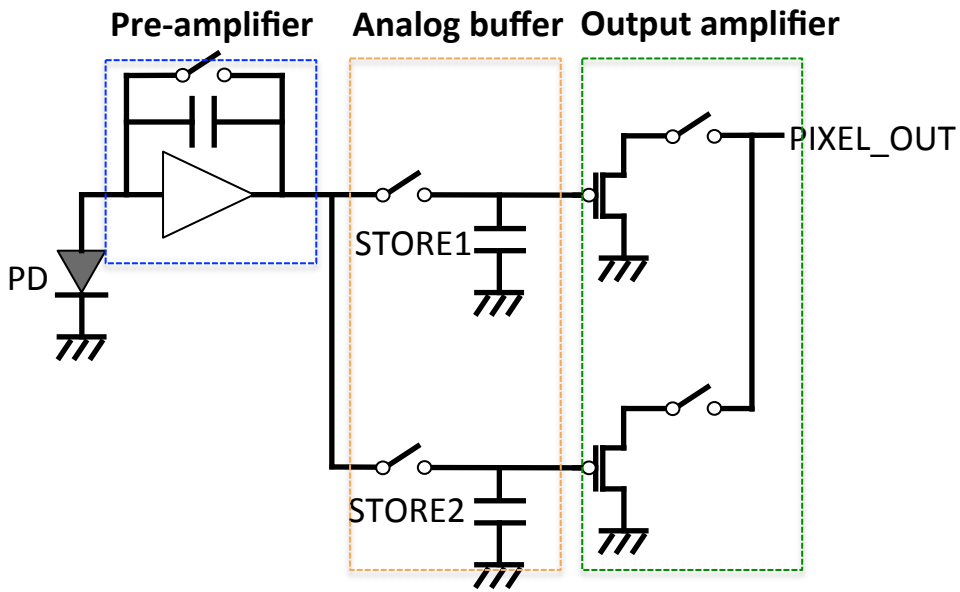
Pixel layout (Lower layer)



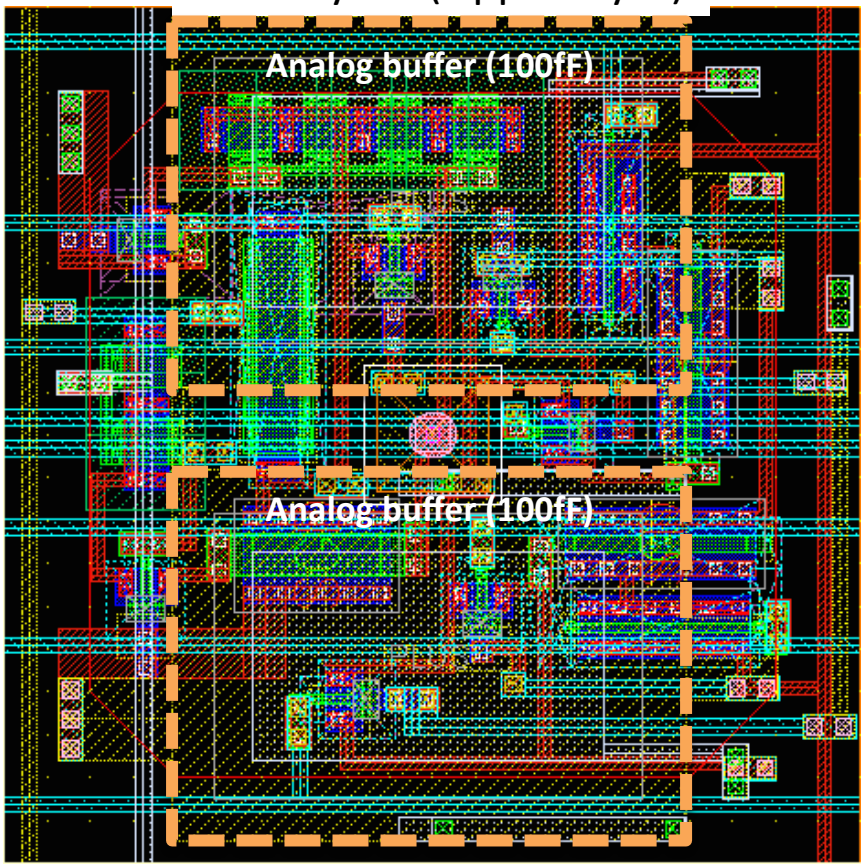
Pixel layout

- Pixel circuit schematic and layout

Two capacitors are located on the upper layer of the circuits

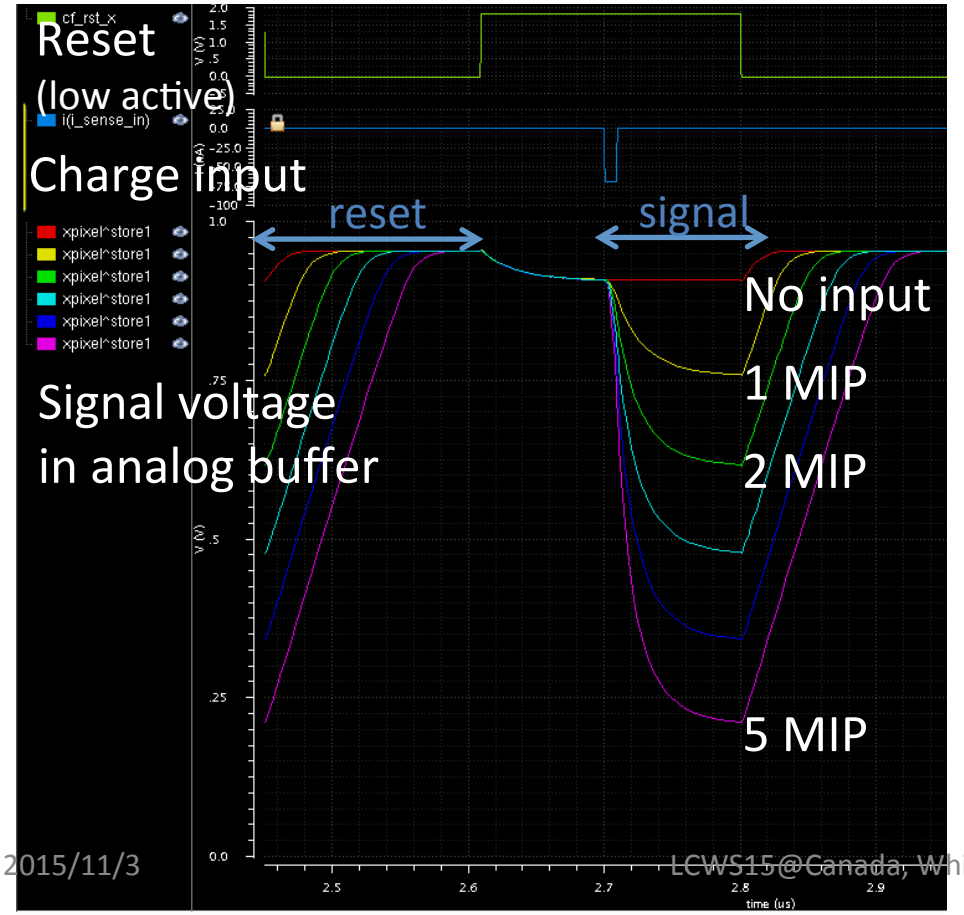


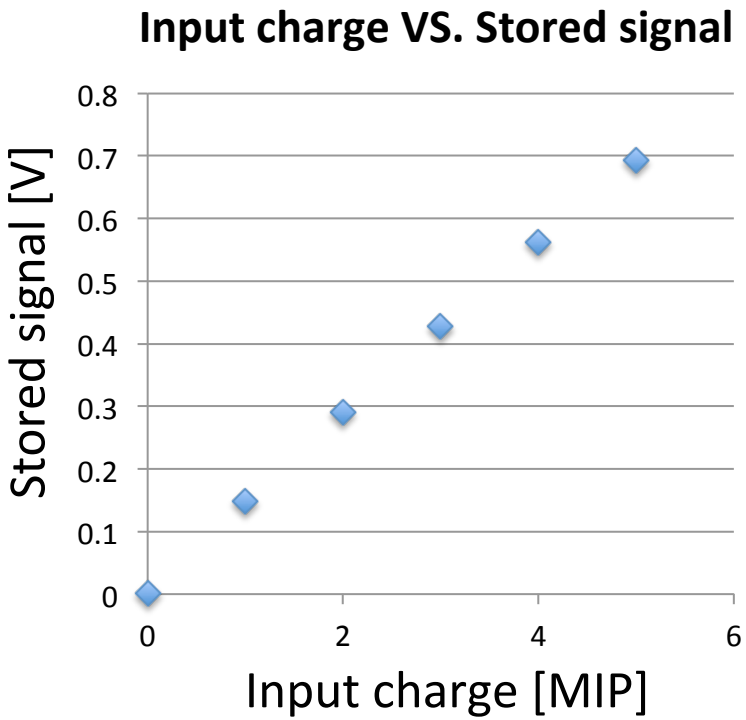
Pixel layout (Upper layer)



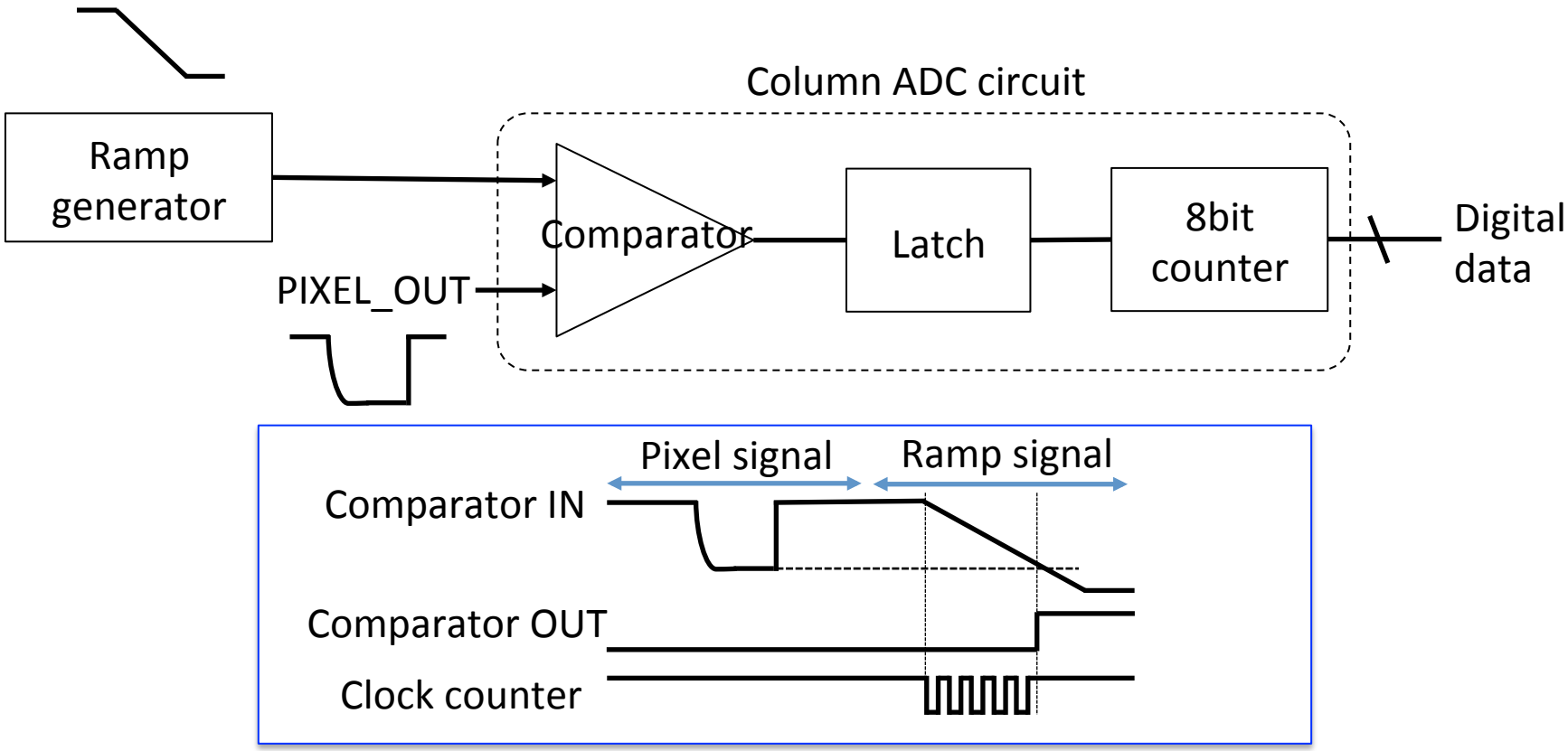
Pixel simulation

- Stored-signal simulation by charge input
  - Input charge: 0~5 MIP (0~19,000e- 1MIP = 3777e-)





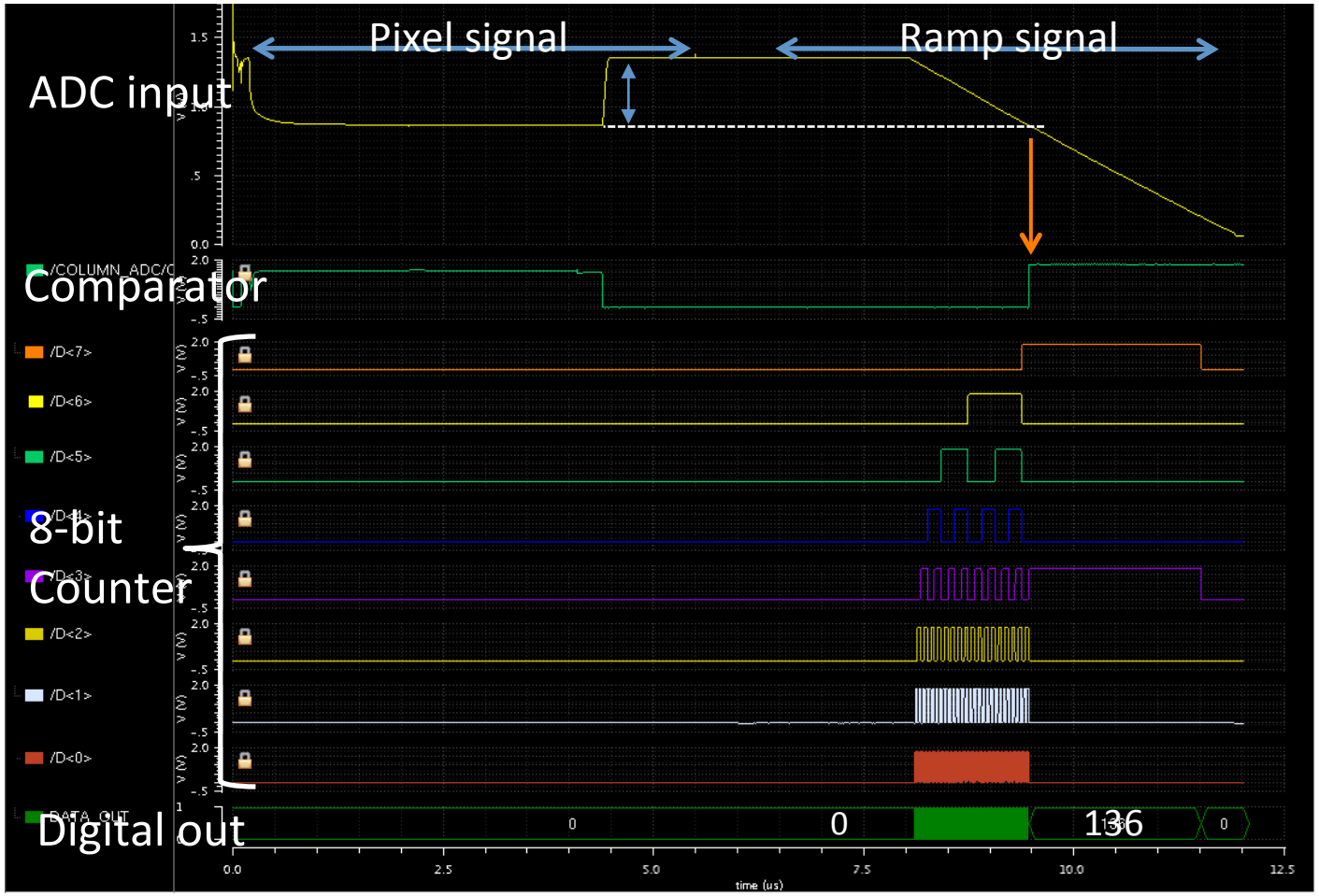
Column parallel ADC



- Input range: 1V, Output: 8bit, Resolution: 1LSB=3.9mV
- Clock: 100MHz

ADC simulation

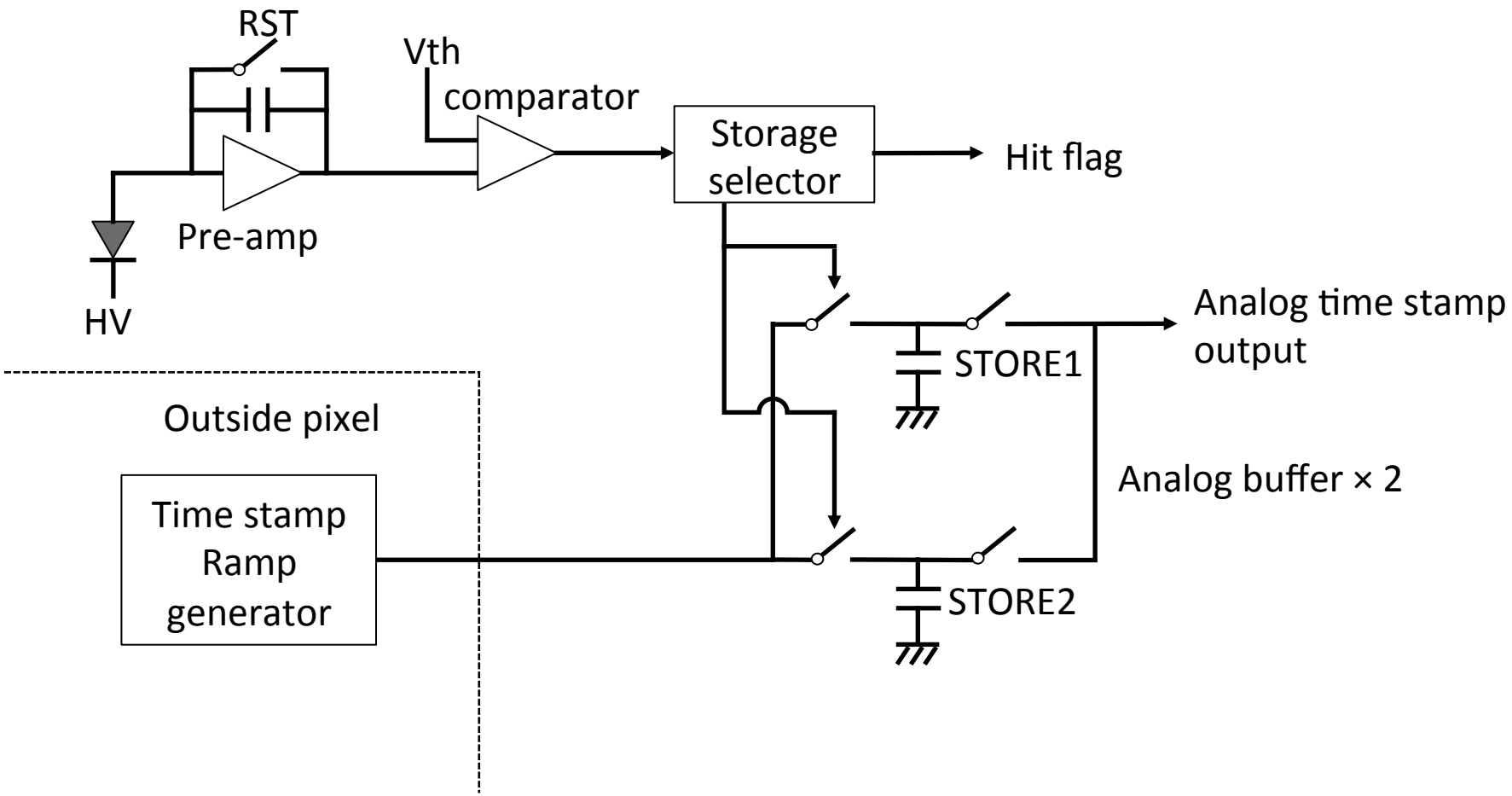
- Digital conversion result



Next development

- The development of Ver.2 chip
  - Time stamp circuit in pixel
    - Analog time-stamp (Time-to-Voltage conversion)
    - Those circuit have to be layout within 20x20um^2 pixel
  - 0-suppression logic circuit
    - Digital data processing circuit after AD conversion

Time stamp pixel



Summary

- SOFIST: SOI sensor optimized for ILC vertex detector
  - Sensor stores both position and timing of the hits in 20x20um pixel.
  - Multi-buffers in a pixel.
  - Readout by column-parallel ADC and 0-surppression logic.

- Development of first prototype sensor
  - Design of pixel with analog signal readout and column-ADC.
  - We are going to start sensor evaluation from December 2015.

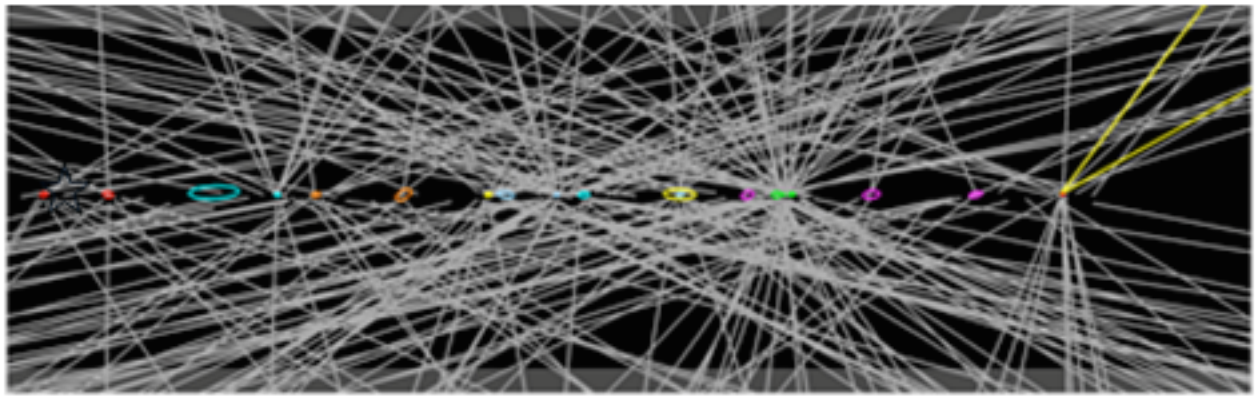
- Next development
  - Design of pixel time stamp and 0-surppression logic.

backup

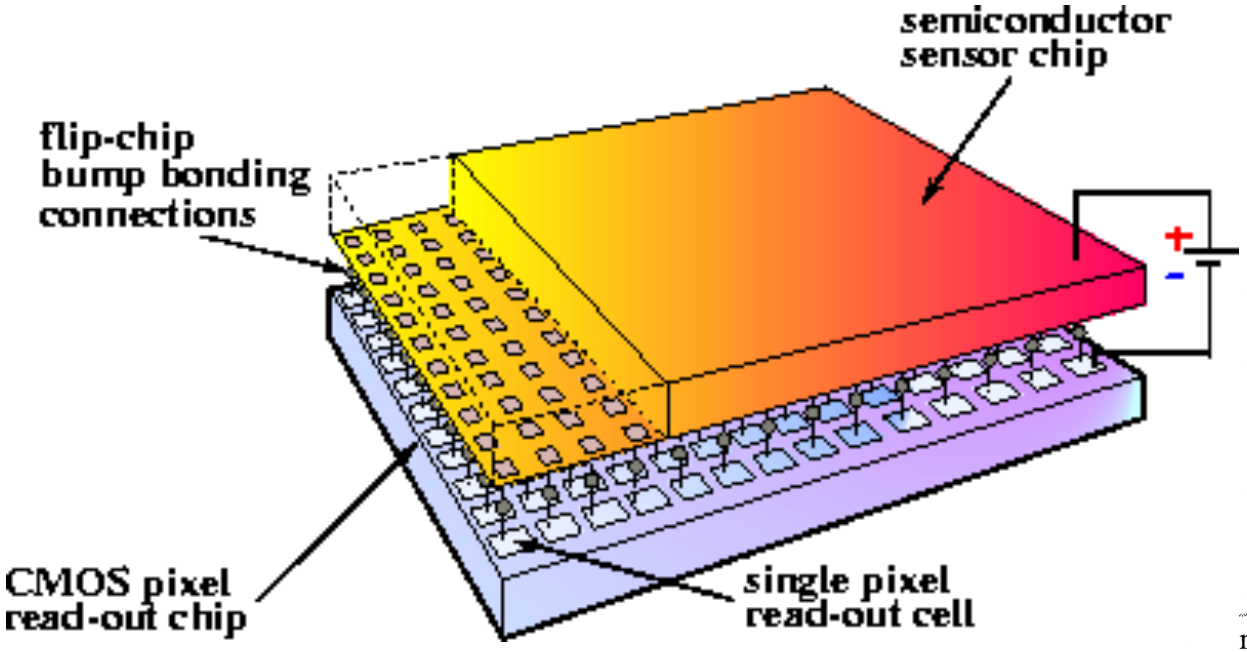
Target of our group

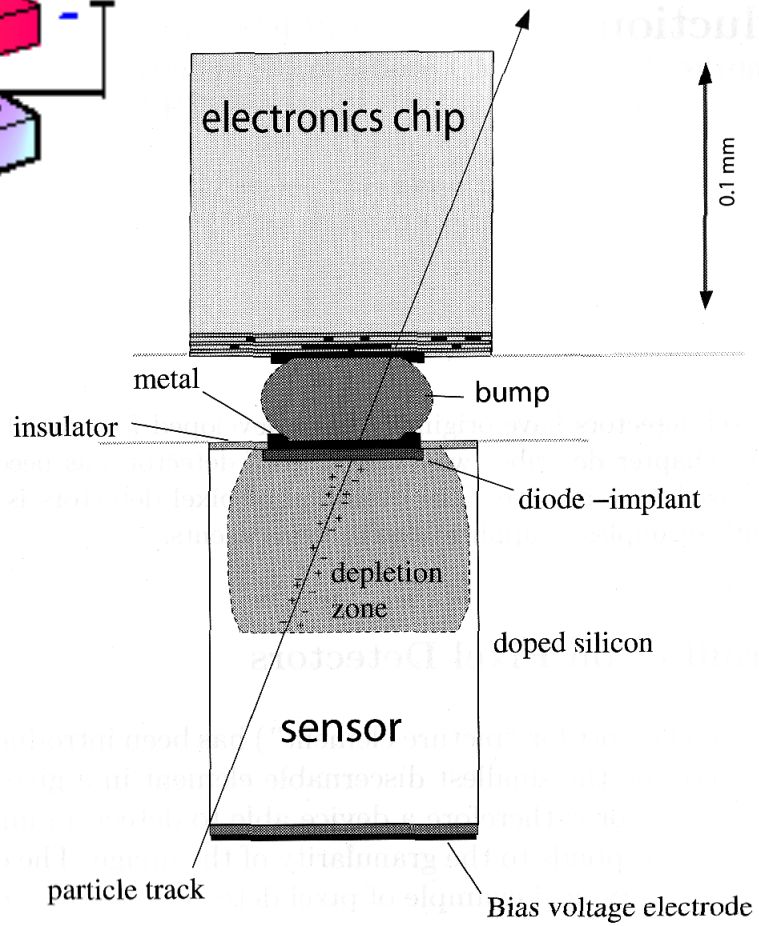
- Development of SOI pixel sensor for next accelerator experiments.
  - higher luminosity accelerator experiment in order to capture the extremely rare interactions.
  - For the identification of the particle by rare interaction, more accurate measurement is critical.

  - The semiconductor vertex detector is required for measuring position of the generated particle with high efficiency and precision.



ピクセル検出器の現状



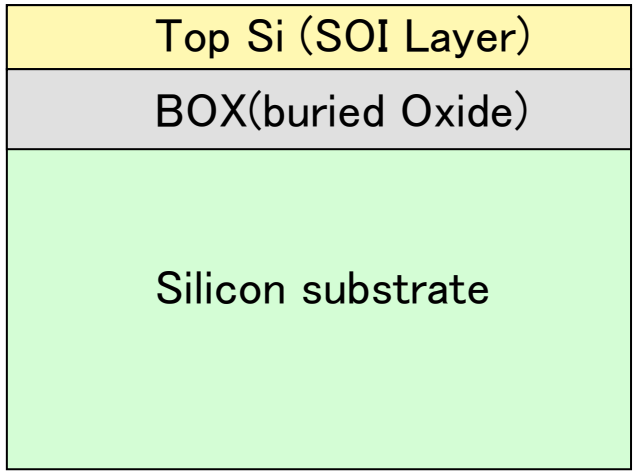


- 検出器と読出しエレクトロニクスを別々に作り、金属バンプにより接合する
- 位置分解能に制限
- 余分な物質が大量にある
- 寄生容量によるスピ-ドの低下

Monolithic detector based on SOI technology

Silicon-On-Insulator

- SOI wafer consists of silicon substrate, Si02 layer called buried oxide (BOX), and top silicon layer (CMOS circuit layer)
- Lower parasitic capacitance due to isolation from bulk silicon,
- The substrate layer can be used as a depleted silicon sensor

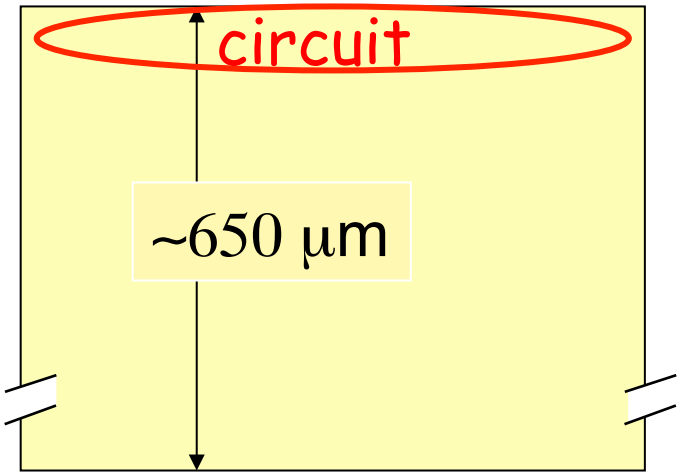


Proposal of SOI sensor

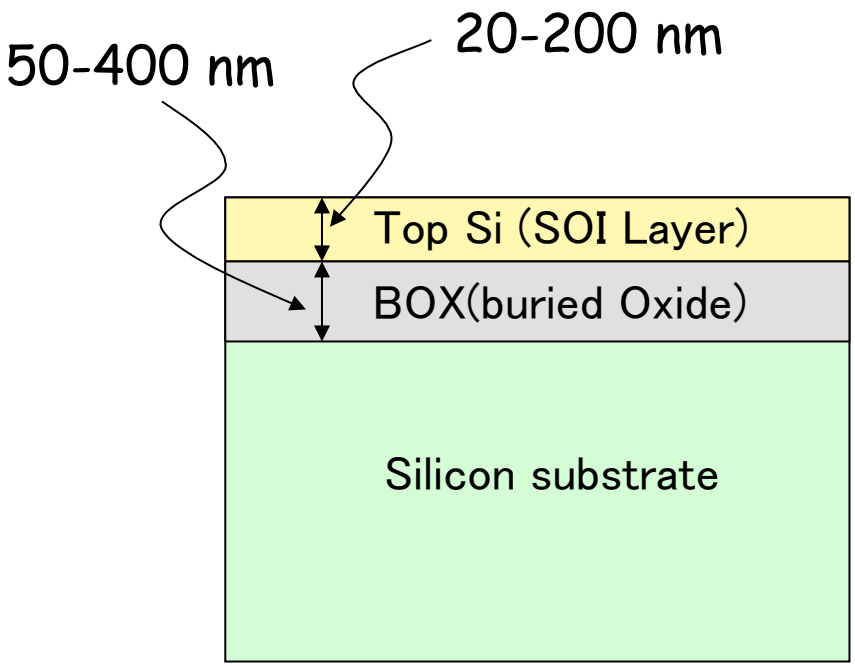
- Implementation plan for ILC sensor
  - Pixel size : 20 × 20μm
  - Maintaining following information in each pixel
    - Analog signal of particle hit position
    - Time information at particle passing
  - More than one storage buffer in each pixel
    - To accumulate multi-hit events in bunch train
  - Digital output by column parallel ADC on sensor chip

- SOI pixel sensor is good solution for those requirement
  - Monolithic detector of sensor and circuit layers.
  - Analog and digital control circuits can be implemented on pixel sensor

Bulk and SOI (Silicon On Insulator) Wafer



通常の半導体ウエハー
(Bulk Wafer)



SOI Wafer

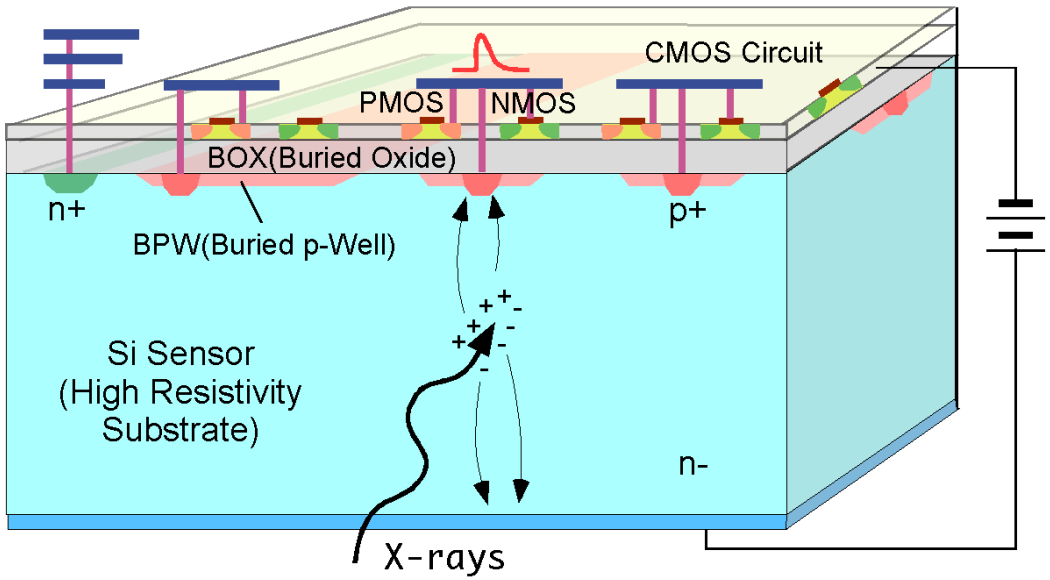
SOIピクセル検出器

- 高抵抗率Si基板と低抵抗率Si基板を絶縁層を介して張合わせ
- 高抵抗率部にp-n junctionを生成し、センサーとする
- 絶縁層(BOX)に穴を開けセンサーと回路を接続

- 余分な物質が少なく、多重散乱をおさえられる
- 電極容量が小さく、少ない電荷で大きなS/Nが得られる
- 複雑な信号処理回路を各ピクセルに持たせられる
- 高レート、高速読み出しが可能
- 機械的接合がなく、高分解能化、低価格化が望める
- 産業界の標準プロセスを基本に開発

Monolithic Radiation Sensor
として理想的な構造

SOI Pixel Detector



Detector requirement 1

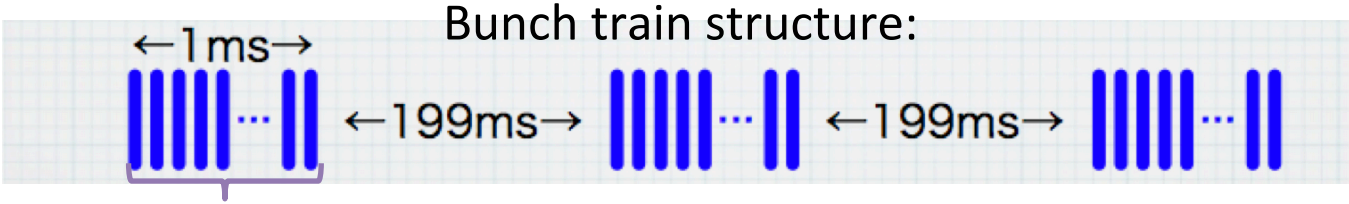
- Position resolution of the decay vertex : < 5μm
  - sensor resolution : < 3μm
  - sensor thickness : < 100 μm / layer
- Correct reconstruction of particle tracks
  - Detector occupancy: < 2%

Pixel size is decided as 20 μm^2 with ADC readout. Thickness of sensor : 50 μm

- Bunch train structure of ILC
  - Separation of hit signals for each bunch event
  - Signal readout between 2 trains

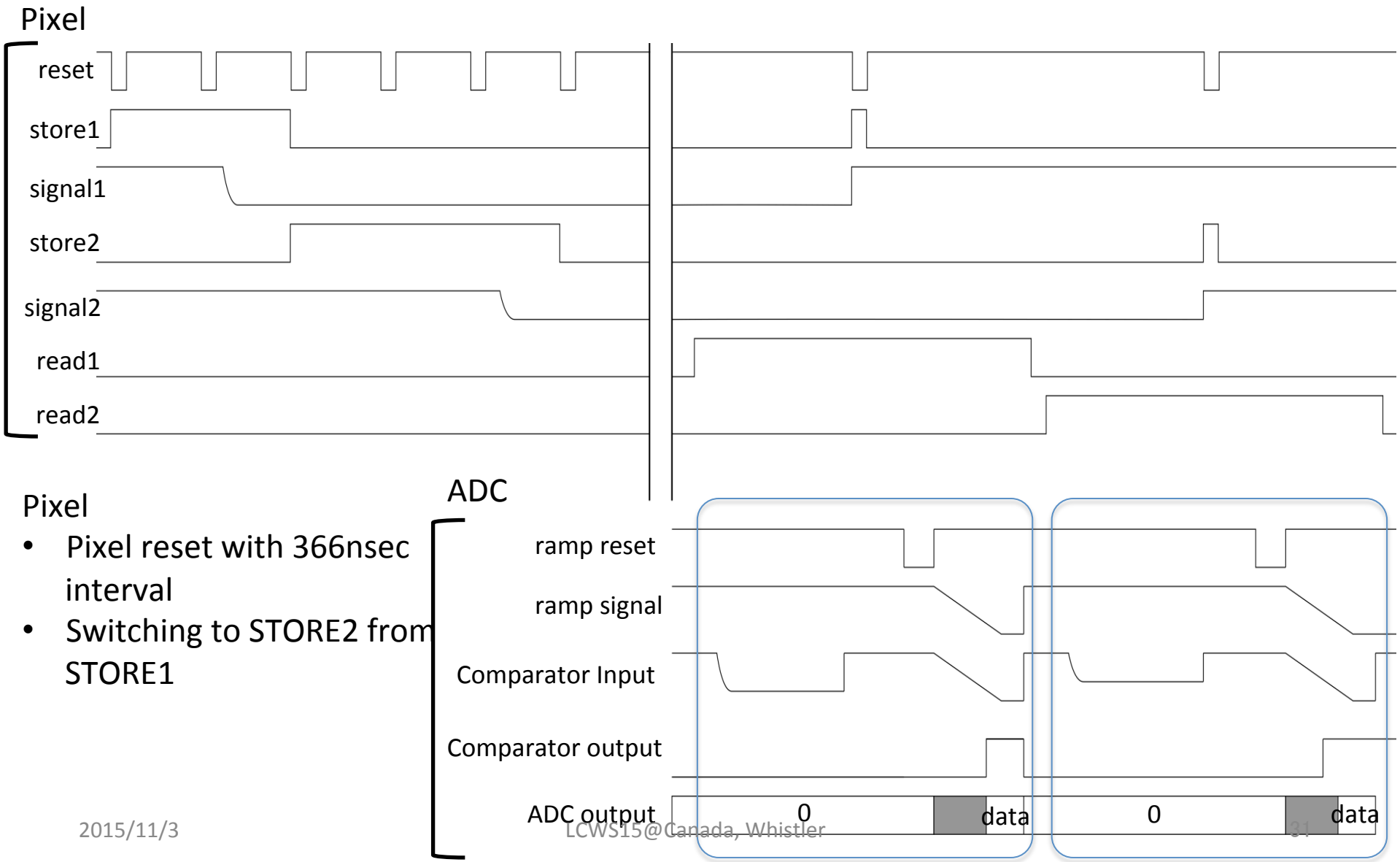
Timing information is necessary

Bunch train structure:



1300 bunches (every 337ns)

Readout timing chart



Pixel

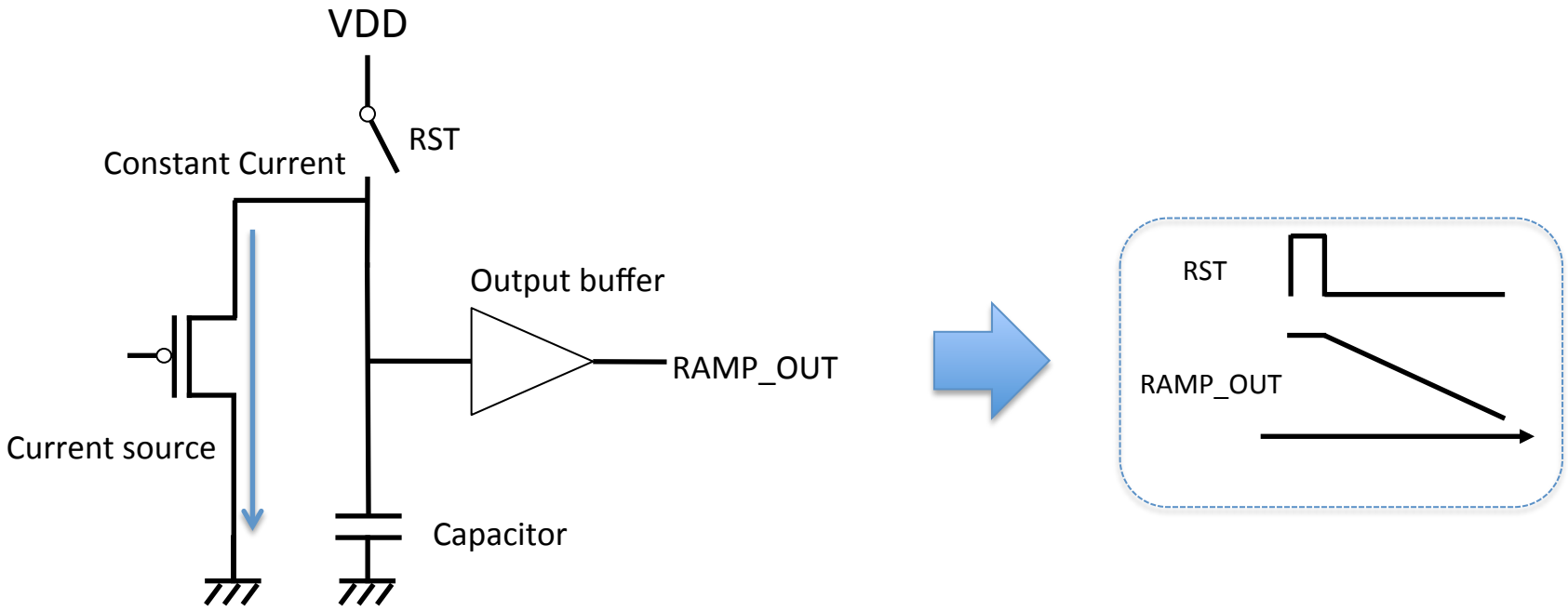
- Pixel reset with 366nsec interval
- Switching to STORE2 from STORE1

SOFIST specification

Description	Spec.	Unit
Pixel size	20	μm□
Active area size	62.5(H) × 10(V)	mm
Total pixel number	3125(H) × 500(V)	–
Sensor thickness	50	μm
Readout	Column parallel ADC	–
Readaout channel	3125	ch
Data buffers in pixel	2 (analog signal) + 2 (time stamp)	–
Noise level	< 237	e^-
Staturation level	20,000	e^-
Time stamp	Analog time stamp circuit (1msec/volt)	–

Ramp generator

- The design of Ramp generator
  - After the charge is stored to the capacitor by reset, the capactor is discharged by constant current source
  - The voltage of capacitance changes linear to time.



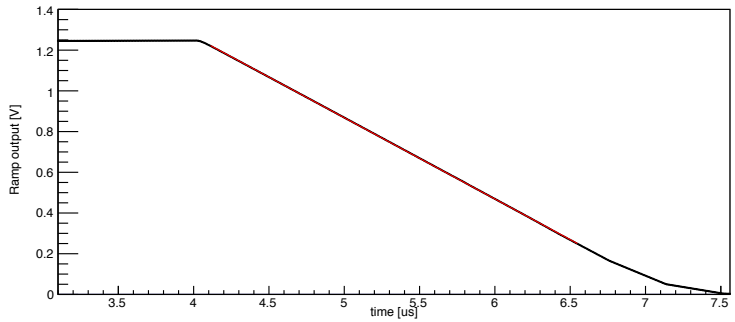
Ramp generator accuracy

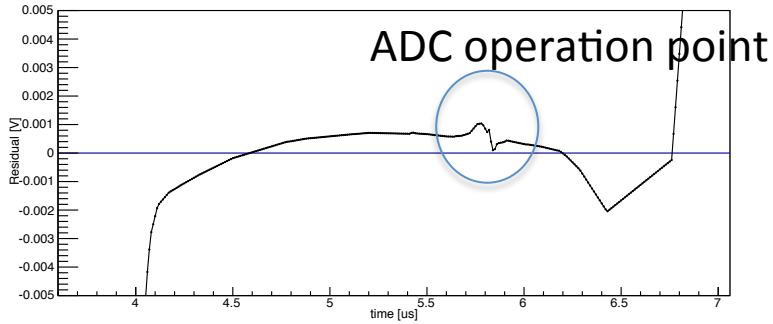
- The linearity of ramp wave output

Ramp output simulation result

- upper: Ramp output voltage
  Red : fitting line

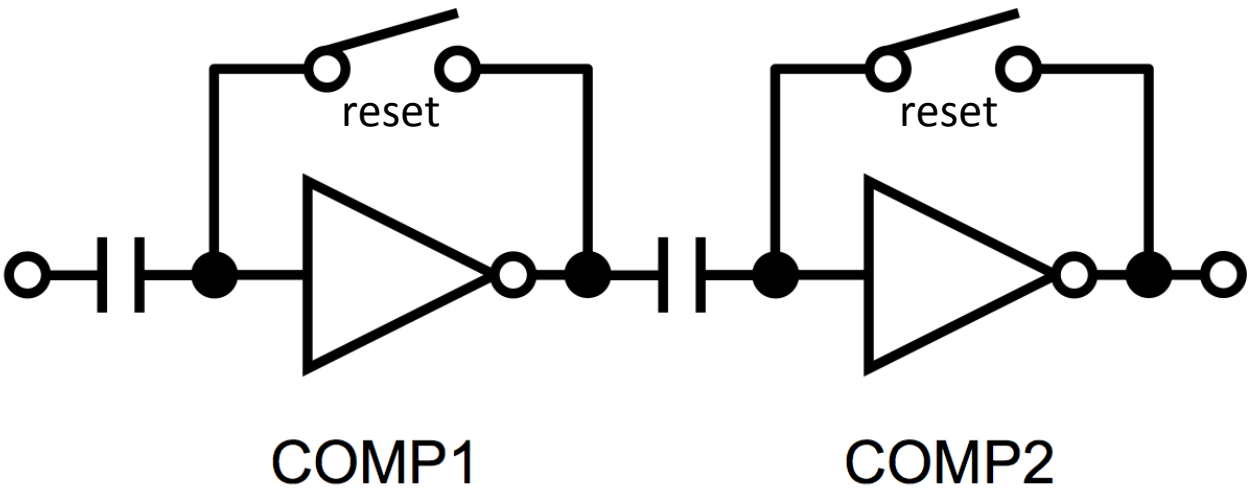
- lower: Residual
  ~ 3.2mV (=0.8LSB)



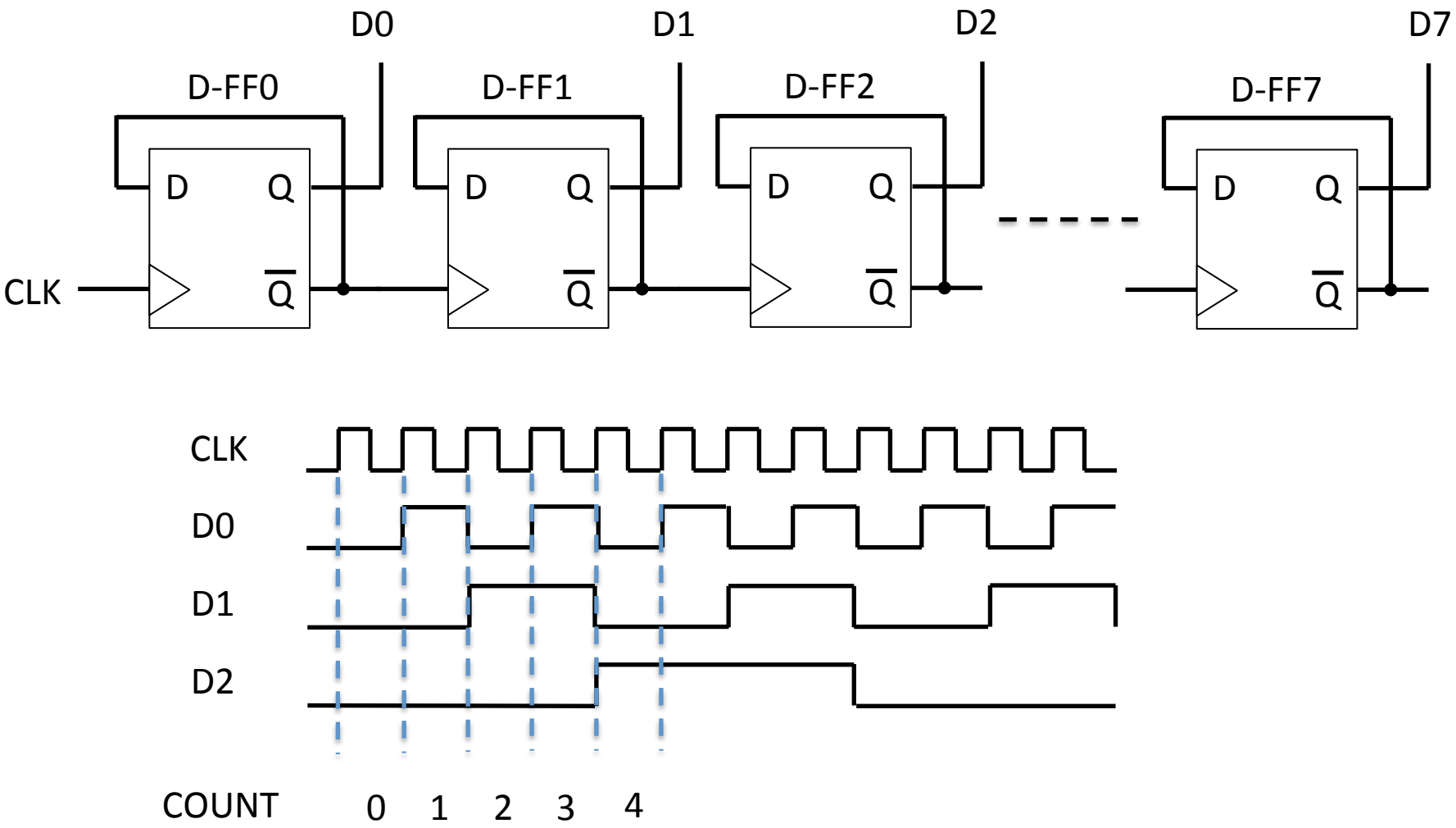


Comparator circuits.

- 2 stage of chopper-inverter comparator
- Operation
  - With turning on 2 reset switches, threshold voltage (V_th) is input.
  - V_th is stored to capacitor by turning off 2 switches in series.
  - Reset voltage (V_rst) is input. The difference voltage (V_th – V_rst) is stored to inverter.
  - If the signal (V_sig) is input and is over V_th – V_rst, the comparator output are inverted.

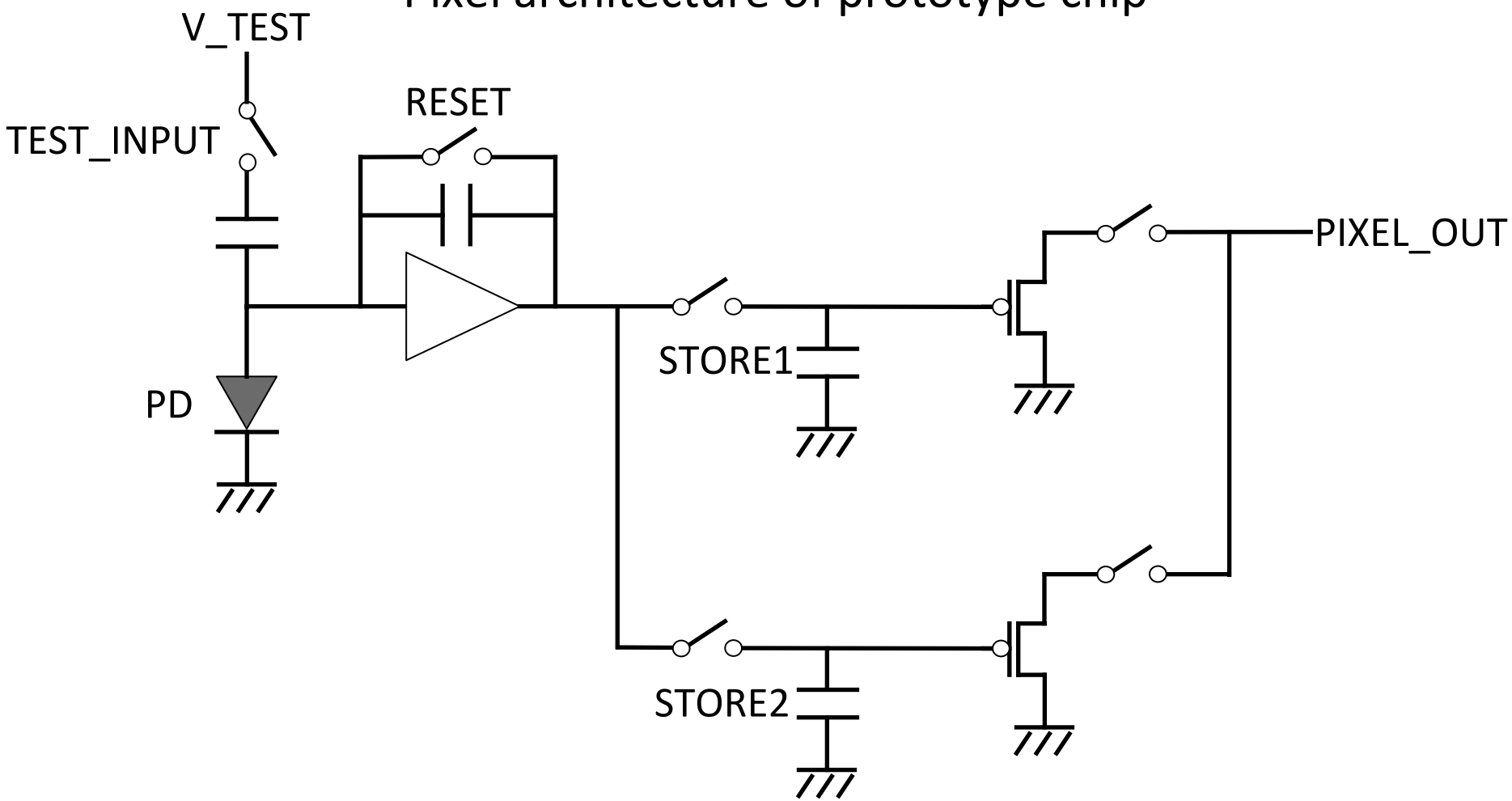


8bit counter



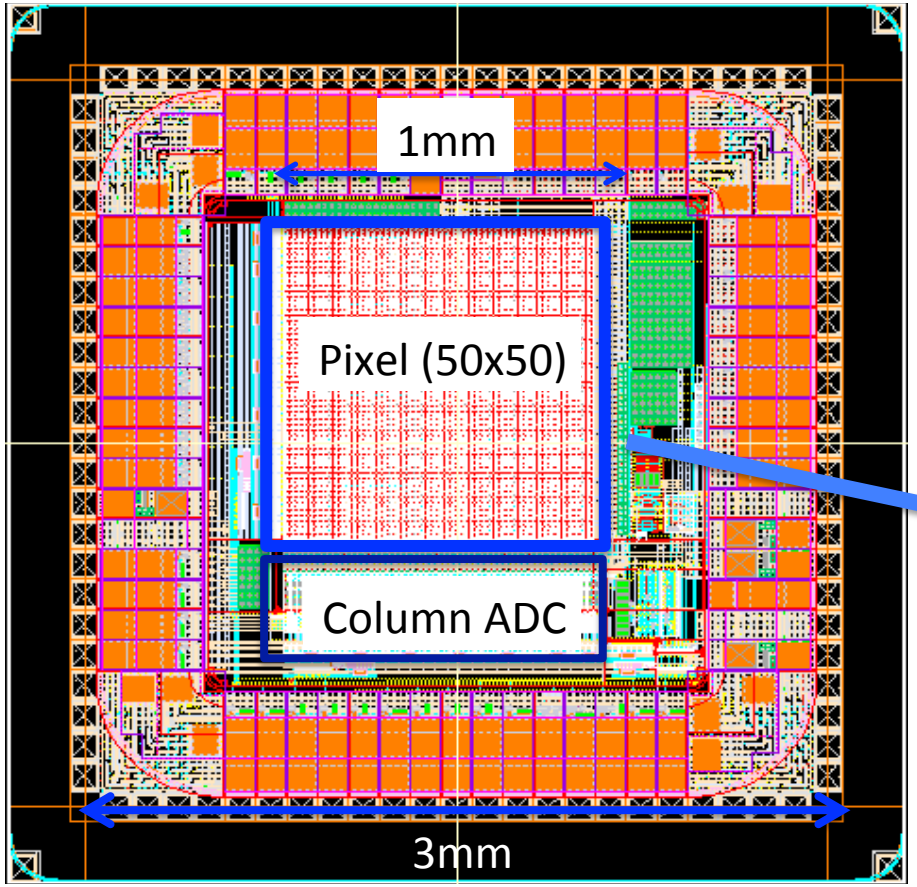
Prototype pixel

- Pixel architecture of prototype chip

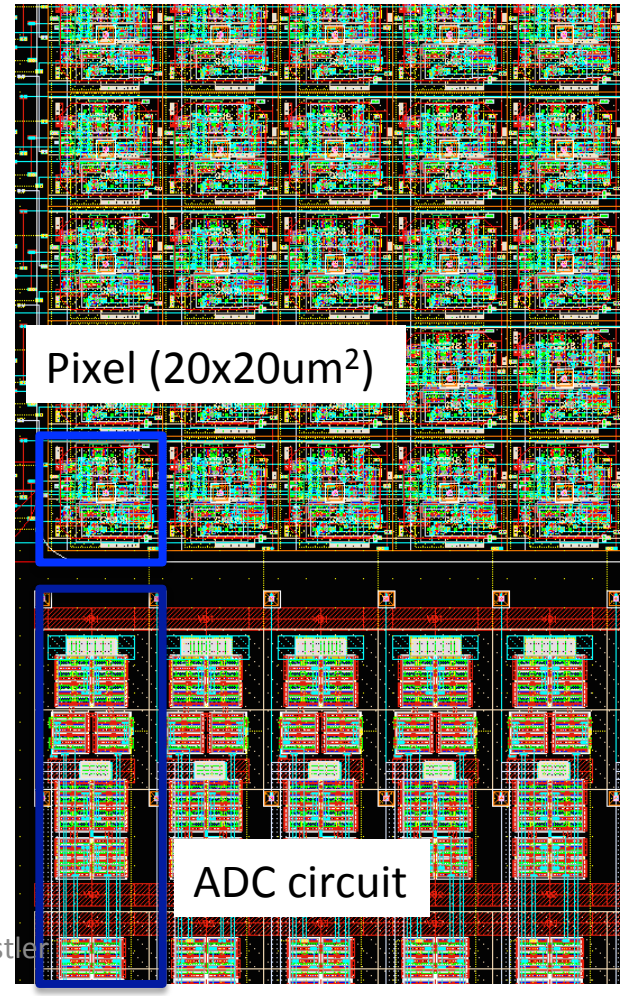


SOFIST Prototype chip (Ver.1)

Prototype chip layout

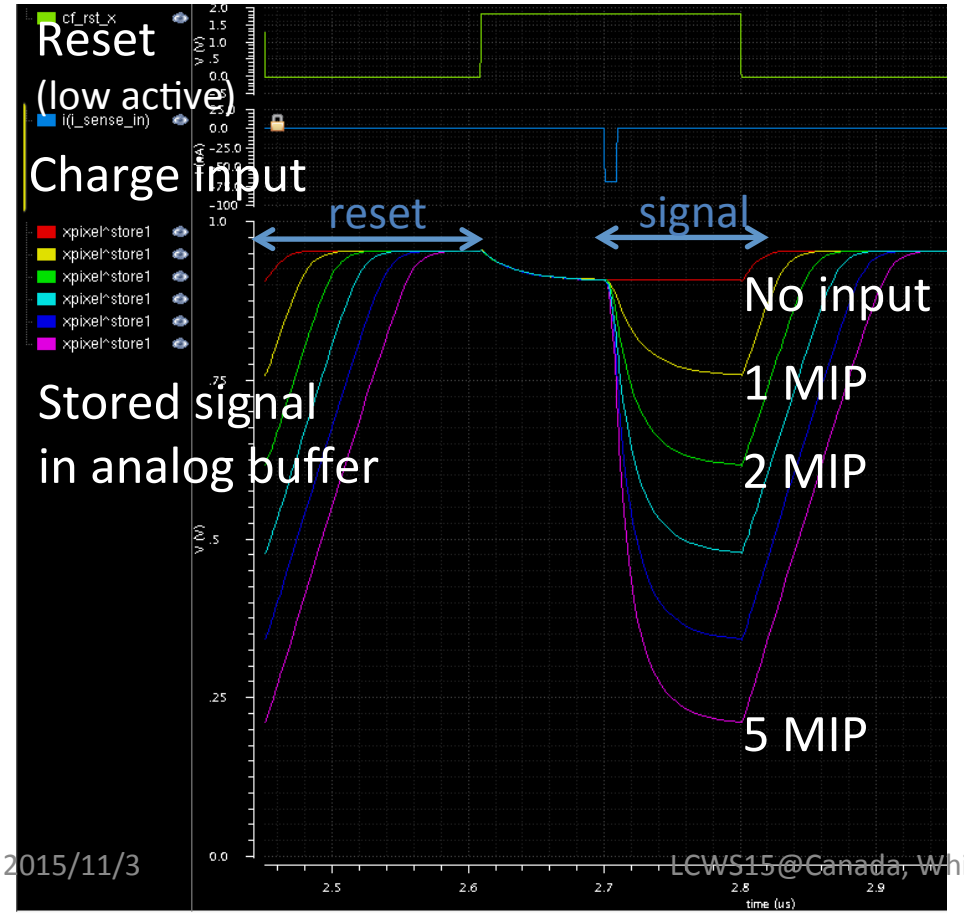


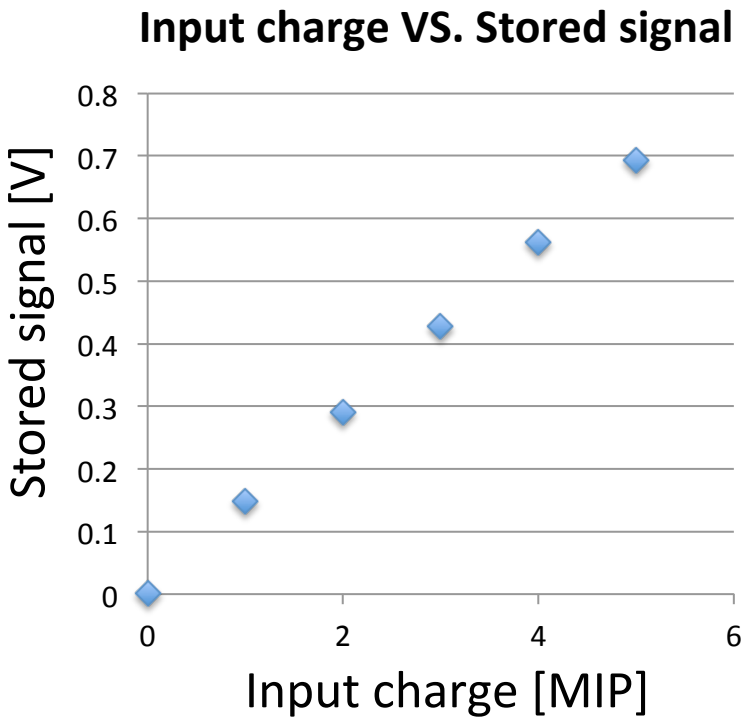
Pixel & column ADC



Pixel simulation

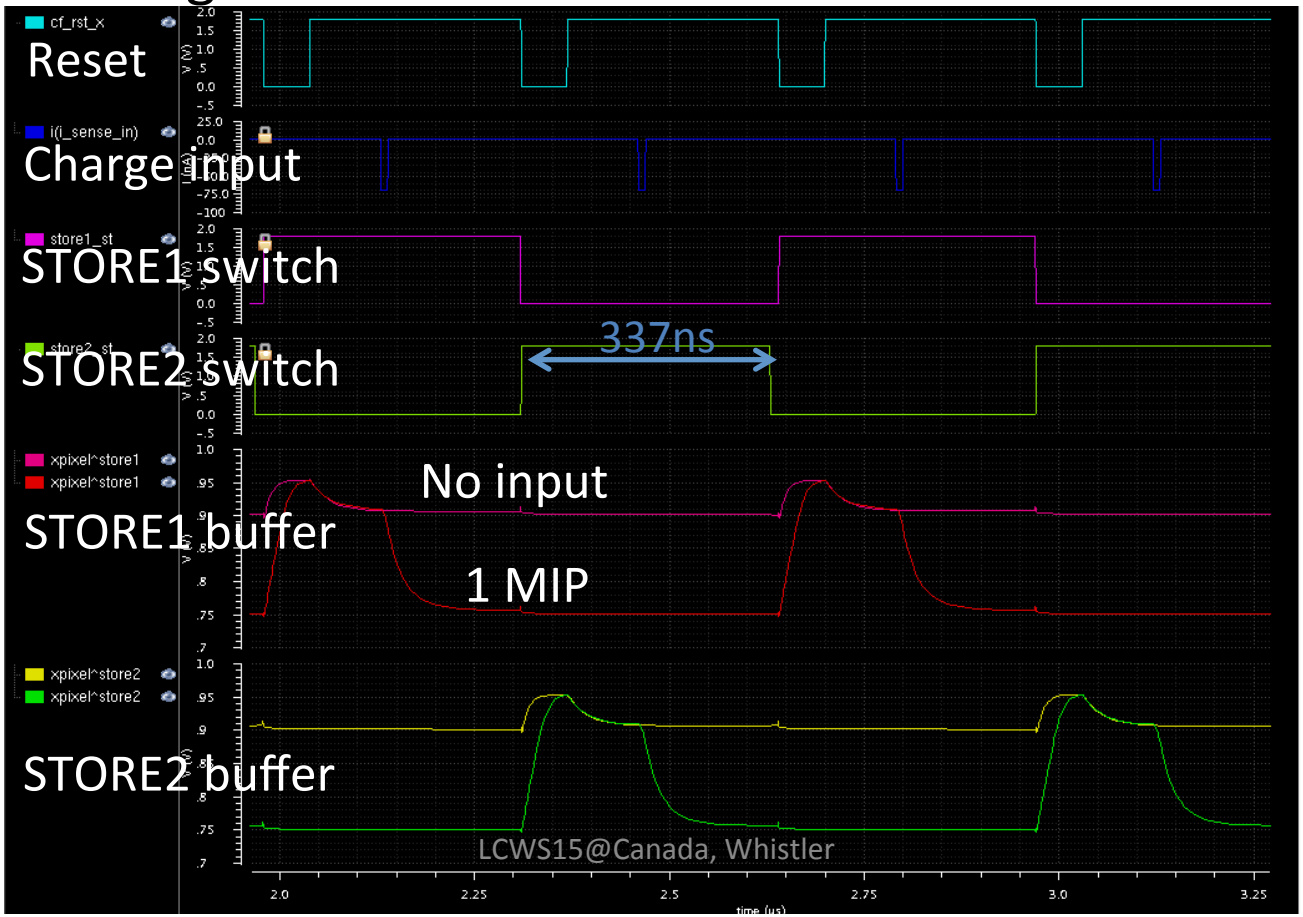
- Stored-signal simulation by charge input
  - Input charge: 0~5 MIP (0~19,000e- 1MIP = 3777e-)



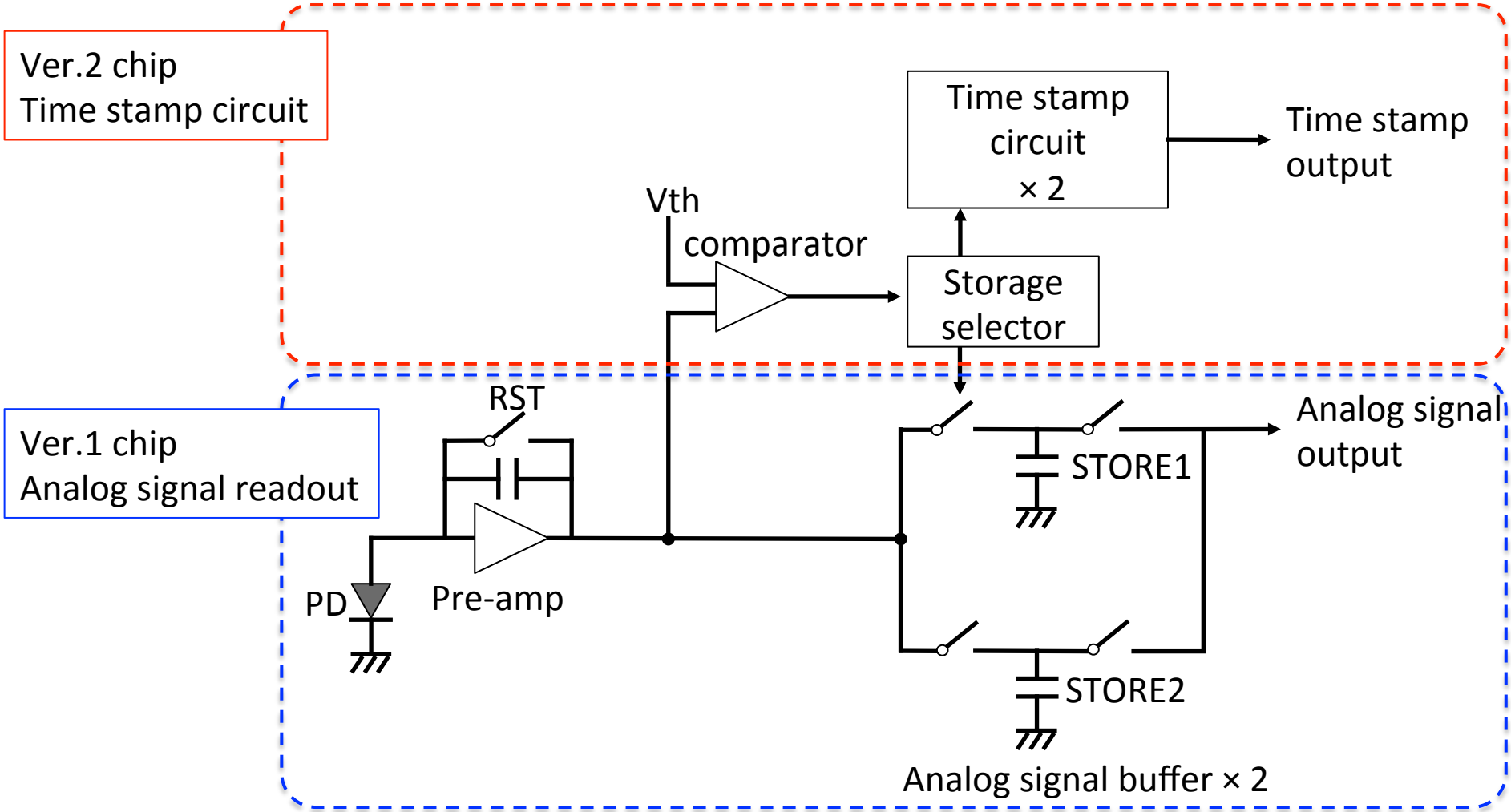


Pixel simulation 2

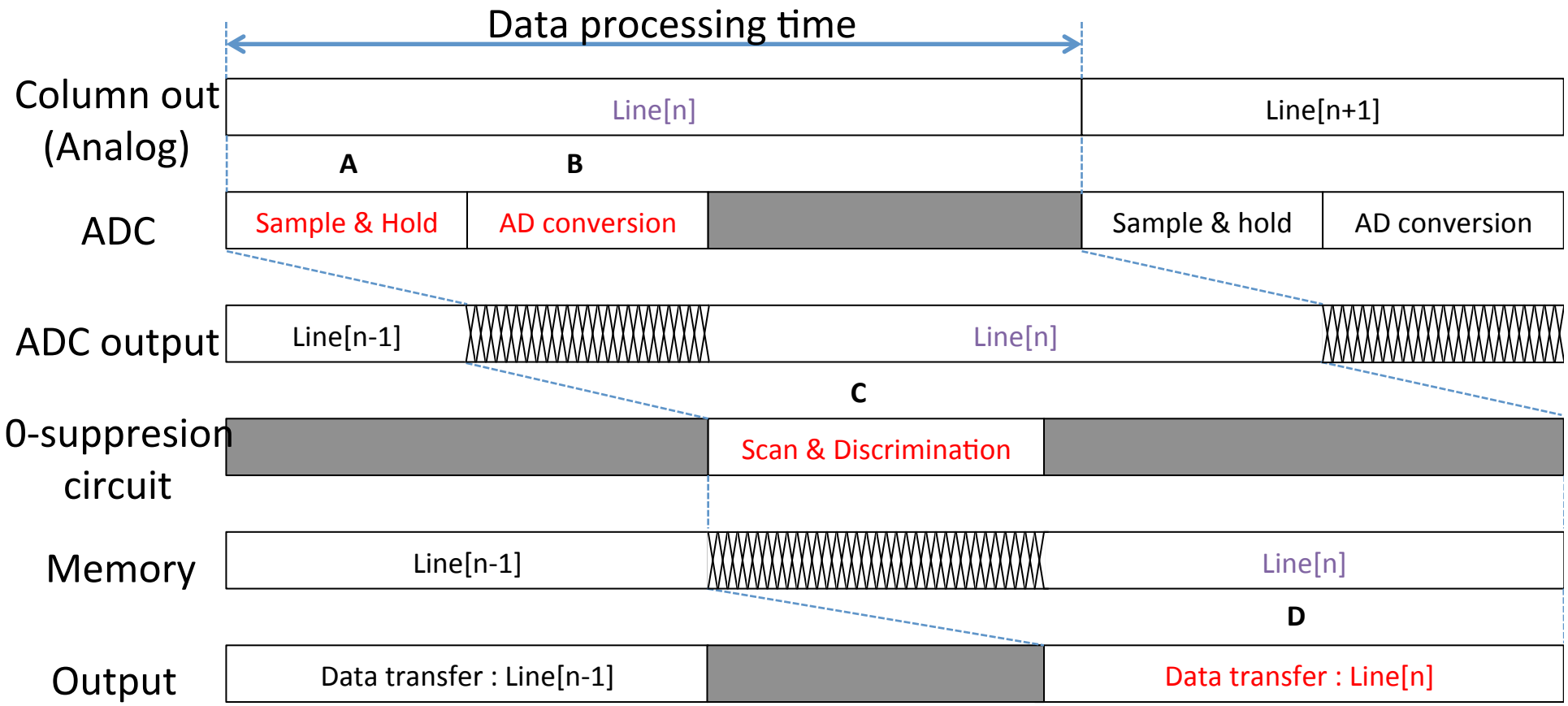
- Switching performance between analog buffers
  - Input charge: 0, 1 MIP (1MIP = 3777e-)
  - Switching interval: 337ns



Development of pixel circuit



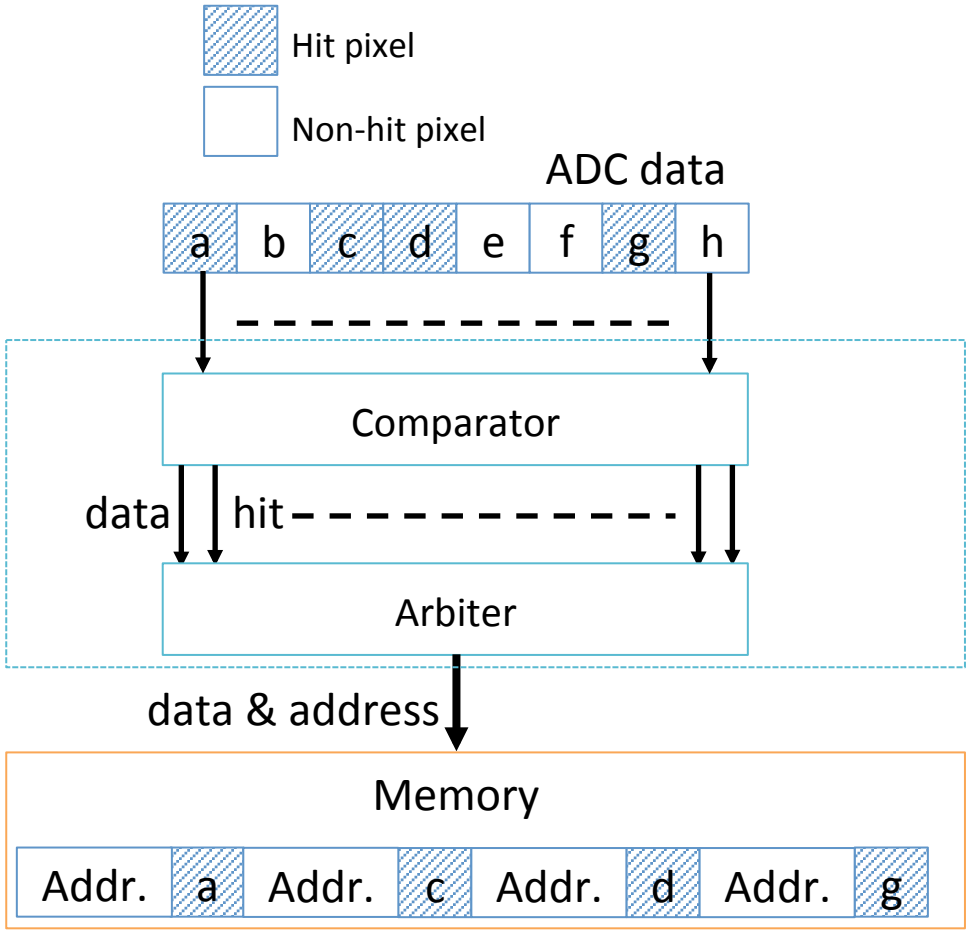
Readout timing chart



- Some operations can be overlapped to next data processing in order to shorten the readout time.
- Total readout time of 1 line (from A to D): < 100usec

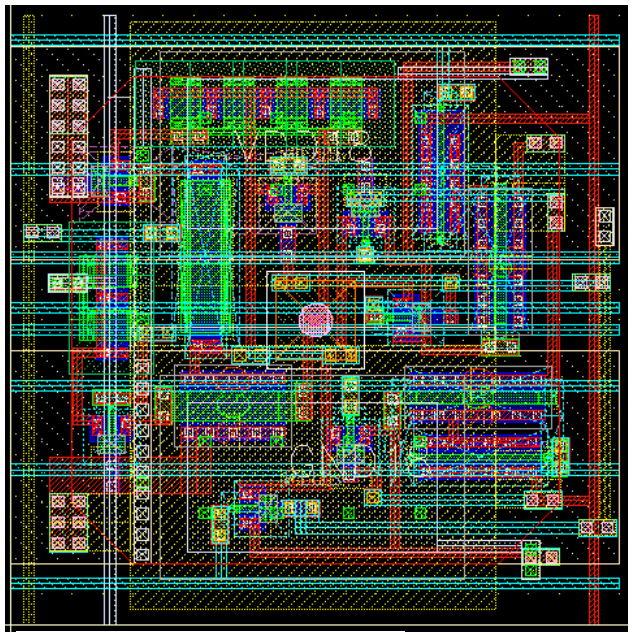
0-suppression logic

- Hit detection of each column
- Extraction of hit data by arbiter block
- Output of hit data with column address

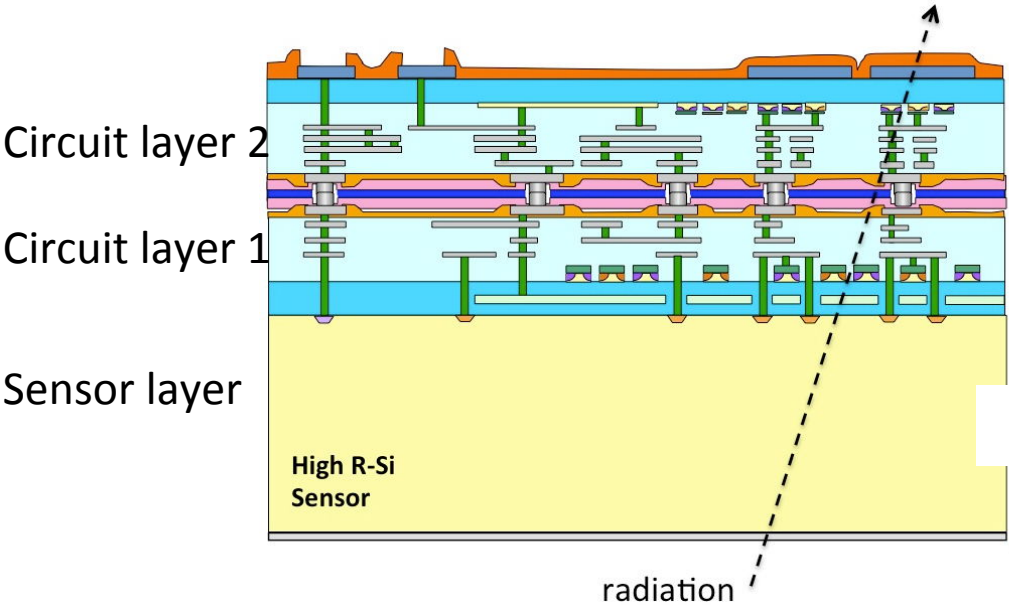


3D technology

- Implementation of pixel circuit
  - Pixel area: 20x20μm^2
  - High density integration by 3D stacked layer technology



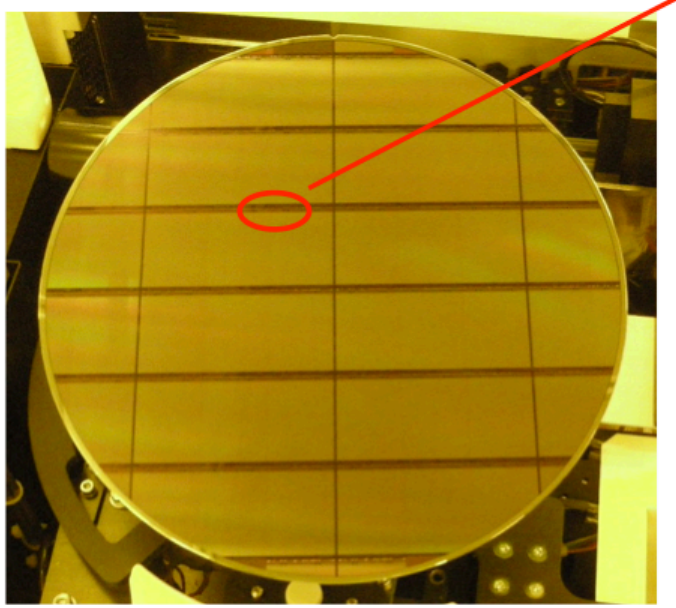
SOFIST ver.1 pixel

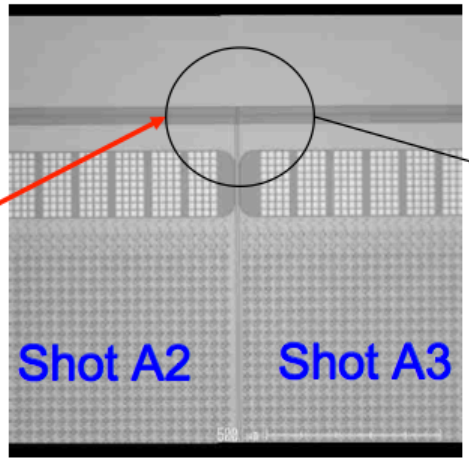


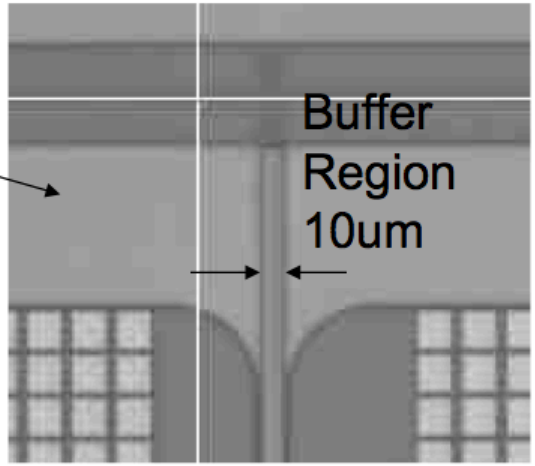
Arai, Yasuo, and Makoto Motoyoshi, *IEEE EDAPS*. 2013

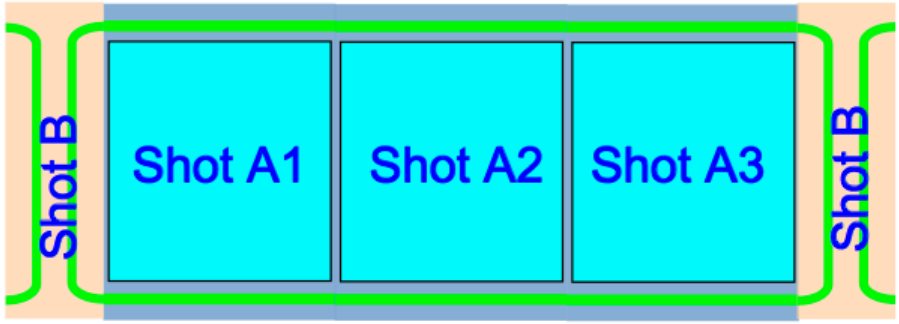
Stitching Exposure for Large Sensor

Produce 26.7 mm x 64 mm Sensing Area (3 Stitching).





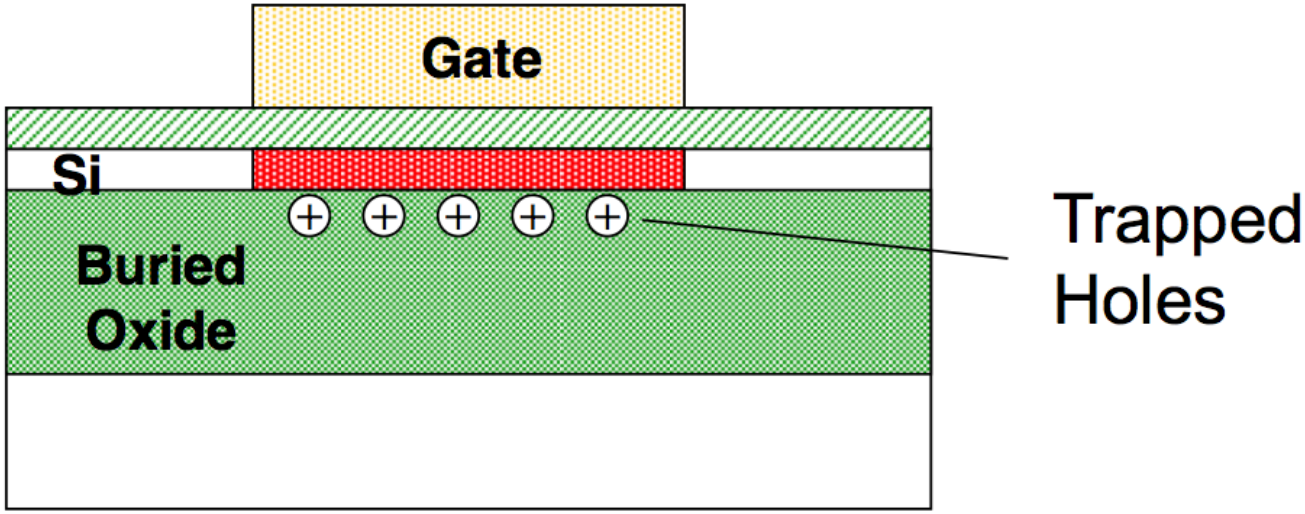




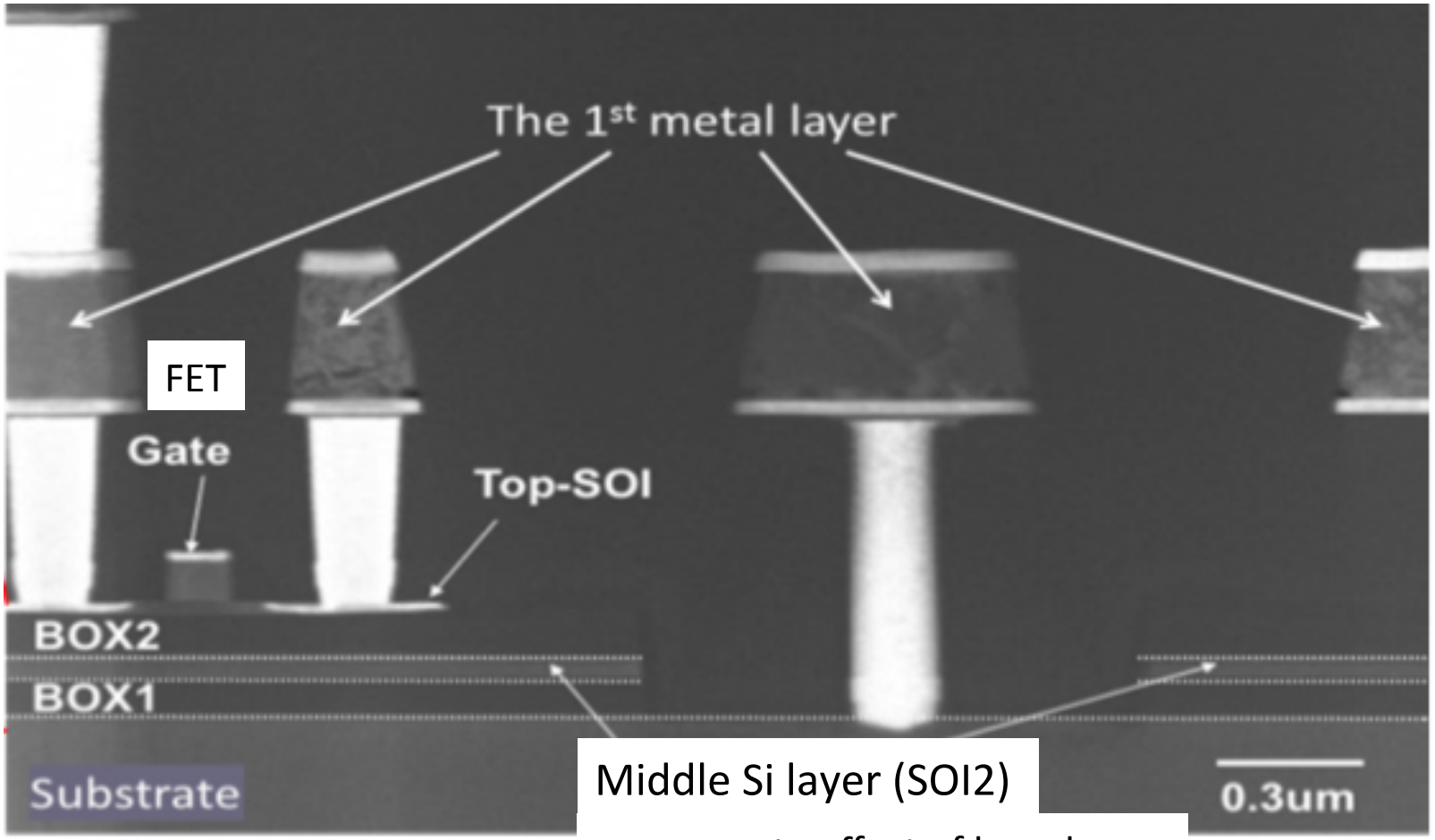
- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
- 1-direction stitching at present.

Radiation tolerance of SOI wafer

Total ionizing dose due to buried oxide layer



Double-SOI wafer



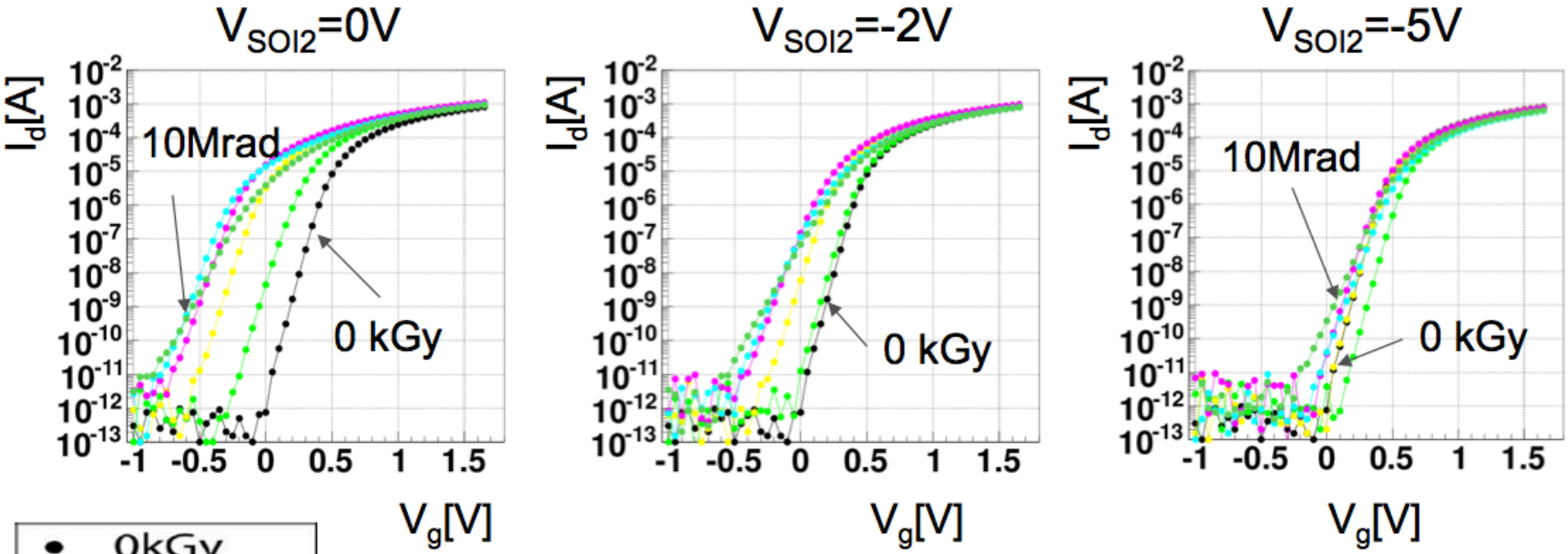
Middle Si layer (SOI2)

compensate effect of box charge

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



By setting Vsoi2 ~ -5V, Id-Vg curve returned nearly to pre-irradiation value.

UNIBOND™ Process (1995, France LETI) -> SOITEC

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B