Recent developments in LC vertex and tracking R&D

LCWS 2015

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Whistler

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Outline

- Vertex-detector concepts and R&D examples
- Tracker concepts and R&D examples
- Conclusions

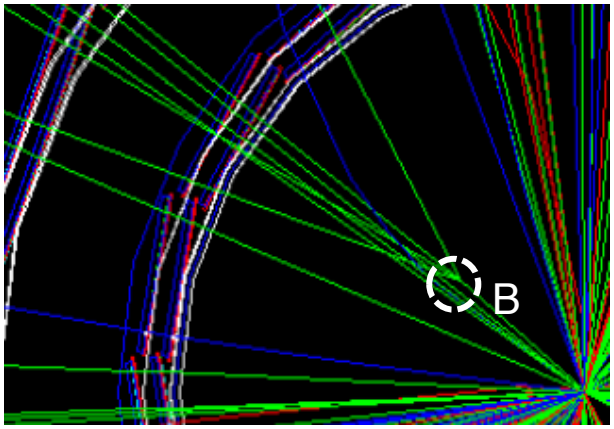
Disclaimer:
- Showing only examples of recent developments here
- More details and results in parallel session talks and in detector R&D report by M. Titov and J. Strube

LC vertex-detector requirements

- Efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

a~5 μm, b~10-15 μm



→ Good single point resolution: σ_{SP}~3 μm
→ small pixels <~25x25 μm²
→ Low material budget: X ≲ 0.1-0.2% X_0 / layer
→ corresponds to ~100-200 μm Si, including supports, cables, cooling
→ low-power ASICs (~50 mW/cm²) + gas-flow cooling

- 20-200 ms gaps between bunch trains → trigger-less readout, pulsed powering
- B = 3.5-5 T → Lorentz angle becomes important

- Few % maximum occupancy from beam-induced backgrounds → sets inner radius
- Moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year

- For CLIC: Time stamping with ~10 ns accuracy, to reject background
  → high-resistivity / depleted sensors, readout with precise time stamping

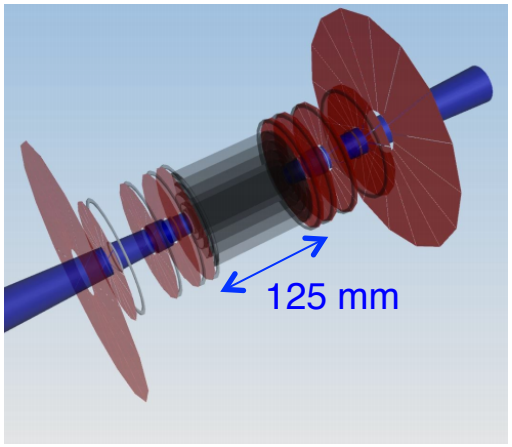
Vertex-detector concepts for ILC + CLIC

ILD, SiD and CLIC detector concepts:

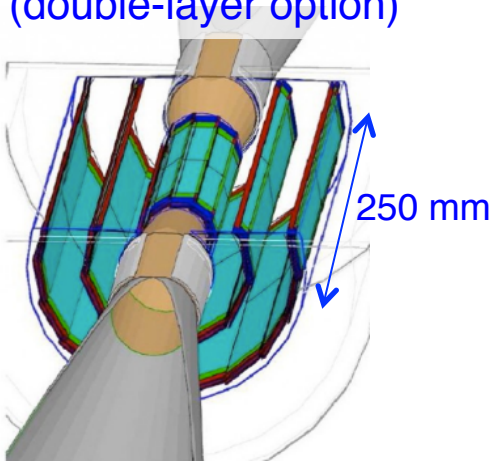
- Systematic optimization of geometries:
  - Background occupancies
  - Detector performance
- Barrel/endcap geometry (except ILD)
- 3 double layers or 5 single layers
- R_i between 14 mm (SiD) and 31 mm (CLIC)
- Beam pipes with conical sections
- ~1 m^2 area, few times 10^9 pixels

- Air-flow cooling and power pulsing presumed (detailed concepts and studies with mockups for CLIC and for ILD FTD)
- r/o technology not yet chosen for any of the projects

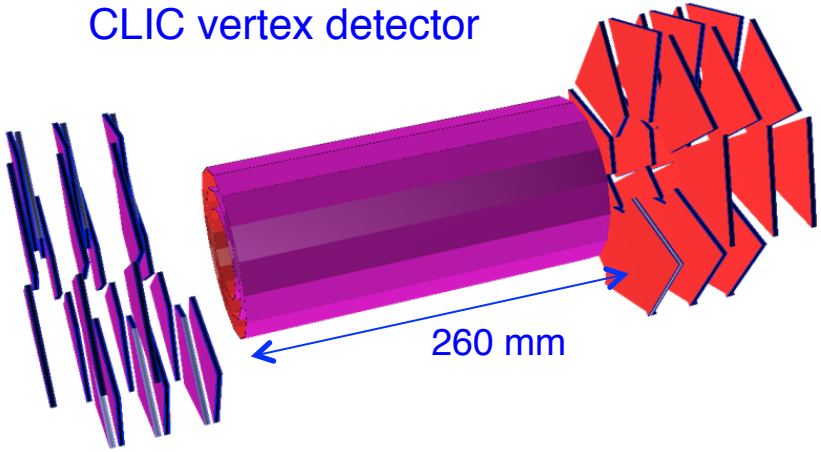
SiD vertex detector



ILD vertex detector (double-layer option)



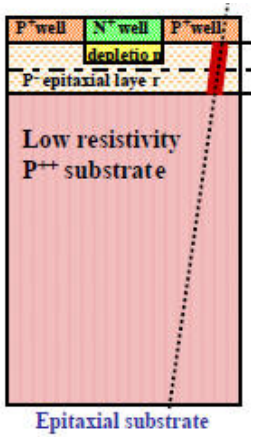
CLIC vertex detector



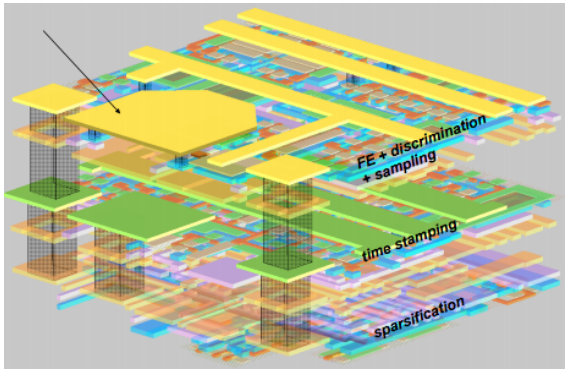
Pixel-detector technologies

Technology	Examples	Small pixels	Low mass	Low power	Fast timing
Monolithic CMOS MAPS	Mimosa CPS	++	++	**++**	**-**
Integrated sensor/amplif. + separate r/o	DEPFET, FPCCD	+/++	o	+	-
Monolithic CMOS with depletion	HV-CMOS, HR-CMOS	+	++	**o**	**+**
3D integrated	Tezzaron, SOI	++	+	o	++
Hybrid	CLICpix+planar sensor, HV-CMOS hybrid	+	o	+	++

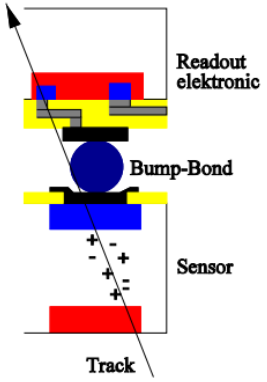
1st generation MAPS



3D integrated



Hybrid



LC pixel R&D examples

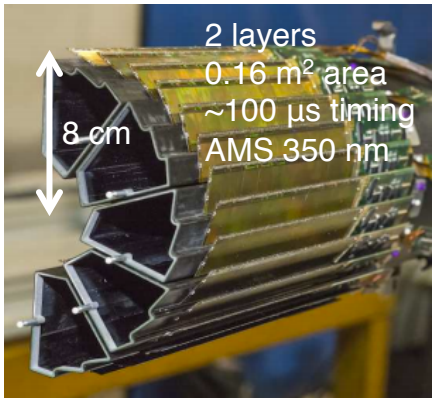
Project	Technology	Target experiments	Groups
Mimosa	**fully integrated** CMOS MAPS Tower Jazz 0.18 um	ILD@ILC, ALICE, CBM, BES-3	IPHC Strasbourg
Arachnid / Cherwell		generic vtx / tracking / calo, ATLAS	RAL and others
Chronopix	**fully integrated** CMOS MAPS IBM 90 nm	SiD@ILC	Oregon
FPCCD	**integrated sensor**, separate r/o, Hamamatsu CCDs	ILD@ILC	KEK, Tohoku
DEPFET	**integrated sensor**, separate readout, MPG-HLL DEPFET	ILD@ILC, Belle II	Bonn, MPI Munich, Barcelona, Santander, others
VIP2b / SDR / MAMBO4	**3d integrated** Tezzaron + STM 130 nm	SiD@ILC, generic vtx/ tracking, Super-Belle	FNAL, KEK, INFN, others
SOI	Latis **SOI** 200 nm	SiD@ILC, LC generic	KEK, Osaka, AGH, others
HV-CMOS CCPD	**active sensor**, 180 nm CMOS	CLIC, HL-ATLAS	KIT, CERN, CPPM, Bonn, Geneva, others
CLICpix	**hybrid r/o**, 65 nm CMOS	CLIC, SiD@ILC	CERN

Integrated r/o technology: Mimosa

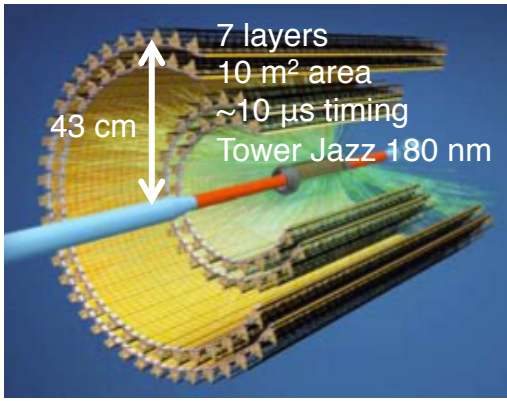
Monolithic Active Pixel Sensor (MAPS/CPS):

- MIMOSA chip family (IPHC Strasbourg)
- Fully integrated CMOS technology
- Charge collection mainly diffusion, timing limited by rolling-shutter r/o (µs)
- Successfully deployed in HEP, with increasingly demanding requirements:
  - Test-beam telescopes
  - STAR @ RHIC
  - CBM MVD
  - ALICE ITS upgrade → 1st example of pixelated tracking
  - Baseline technology for ILD VTX
- Moving towards smaller feature size (180 nm) and higher-resistivity substrates (few kOhm cm)
- Recent focus is on layout/technology optimisation for ILD: double layers with combined spatial / timing layers with with single-bx timing
- Low-mass supports concept: PLUME ladders, 0.3% X0 / module

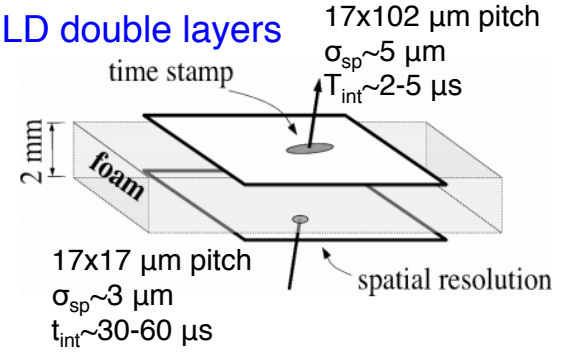
STAR vertex det.



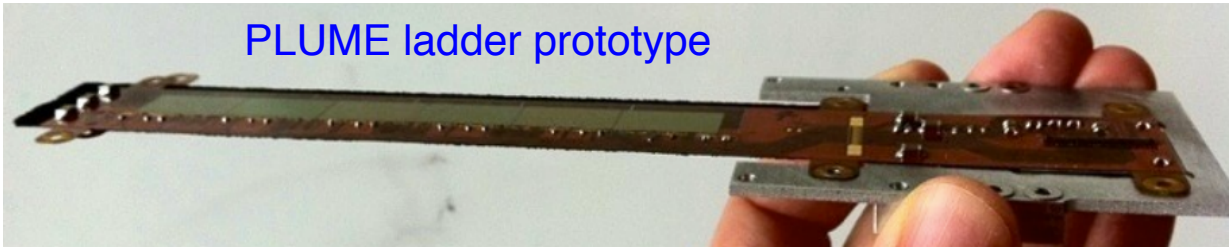
ALICE ITS upgrade



ILD double layers



PLUME ladder prototype



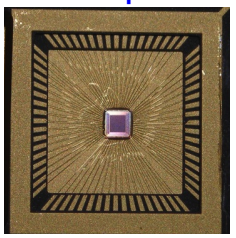
Other integrated r/o technologies

Several MAPS developments for faster timing, for example:

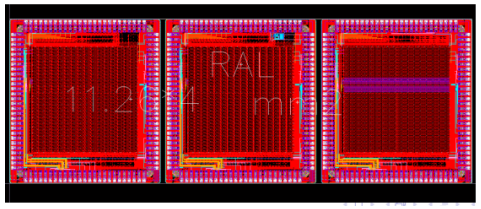
- Chronopix for SiD (Oregon)
  - monolithic CMOS pixel sensor with fast per-pixel time stamping
  - 3rd prototype built in TSMC 90 nm process, 25 µm pixels
  - results so far only with sources
- Cherwell, HR-CHESS (ARACHNID collaboration)
  - integrated MAPS low-noise pixel detector, 180 nm deep well CMOS with **high-resistivity** epitaxial layer
  - Cherwell2 and Cherwell3 prototypes for ALICE ITS upgrade
  - HR-CHESS PonN (40 µm x 40 µm)
  - HR-CHESS2 for ATLAS strip upgrade (800 µm x 40 µm)
  - test-beam measurement campaigns
- Mupix (KIT and others)
  - Fully integrated 180 nm **high-voltage** CMOS process
  - For Mu3e experiment and ATLAS upgrade
  - Mupix7 prototype: 100 µm x 80 µm pitch, ~20 ns timing

- Progress for LC often limited by manpower and driven by applications in other domains

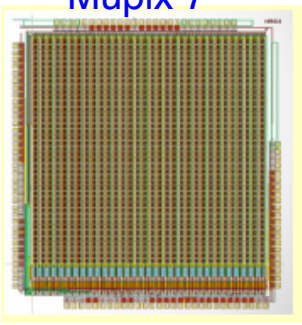
Chronopix 3



Cherwell 2



Mupix 7



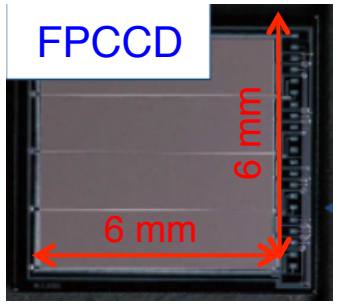
Semi-integrated technology: FPCCD

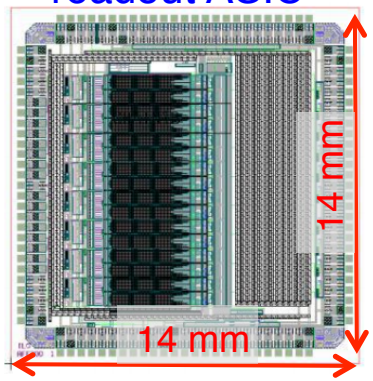
Fine Pixel Charge-Coupled Device:

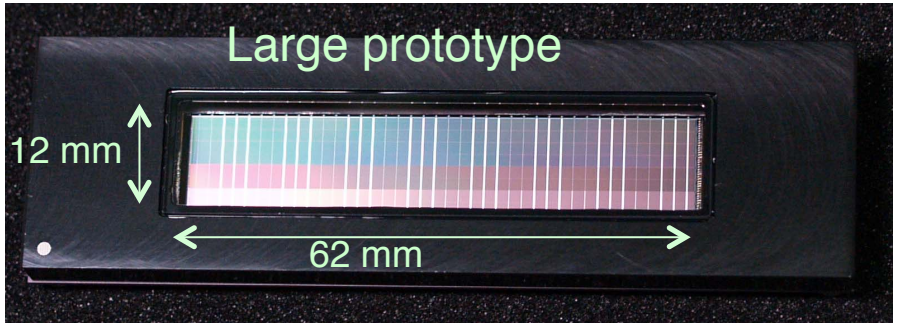
- Semi-integrated technology (separate r/o ASICs), thin modules, but material pushed to endcaps
- 5-10 µm pixel pitch (10^{10} px for ILD VTX!)
- Integrate over ILC bunch trains (no time stamps), r/o during gaps ~ 10 MPx/s
  → background rejection by pattern recognition

- Operation at -40 °C in cryostat with CO_2 cooling (power consumption ~30 W)

- Small and large prototypes built and tested:
  50 µm thin wafer
  6, 8, 12 µm pixel pitch
- neutron-irradiation tests performed







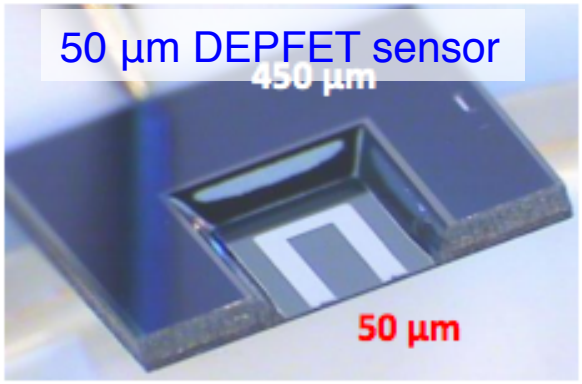
Semi-integrated technology: DEPFET

Depleted Field Effect Transistor (DEPFET):

- Depleted layer under FET
- Monolithic sensor, but r/o separate

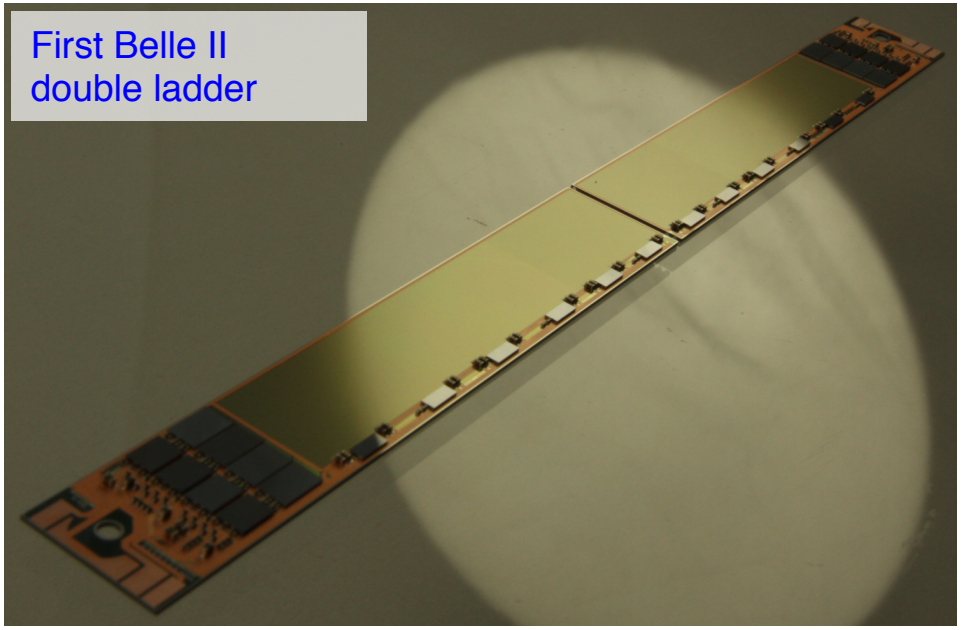
→ Thin (~50 µm), small pixels (~25x25 µm^2), but material accumulation at endcaps

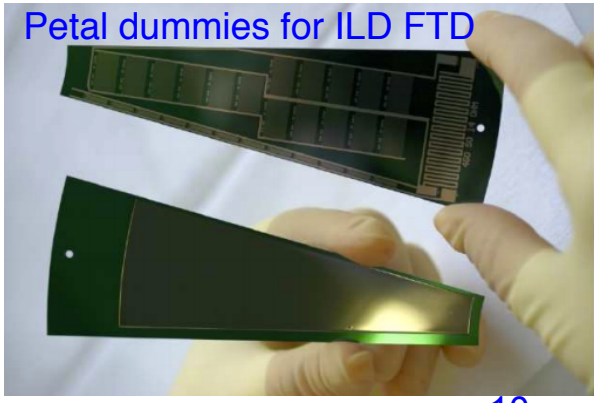
- Readout with ~20-100 µs frame time
- In production for Belle II
- Good yield: 80% of sensors from pilot wafers working
- First Belle II half ladders fully functional
- New: concept for ILD forward disks, taking advantage of flexibility in wafer-layout



Sensor yield pilot wafers

Type	W30	W35	W36
IF	0	98.44	98.96
OF1	100.00	98.44	98.96
OF2	99.48	98.96	99.48
OB1	97.72	99.40	0
OB2	99.48	0	98.96
IB	97.92	0	99.48
Total	**83.3**	**66.6**	**83.3**



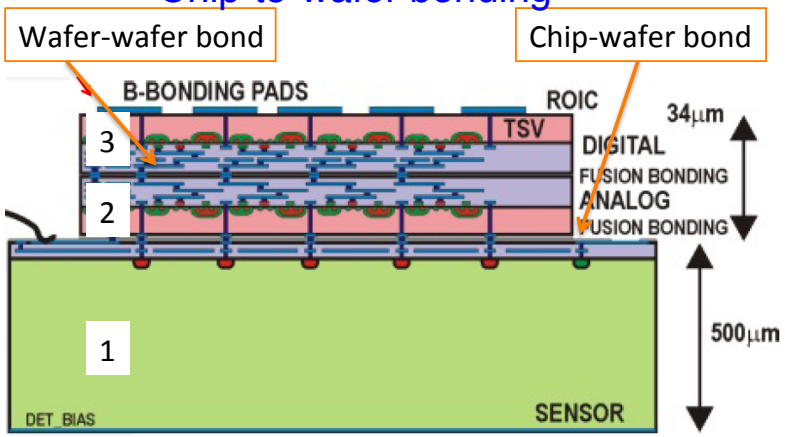


3D sensor+r/o technology

3D technology:

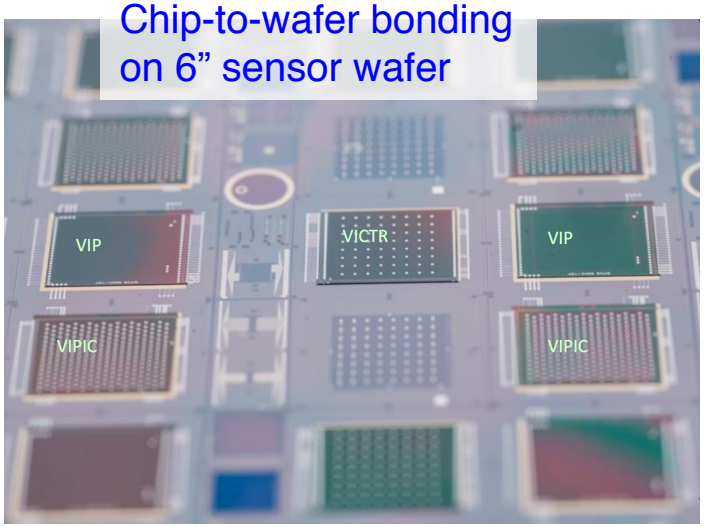
- Functionality of hybrid pixel detector in monolithic devices through 3D integration: sparsification, time stamping
- Example: 3DIC multi-project-wafer run through Tezzaron / Chartered in STM 130nm:
  - 2-tier process, many technical problems, 3y turnaround
  - Now functional chips produced:
    - VIP2b for SiD@ILC (FNAL): 24 µm pitch, 192x192 array
    - SDR1 for Super-B, now ILC (Bergamo, Pavia, INFN)

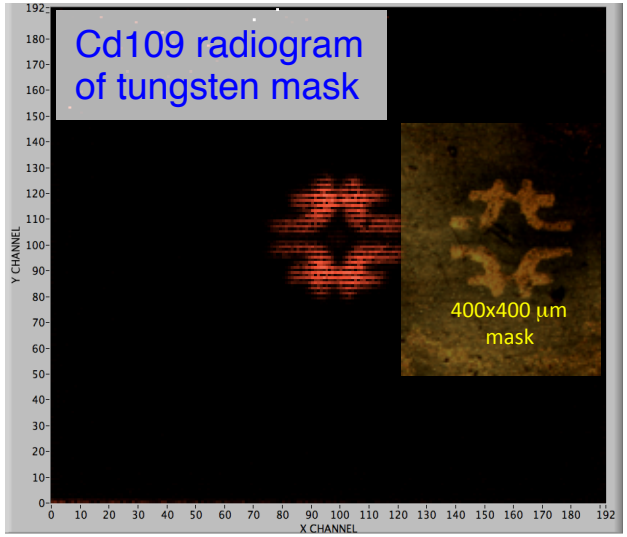
Chip-to-wafer bonding



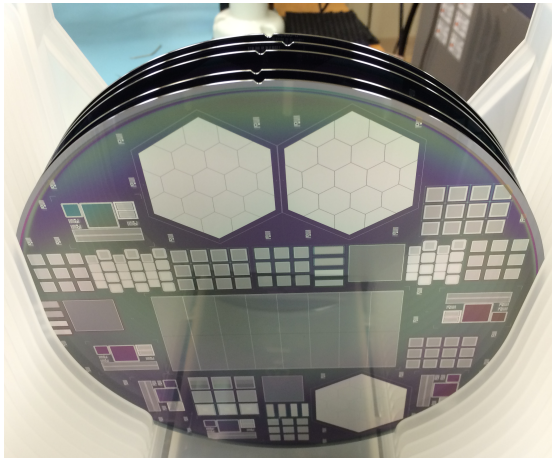
- Test results for VIP2b chips oxide-fusion bonded to FNAL/Tezzaron 6" sensor wafers: ~2x less noise compared to bump-bonded sensors (lower capacitance of oxide bonds)
- 8" sensor wafer produced (version thinned to 200 µm in production)
- Next project phase with DOE x-ray funding, demonstrated 1µm vias in 6µm thick silicon

Chip-to-wafer bonding on 6" sensor wafer





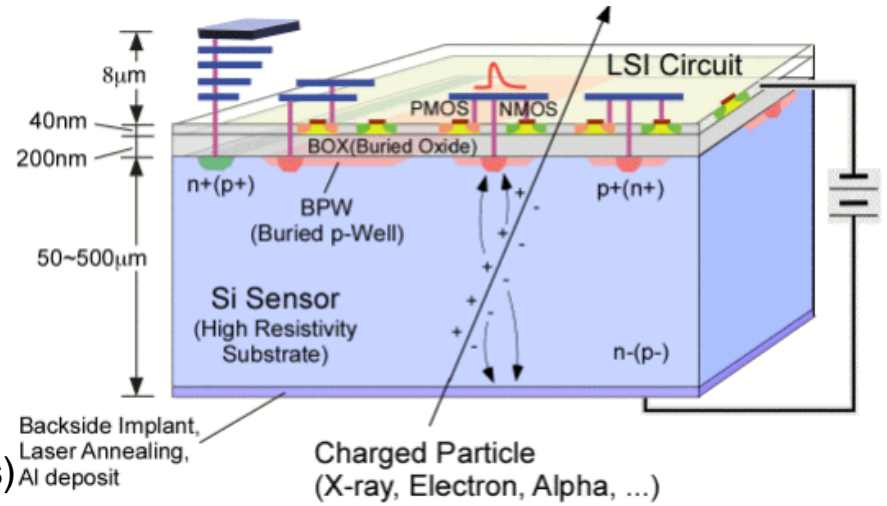
FNAL/Tezzaron 8" sensor wafer



Silicon On Insulator (SOI)

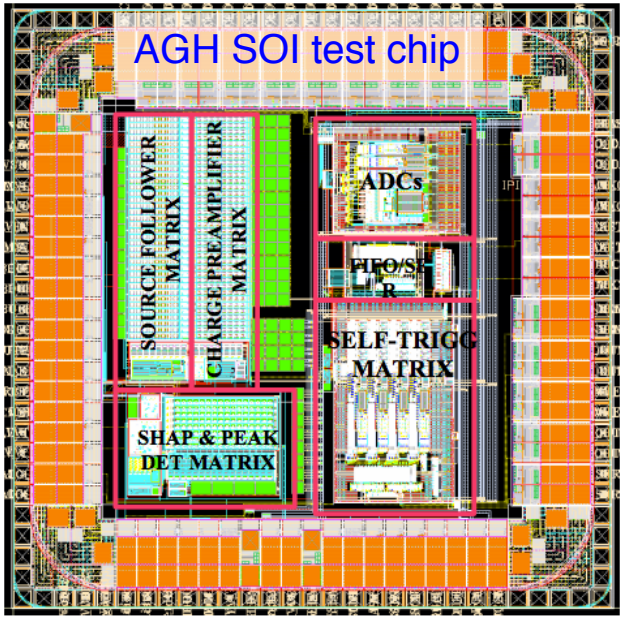
Silicon On Insulator (SOI) technology

- CMOS sensor on SOI wafers
- Electronics on low resistivity wafer separated by buried oxide from fully depleted high-resistivity sensing layer
- Allows for standard CMOS electronics with complex functionality
- Fast time stamping possible
- Recent progress on radiation hardness (double SOI, controlled discharge of surface charges)



- Example: Latis 200 nm SOI process (KEK, Osaka, AGH Krakow, others)
- Complex process work flow, limited availability and long turn-around times

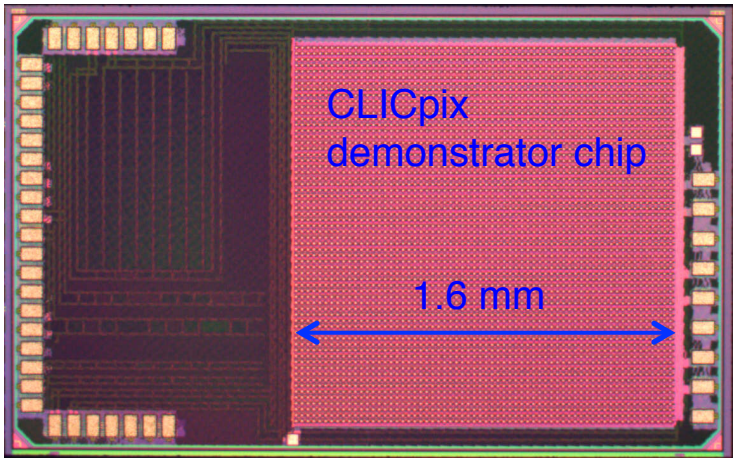
- Recent LC test-chip submission from AGH:
  - Small matrices with pixel sizes ≥ 30 x 30 µm^2
  - Targeted towards CLIC requirements (position, amplitude and few ns timing)
  - Chips expected ready for testing soon
- LC test chip with 20 x 20 µm^2 pixels under design at Osaka, targeted to ILC (µs timing)

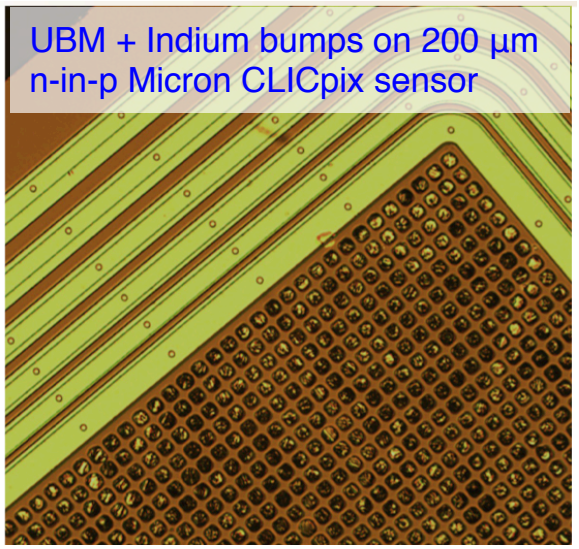


Hybrid r/o with planar sensors

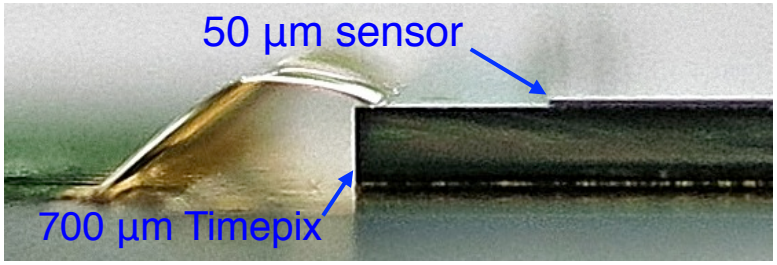
Hybrid readout assemblies:

- Ultra-thin planar sensors bonded to high-performance r/o ASICs
- "Classical" approach used in LHC pixel detectors
- Allows for factorization of ASIC and sensor R&D
- Example: CLICpix r/o ASIC in 65 nm (with RD53)
  - Targeted to CLIC requirements: 25 µm pixel pitch with analog r/o, timing ~10 ns, power pulsing
  - Small-pitch bump-bonding process developed
  - Test results from demonstrator chips bump-bonded to 200 µm thick Micron n-in-p sensors
  - TCAD and Geant4 simulations
- In parallel: evaluating performance of ultra-thin edgeless sensors with Timepix r/o ASICS (55 µm pitch)
- Concepts for mechanical integration, air-flow cooling, power delivery and power pulsing





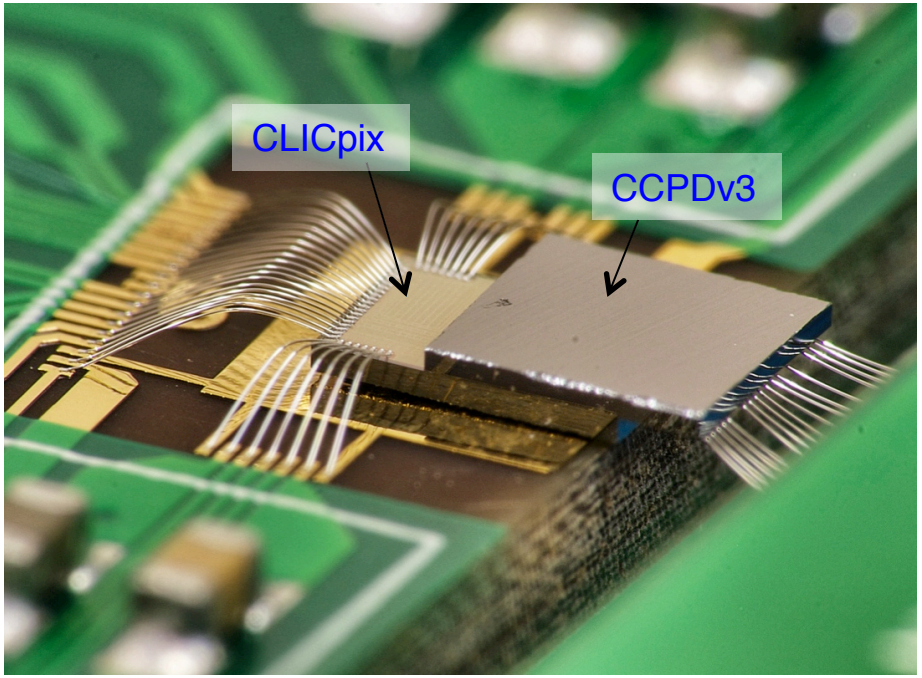
C. Kenney, A. Tomada (SLAC)

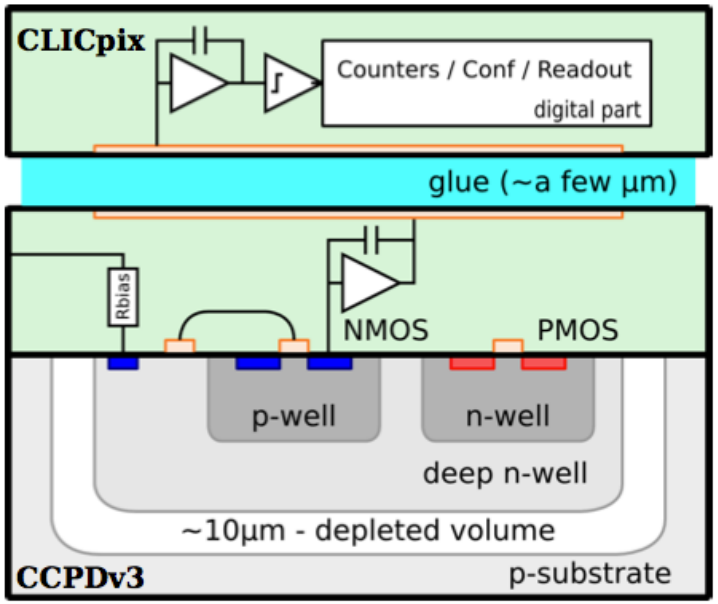


Hybrid r/o with active HV-CMOS sensors

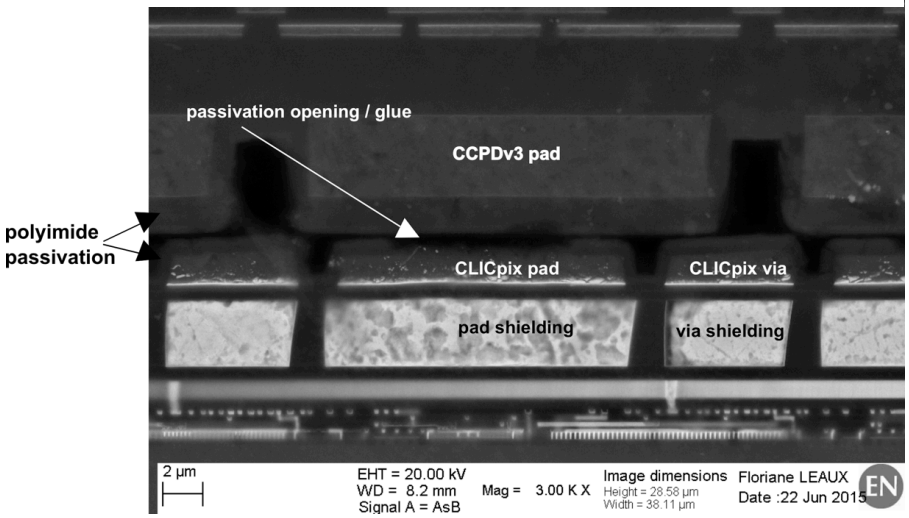
Capacitive Coupled Pixel Detector (CCPD)

- HV-CMOS chip as integrated sensor+amplifier
- Capacitive coupling from CSA output to r/o chip through layer of glue → no bump bonding!
- CCPDv3 test chip for ATLAS FEI4 and CLICpix (KIT, CERN, Geneva, others)
- Proof-of-principle test-beam measurements
- Systematic studies of glue parameters and device calibration ongoing





SEM picture CLICpix-CCPDv3 assembly



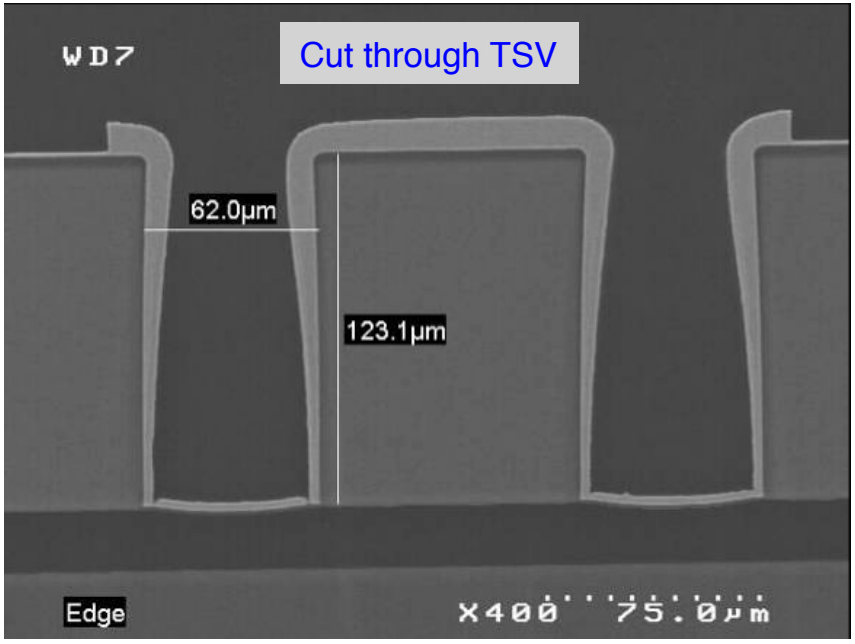
Interconnect R&D

Through Silicon Via (TSV): vertical electrical connection

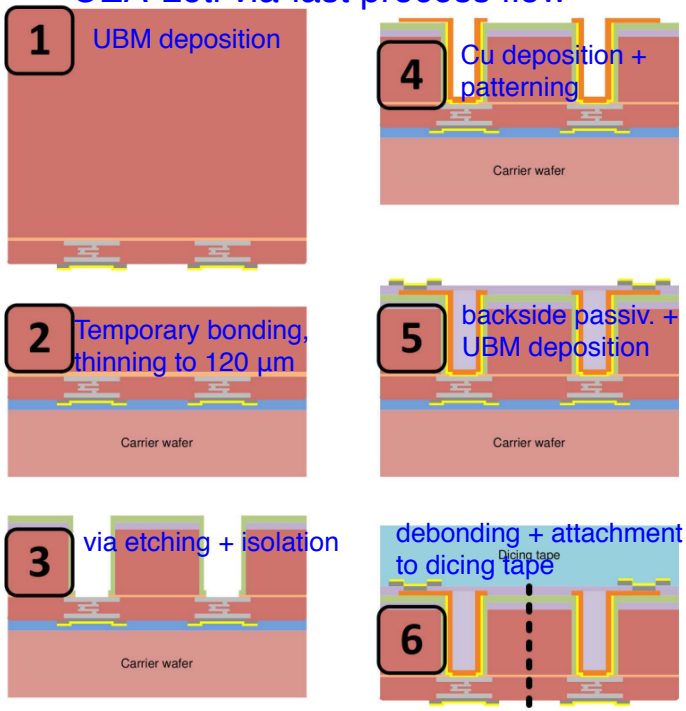
→ Eliminates need for wirebonds
→ 4-side buttable chips
→ Increased reliability, reduced material budget

TSV project (ALICE, CLIC, ACEOLE, AIDA) with CEA-Leti

- 130 nm Medipix(RX)/Timepix3 wafers, via-last process
- 1st phase: demonstrated feasibility
- 2nd phase: demonstrated good yield
- 3rd phase: TSV with 50 µm wafer thickness produced
- Next: establish wafer-to-wafer direct bonding of thinned 8" sensor and ASIC wafers

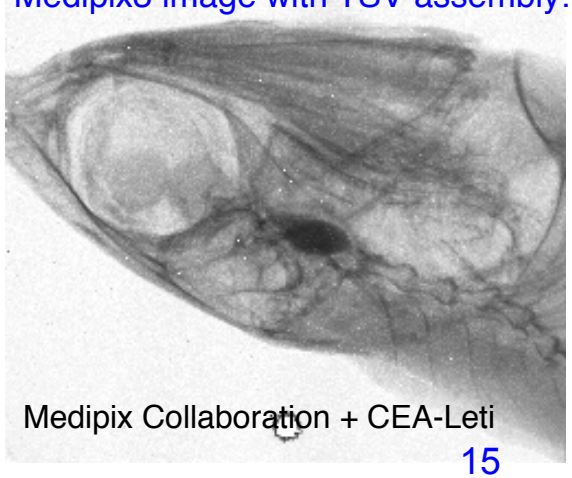


CEA-Leti via-last process flow



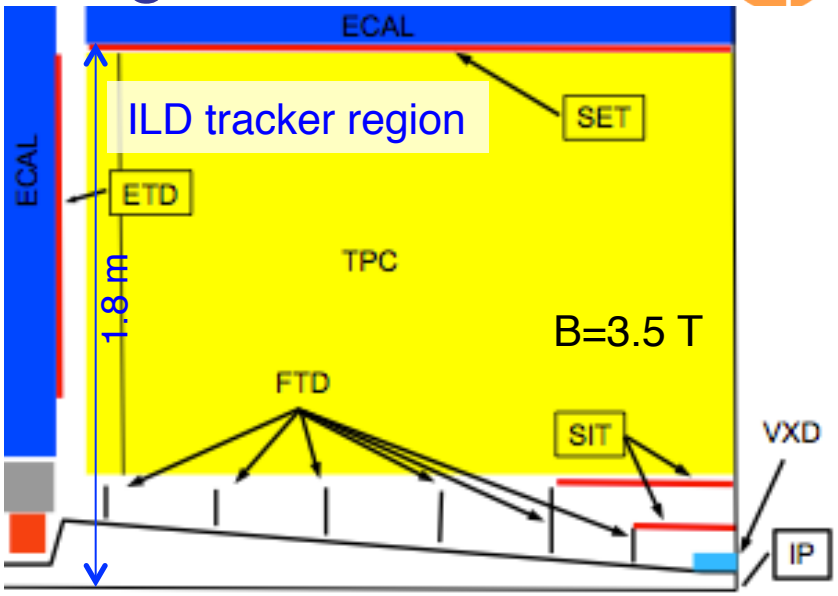
http://iopscience.iop.org/1748-0221/6/11/C11018/pdf/1748-0221_6_11_C11018.pdf

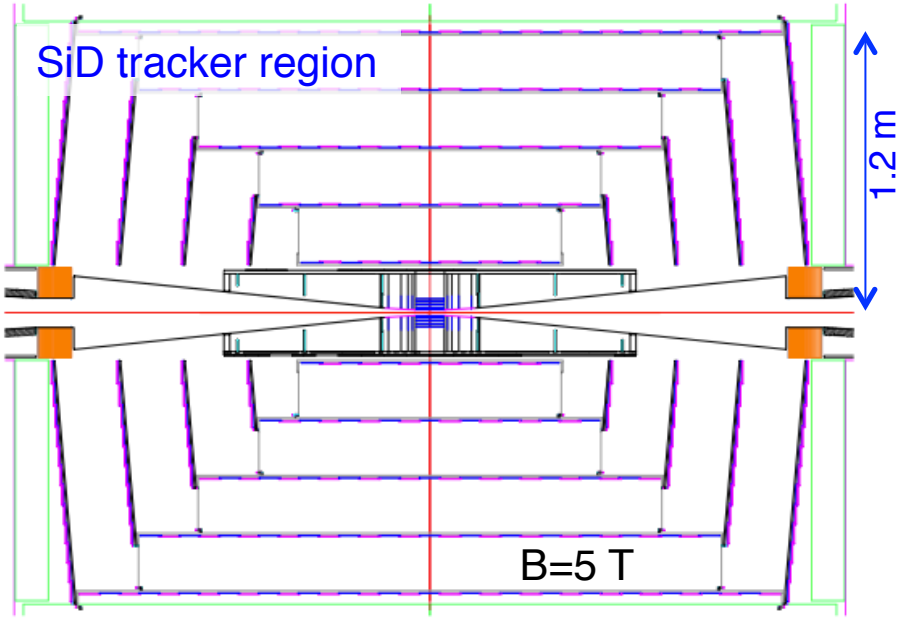
Medipix3 image with TSV assembly:

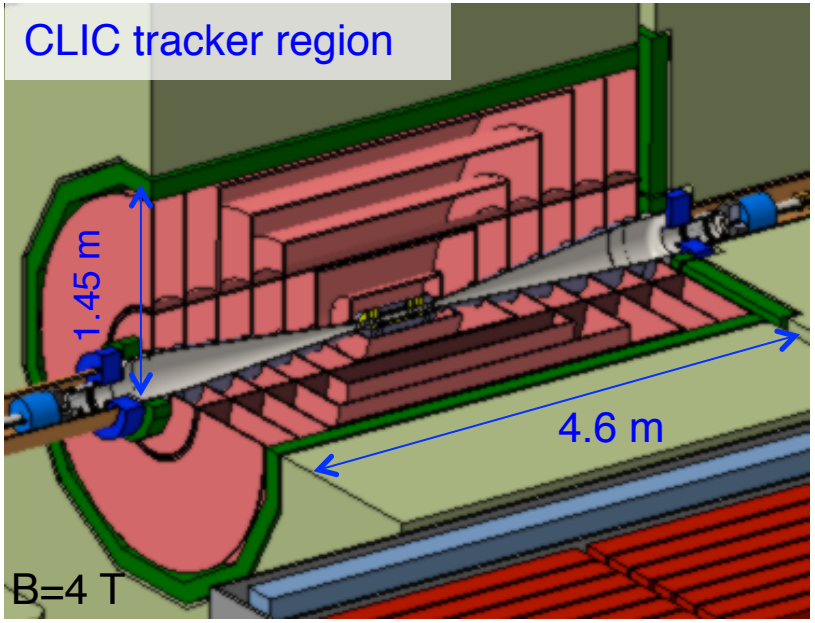


LC outer tracking

- Very good momentum resolution required (Higgs mass measurement, PFA):
  $\sigma(p_T)/p_T^2 = 2\text{-}5 \times 10^{-5}/\text{GeV/c}$
- Different concepts, all with large BR^2/σ:
  - SiD, CLIC: all-silicon tracker with 5 barrel layers, 4-7 forward disks
  - ILD: silicon + gaseous tracking (TPC) up to 228 hits per track
  - 1.2 - 1.8 m outer radius (~80-180 m^2 silicon)
  - Long strips for ILC sufficient, CLIC needs higher granularity (~1 mm "strixels") for inner layers because of large BG levels



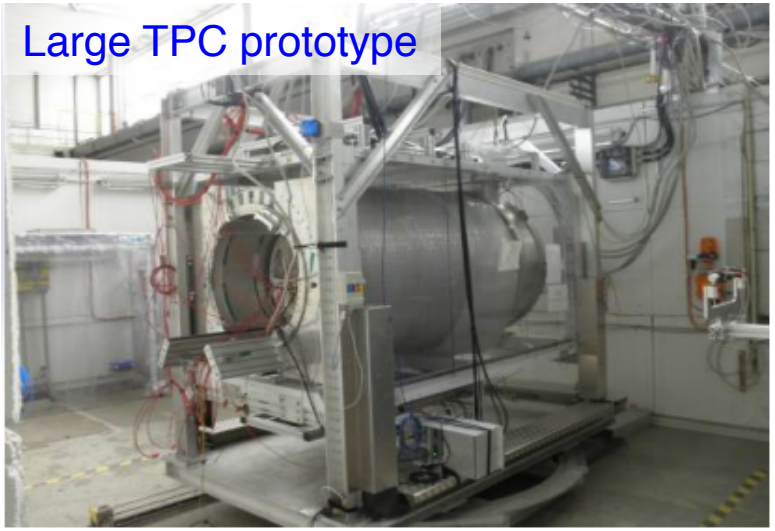




Time Projection Chamber (TPC)

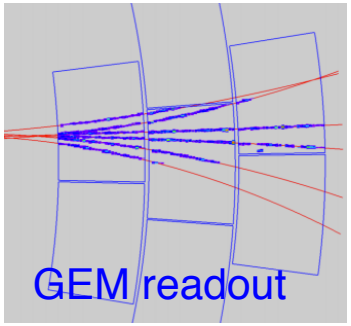
Active R&D on TPC readout and integration (LCTPC)

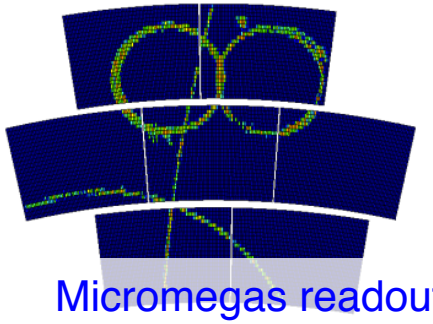
- Large prototype built and operated in test beams with various r/o technologies and in B field:
  - Micromegas (CEA, Carleton)
  - Double/Triple GEM (DESY, Asia)
  - InGrid Pixel TPC (Bonn, NIKHEF, CEA):
- Performance meets ILD requirements
- Ongoing reconstruction / pattern-recognition studies



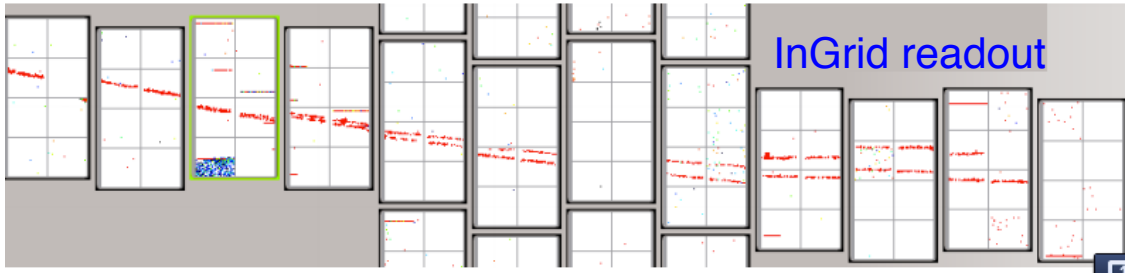
Conceptual challenges are being addressed:

- Limited hit timing and momentum resolution
  → silicon envelope requirements under study
- Ion back flow limits resolution
  → gating concepts under study
- Material in field cage and end plates
  → optimization ongoing





Recent development:
TPC tracker for CEPC
Chinese Circular Collider

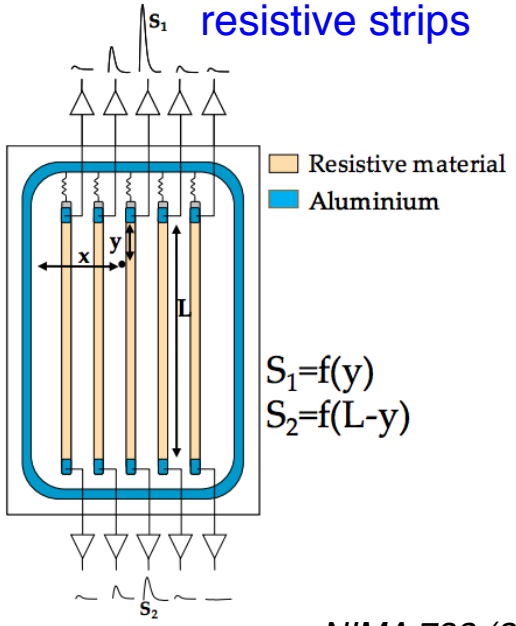


Strip sensors with charge division

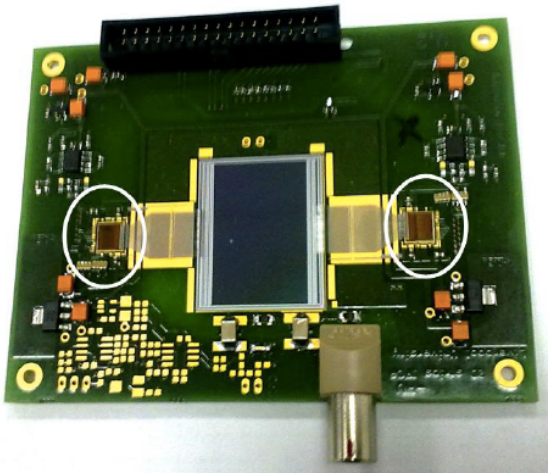
Poly-strips sensors for ILD@ILC:

- 2d-sensitive strip sensors with charge division (CNM, IFCA, KIT-CMS)
- Highly doped silicon strips, 2 r/o channels / strip
  → charge division according to position along strip
- Proof of principle measurements with laser and in CERN test beam
  ~1% fractional position error achieved (20% signal loss for 20 mm strips)
- New / ongoing work on further improvements:
  - Routing for same-side readout
  - Cross-talk reduction and signal-loss minimization

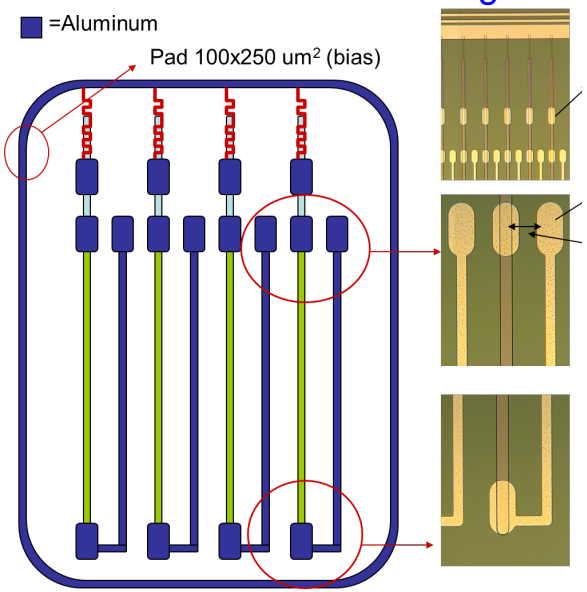
resistive strips



Polystrips sensor prototype



Same-side readout routing



NIMA 732 (2013) 186–189

Low-Gain Avalanche Diodes (LGAD)

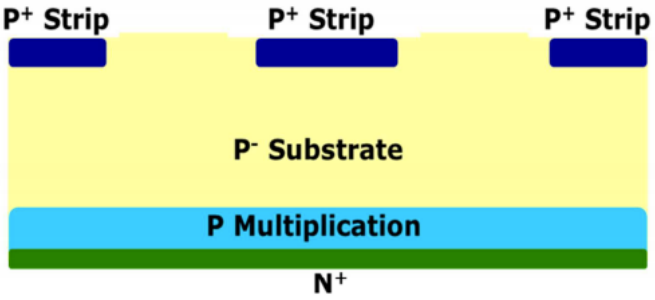
Low Gain Avalanche Diodes (LGAD):

- Tune doping profiles inside sensor, creating small volume with very high field

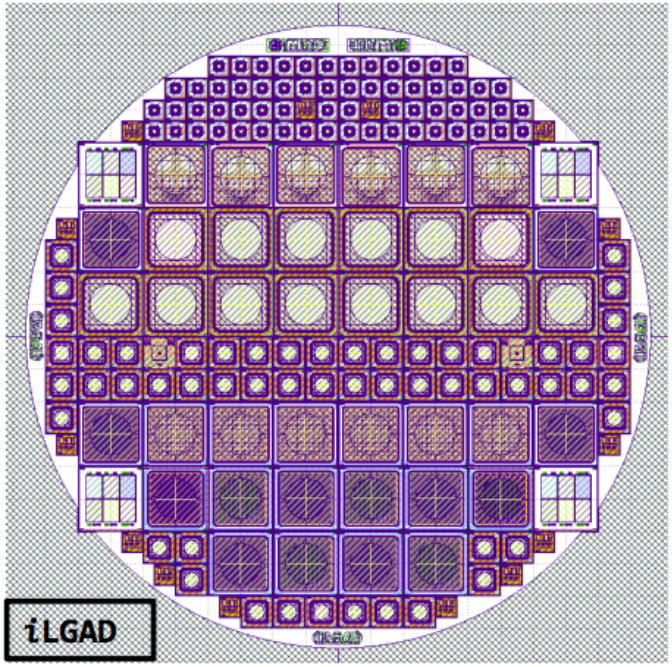
→ Charge multiplication (~10x) results in fast and large signal even in very thin sensors

- Works well for larger structures
- Recent progress for finer pitch (strips, pixels): iLGAD with multiplication volume at backside
  - TCAD simulations show improved uniformity w.r.t. conventional LGAD
  - MPW production at CNM started (RD 50 project)

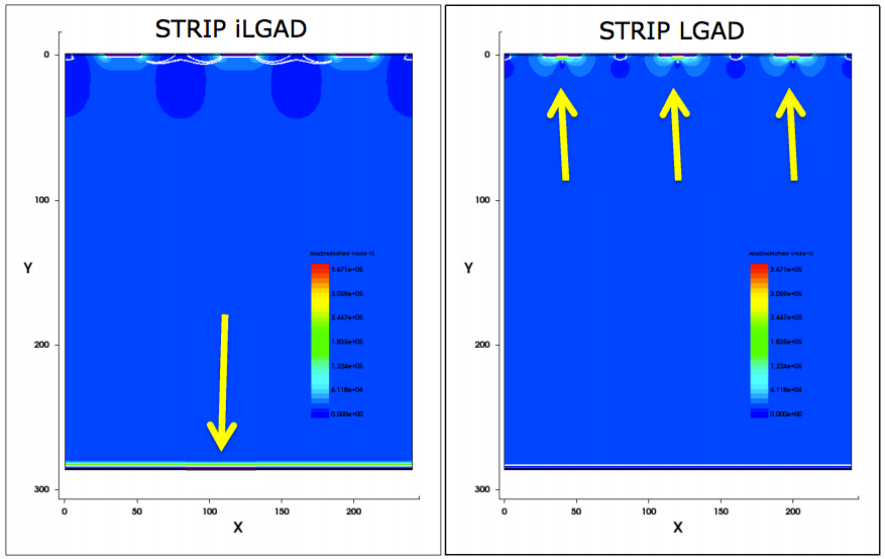
iLGAD micro strips



iLGAD MPW mask



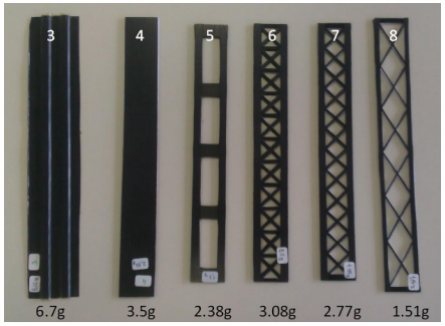
TCAD simulations



Detector integration

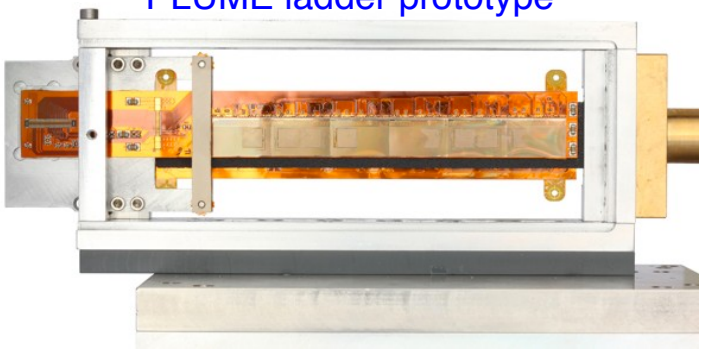
- Development of realistic detector-integration concepts in several domains
- Close link between readout R&D and mechanics/powering/cooling studies
- Results need to be incorporated in physics performance simulation studies

CFRP support prototypes

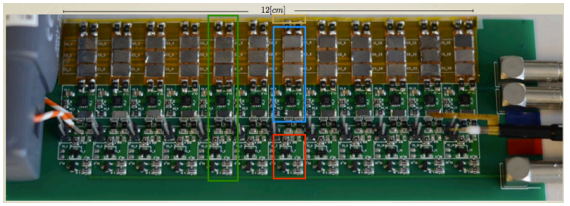


X/X0					
0,156 %	0,134 %	0,091 %	0,118 %	0,106 %	0,058 %

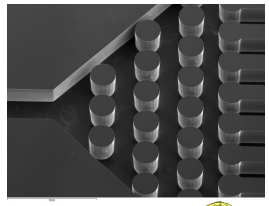
PLUME ladder prototype

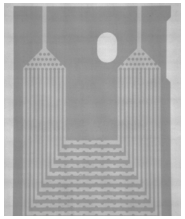


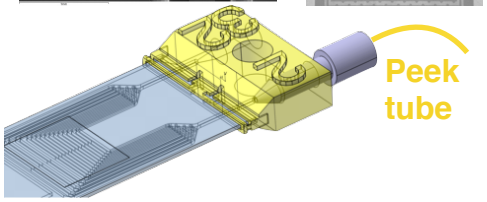
CLIC vtx power-pulsing demonstrator



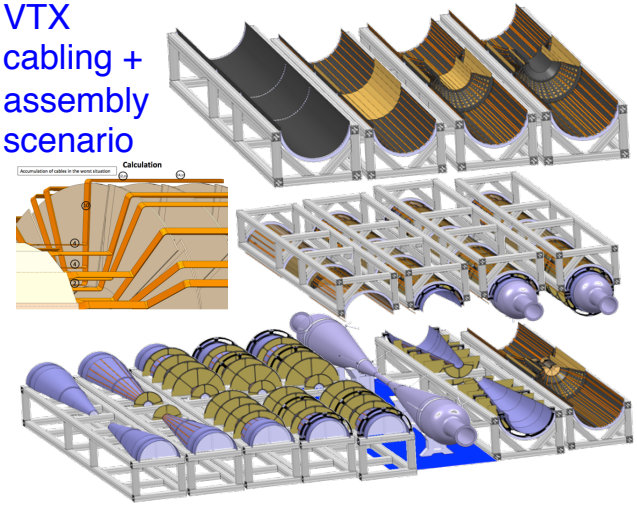
DEPFET micro-channel cooling



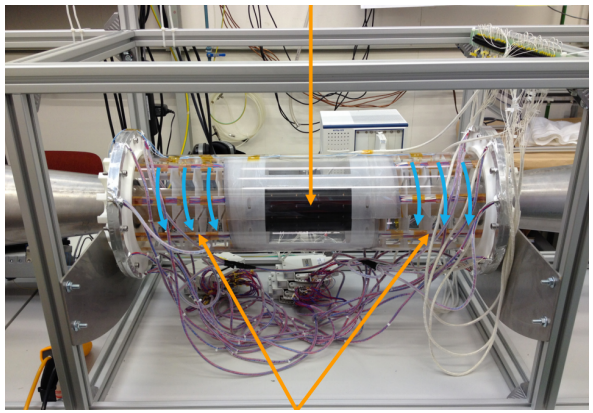




VTX cabling + assembly scenario



CLIC vertex air-cooling mockup



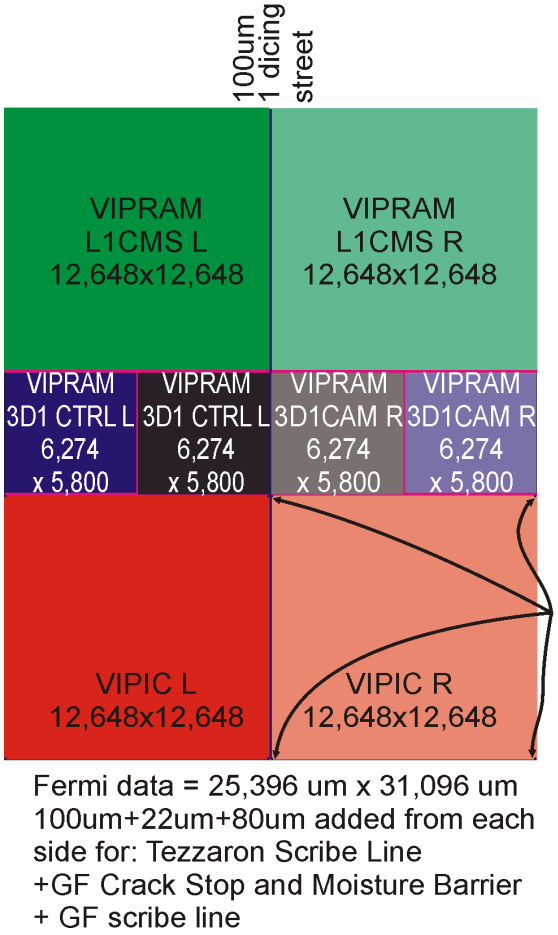
Summary / Conclusions

- Demanding requirements and ambitious concepts for LC vertex- and tracking detectors
- Examples for R&D on high-resolution pixel detectors for LCs:
  - ILC: mainly integrated technologies, ~µs timing
  - CLIC: hybrid and integrated technologies, ~10 ns timing
  - Promising developments in 3D technologies
- Examples for R&D on silicon-strip detectors and TPC
- Mechanical integration, powering, cooling are essential parts of technology R&D
- LC projects profit from advancements in micro-electronics technology (smaller feature sizes) and from synergy with approved experiments

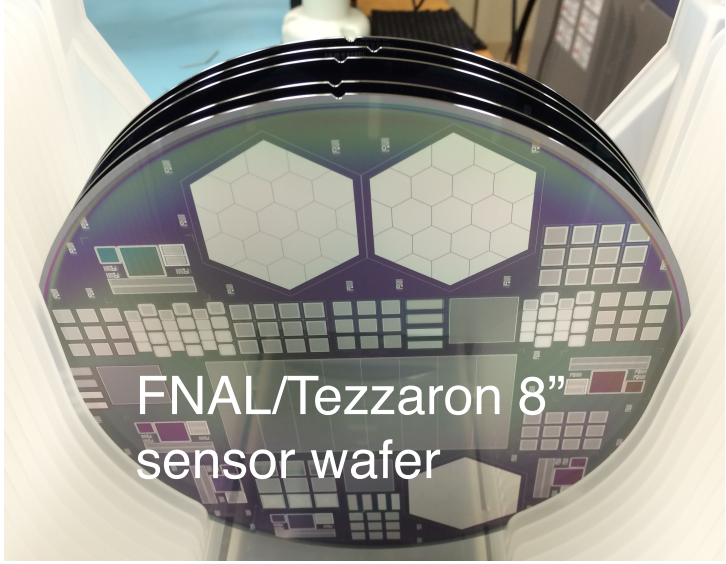
Thanks to Ron Lipton, Alberto Ruiz, Marcel Vos and Marc Winter for providing input and to everyone else from whom I took material for this talk!

Additional material

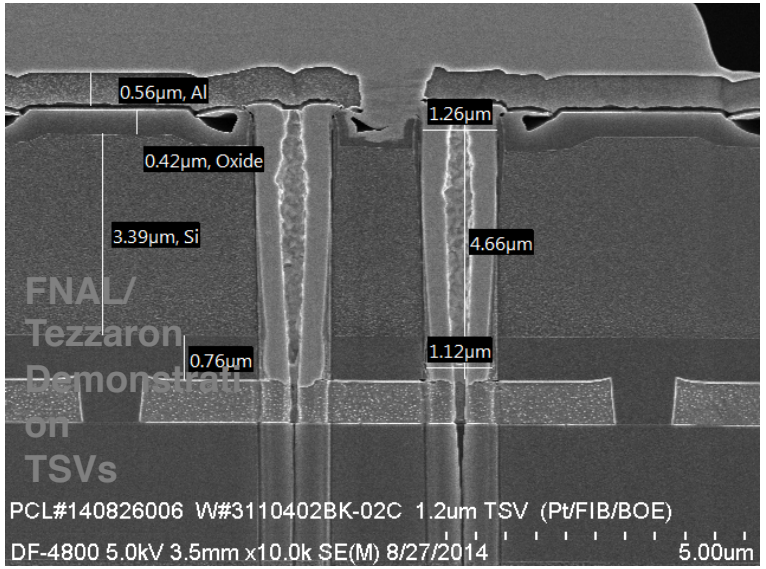
3D Work Images



Fermi data = 25,396 um x 31,096 um
100um+22um+80um added from each side for: Tezzaron Scribe Line
+GF Crack Stop and Moisture Barrier
+ GF scribe line

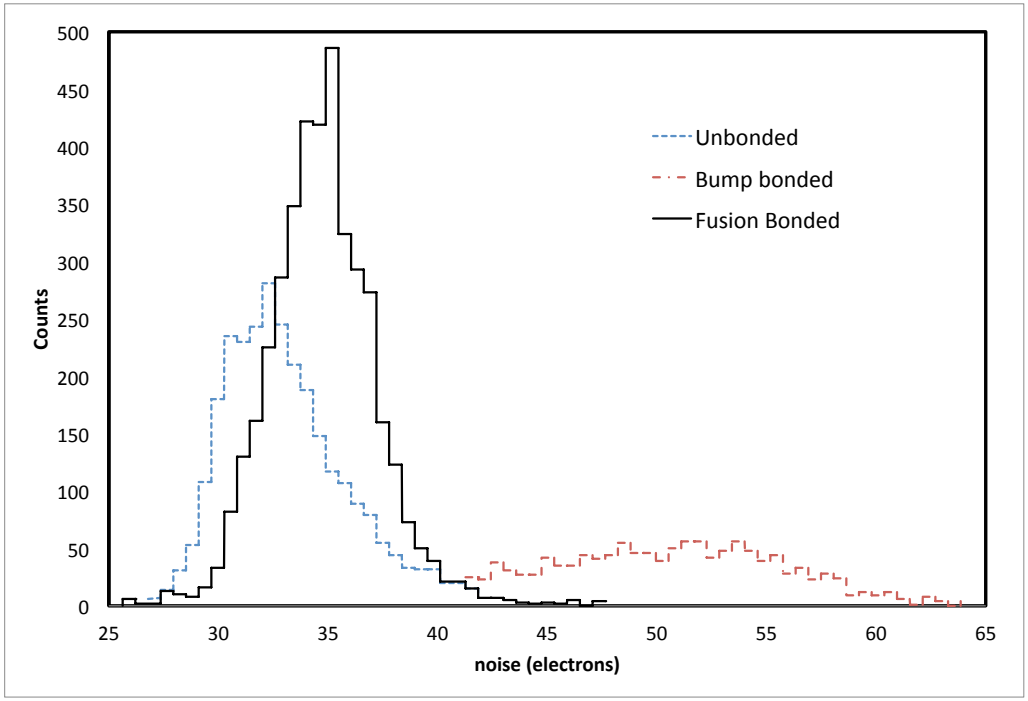


R. Lipton



Noise measurements 3d assemblies

For the VIPIC x-ray imaging chip we were able to compare noise of the oxide-bonded pixels to the same chip with bump bonds.
The noise in the oxide bonded pixels is almost a factor of two lower than the conventionally bump bonded parts due to lower capacitance.

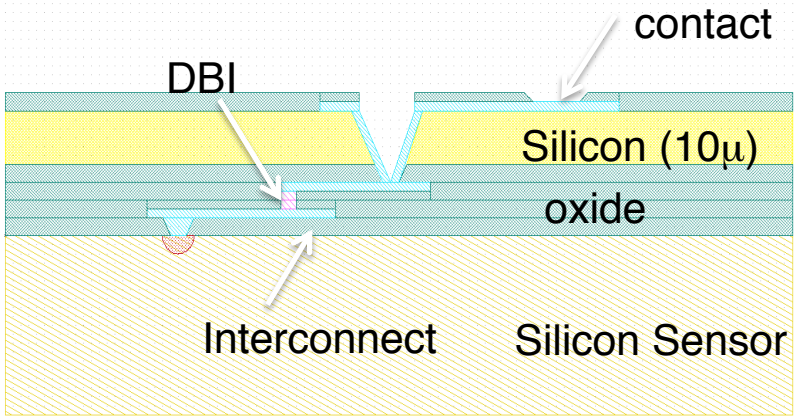


R. Lipton

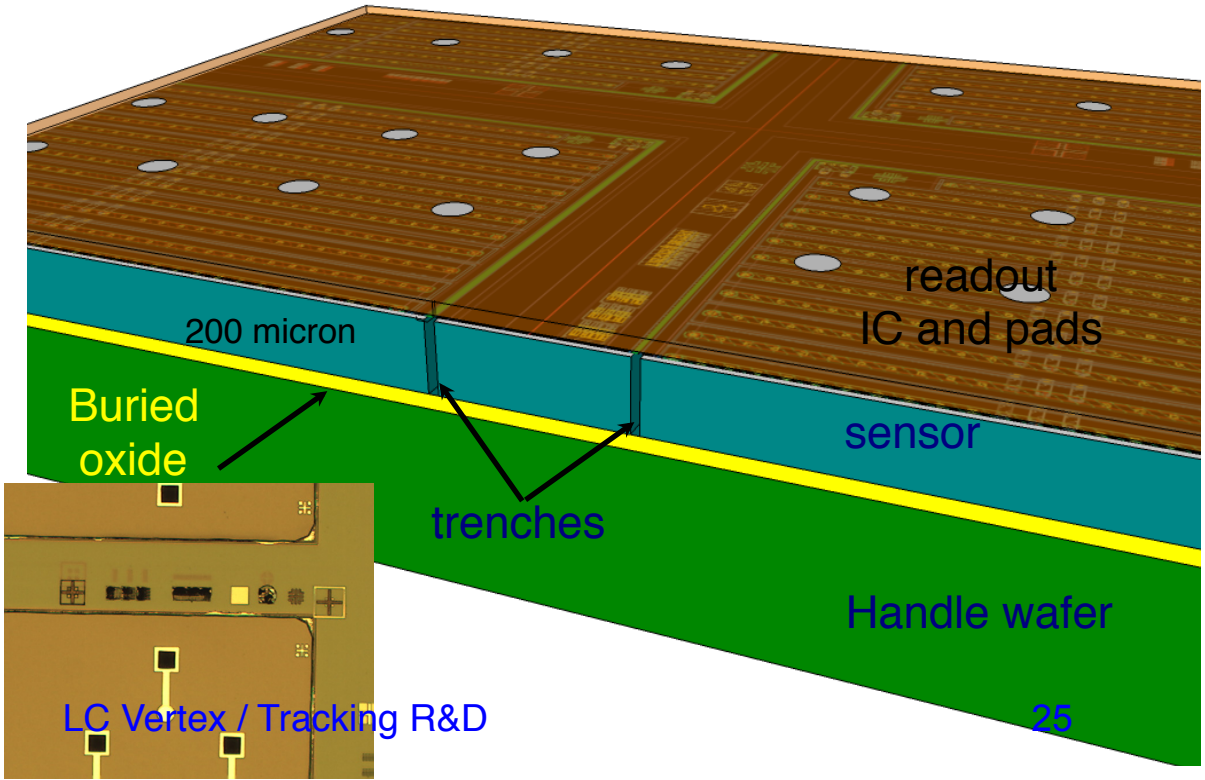
How to build large area intelligent trackers?

Combine active edge technology with 3D electronics and oxide bonding with through-silicon interconnect to produce fully active tiles.

- These tiles can be used to build large area pixelated arrays with good yield and reasonable cost
- Tiles can populate complex shapes with optimal tiling and low dead area
- Only bump bonds are large pitch backside interconnects
- High density and geometrical flexibility



R. Lipton



DEPFET one-slide status report

PXD9 pilot wafer number

Sensor type	W30	W35	W36
IF	0	98.44	98.96
OF1	100.00	98.44	98.96
OF2	99.48	98.96	99.48
OB1	97.72	99.40	0
OB2	99.48	0	98.96
IB	97.92	0	99.48
Total	**83.3**	**66.6**	**83.3**

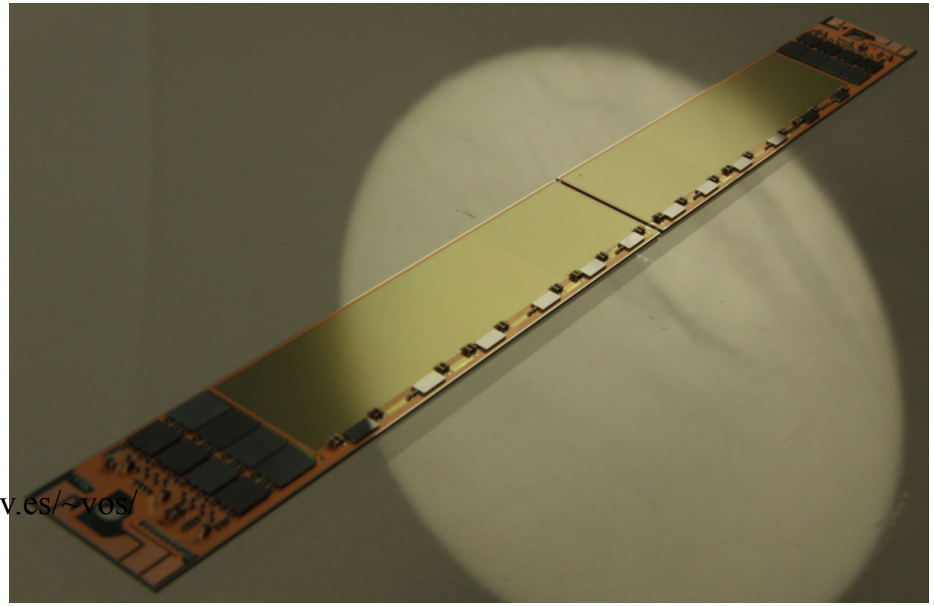
DEPFET sensor yield results after all production steps

Executive summary:

4/18 sensors have fatal shorts
14/18 (78%) sensors are working
10/18 (56%) are grade A

Electrical tests with ASICs mounted on Silicon: noise performance as expected

First complete assembled Belle II (double-) ladder: fully functional



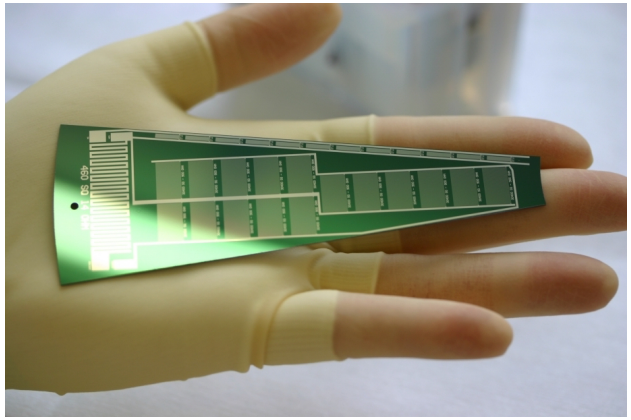
supporting paper for ILC TDR/DBD
in IEEE TNS 60, 2, 2 (2013)

Report for ECFA review, June 2014 http://ific.uv.es/~vos/ECFA_DEPFET.pdf

LC thermo-mechanics of thin sensors

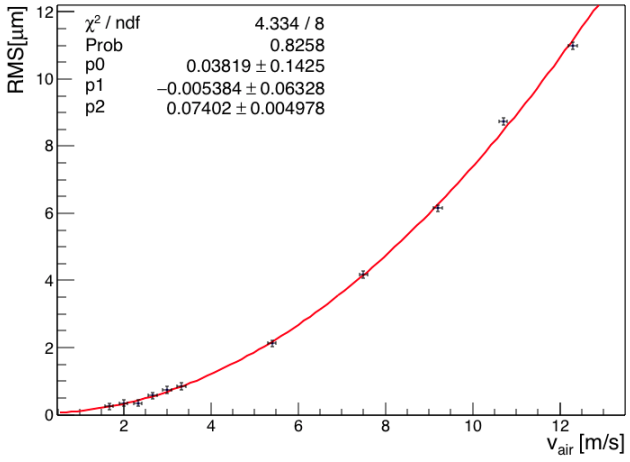
Solution for forward disks

Adapted ladder design → all-silicon petal
Mock-up for ILD FTD1-2 under construction

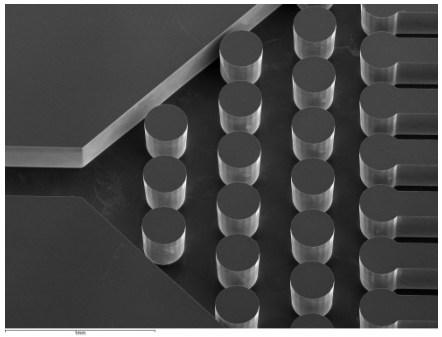


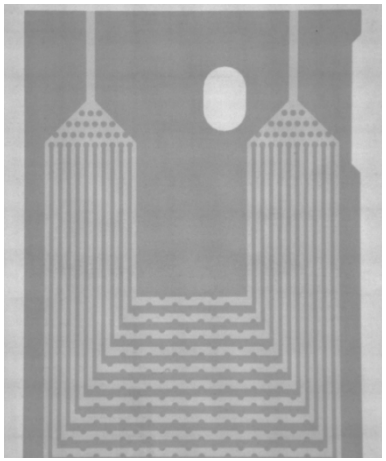
Thermo-mechanical performance of ultra-thin sensors in LC environment

Power pulsing very effective: DT = 3 K, without cooling!
No impact on mechanical stability
Gentle air flow (1 m/s) is enough to remove heat;
induced vibrations are small

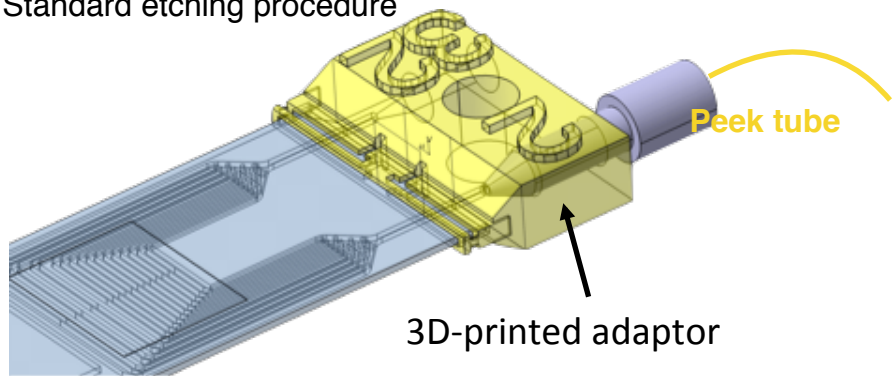


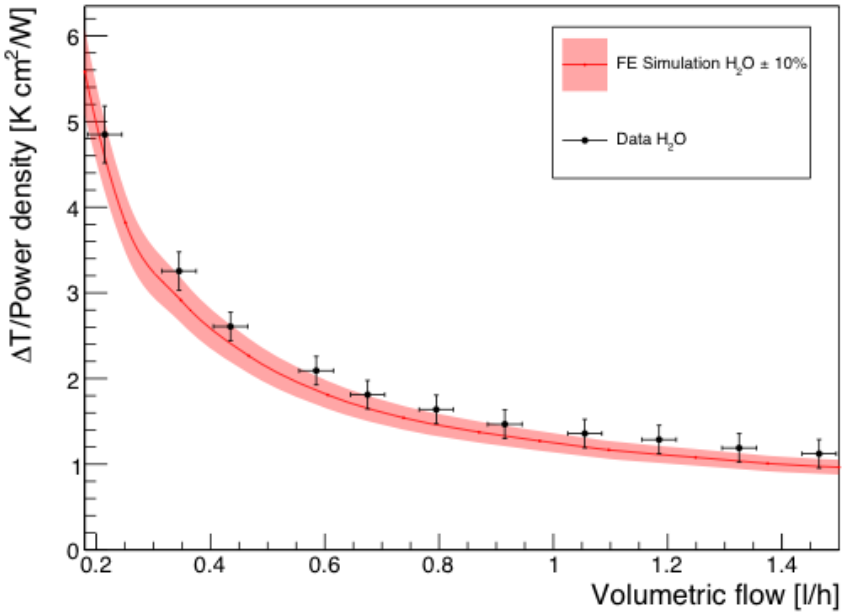
Micro-Channel Cooling on ultra-thin Silicon sensors





Micro-channel pattern in handle wafer
Standard etching procedure





Low cost mono-phase fluid: H_2O

Low volumetric flow (~1l/h) and low pressure (< 1bar) are enough to dissipate the heat in the front end

Good agreement with the FE simulation inside an error area of 10%

Thermal Figure of Merit (TFM) of ~ 1 K·cm²/W

See talk in Vertex/Tracking session on Tuesday
Advanced vertex detector cooling concepts: from air flow to micro-channel cooling
M.A. Villarejo, I. Garcia (IFIC Valencia)

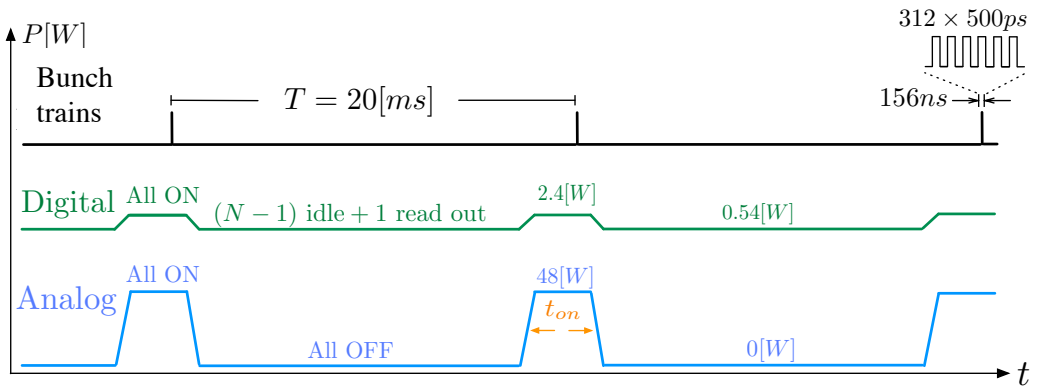
CLICpix power-pulsing + delivery requirements

Small duty cycle of CLIC machine allows for power reduction of readout electronics: turn off front end in gaps between bunch trains

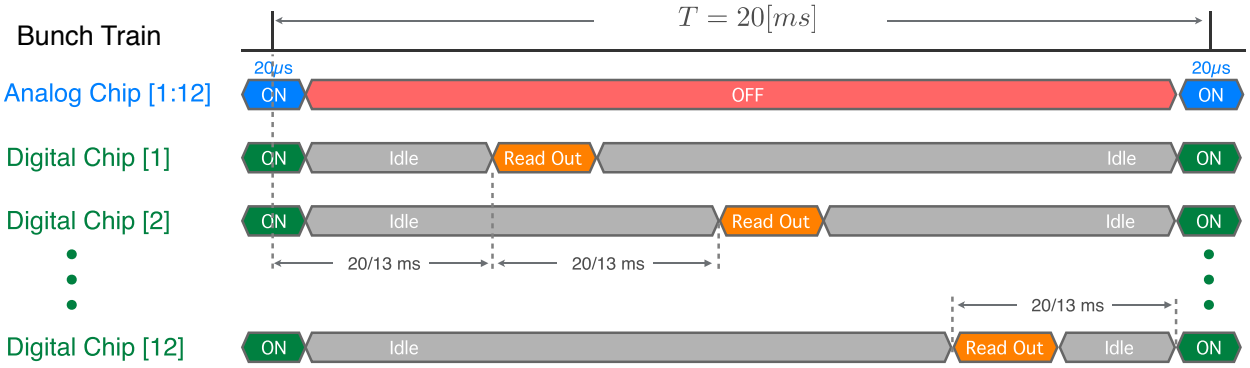
Challenging requirements:

- Power budget **<50 mW/cm²** average (air-flow cooling limit)
- High peak current **> 40A/ladder**
- Different timing **analog/digital** electronics
- High magnetic field **4-5 T**
- Material budget **< 0.1% X_0** for services+supports
- Regulation **< 5% (60 mV)** for analog part

Vertex-detector power consumption



CLICpix powering states



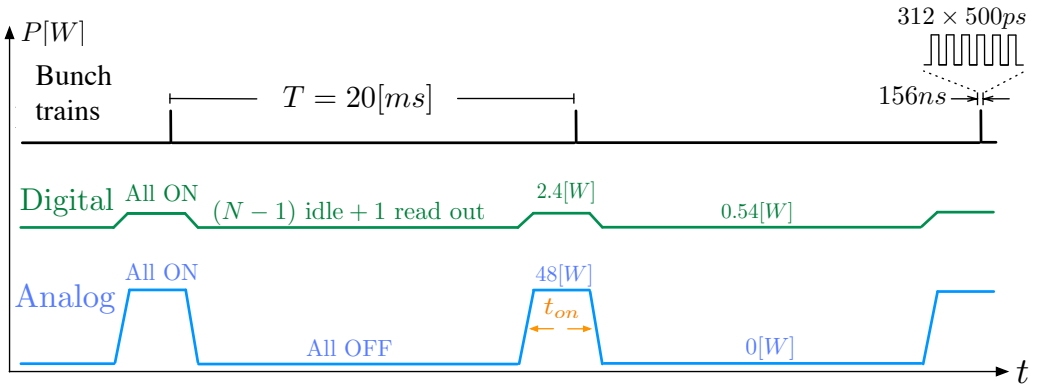
C. Fuentes, X. Llopart, P. Valerio

CLICpix power-pulsing + delivery concept

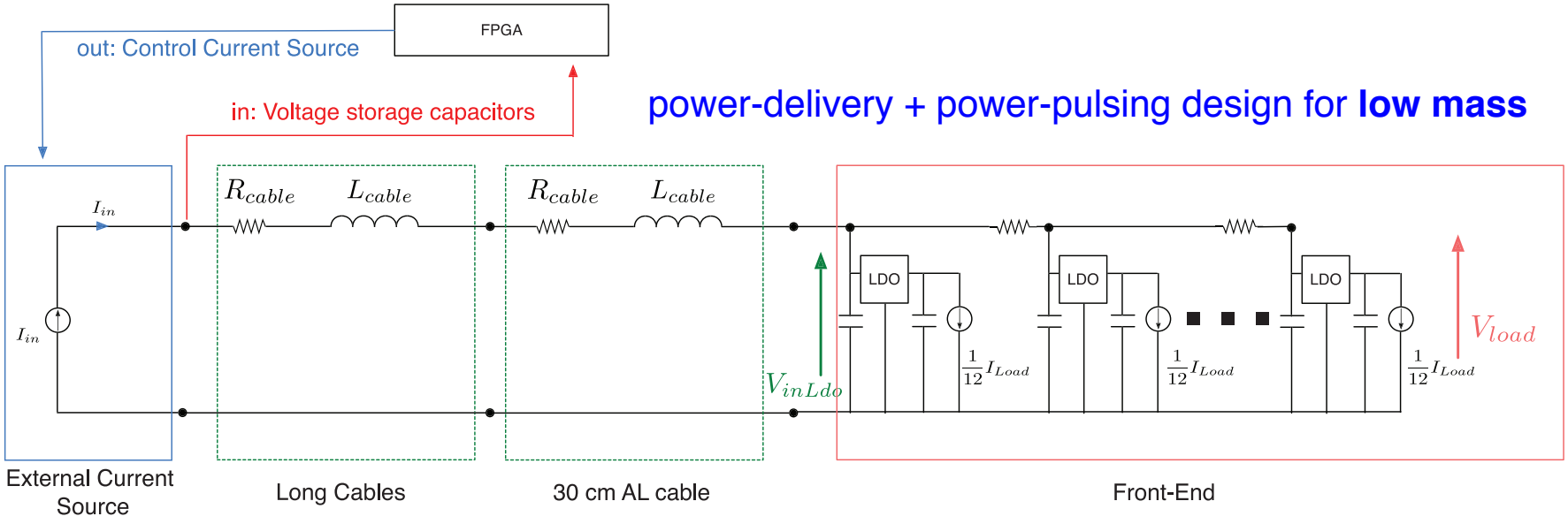
Small duty cycle of CLIC machine
→ turn off front end in gaps between bunch trains, to reduce avg. power

- Power pulsing with local energy storage in Si capacitors and voltage regulation with Low-Dropout Regulators (LDO)
- FPGA-controlled current source provides small continuous current
- Low-mass Al-Kapton cables

Vertex-detector power consumption



C. Fuentes

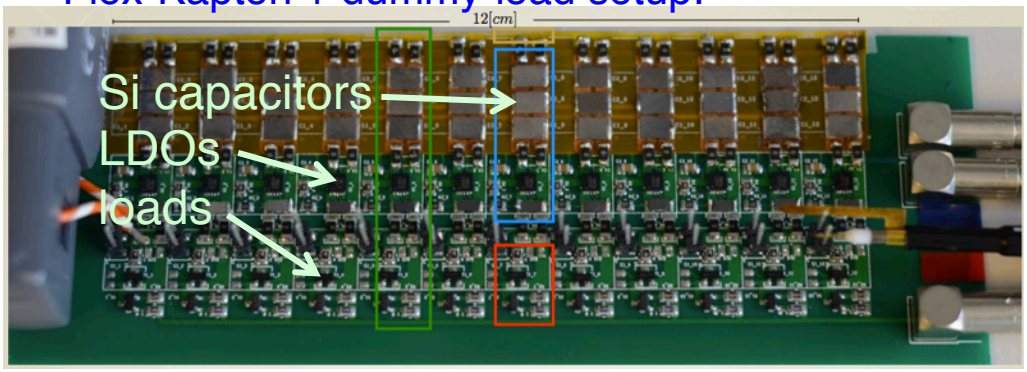


power-delivery + power-pulsing design for **low mass**

CLICpix power-pulsing + delivery results

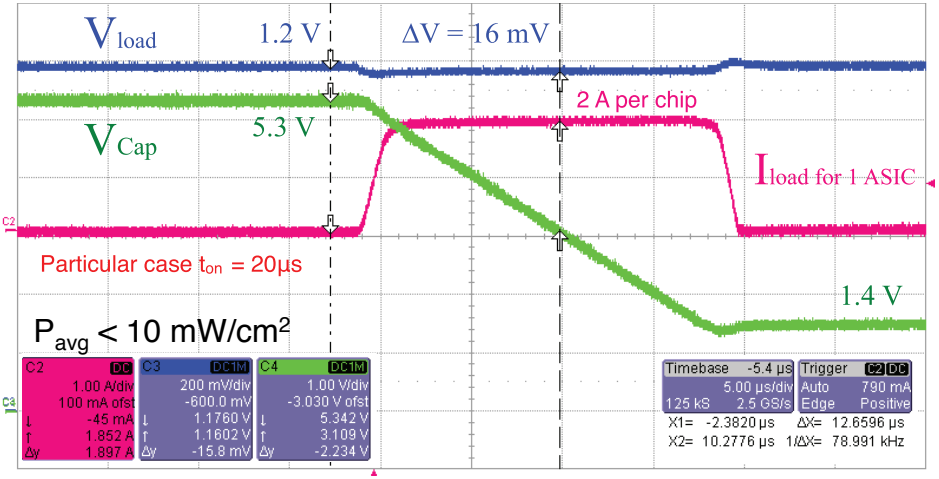
- Measurements on prototypes for digital and analog powering of ladders:
  - I_{ladder}<300 mA; P<45 mW/cm^2
  - Voltage stability: ΔV~16 mV (analog), ~70 mV (digital)
  - ~0.1% X_0 material contribution, dominated by Si capacitors
  - Can be reduced to ~0.04% X_0 with evolving Si capacitor technology: 25 µF/cm^2 → 100 µF/cm^2

Flex-Kapton + dummy-load setup:

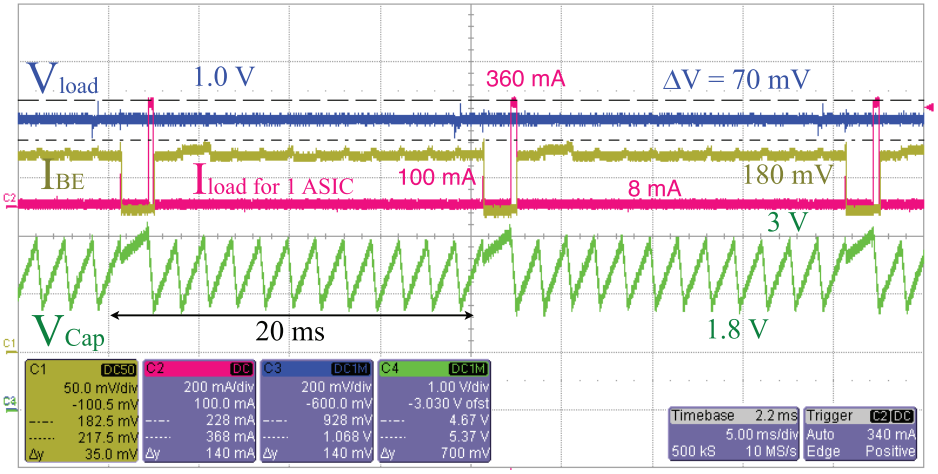


C. Fuentes

analog power

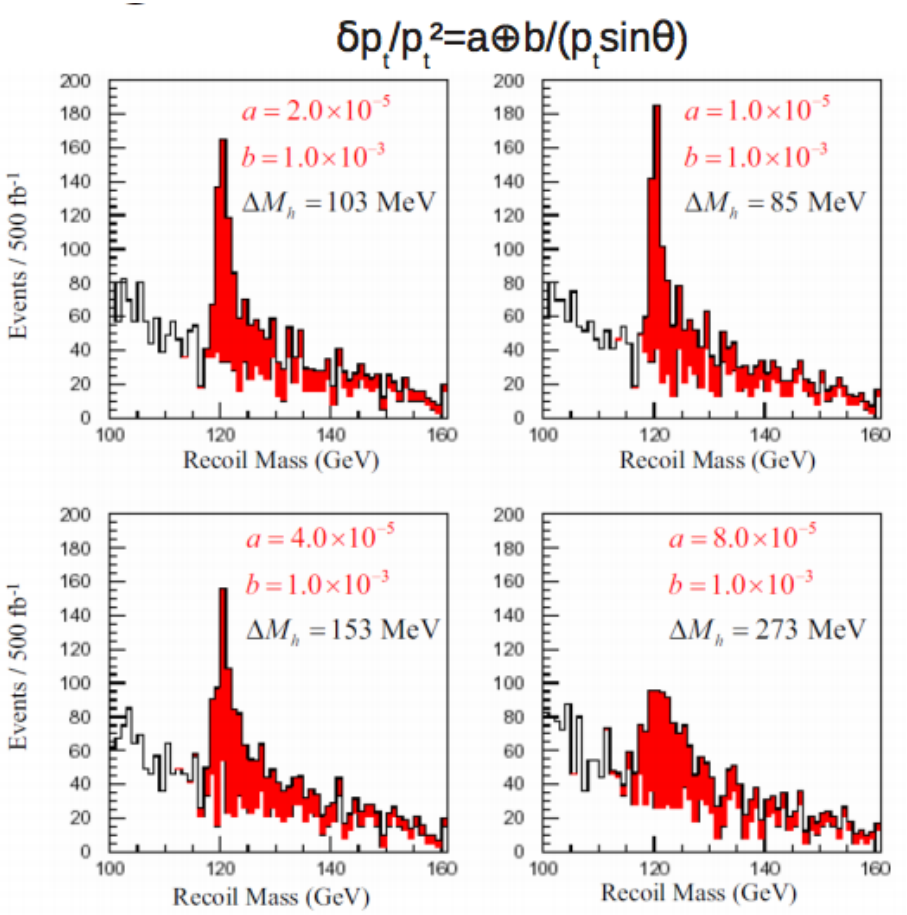


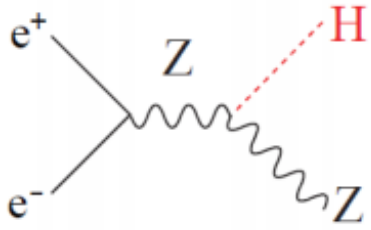
digital power

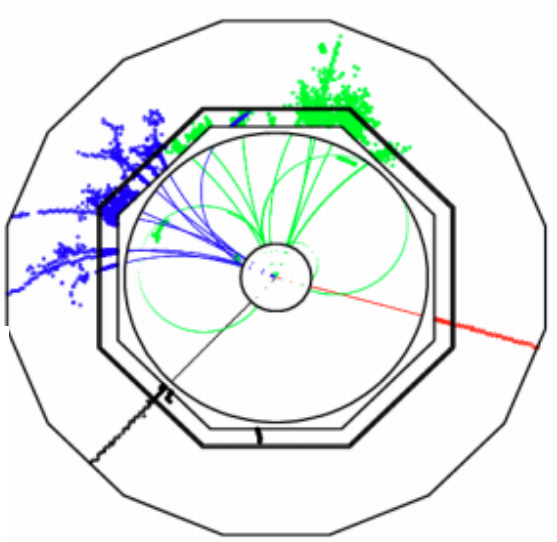


LC tracking requirements

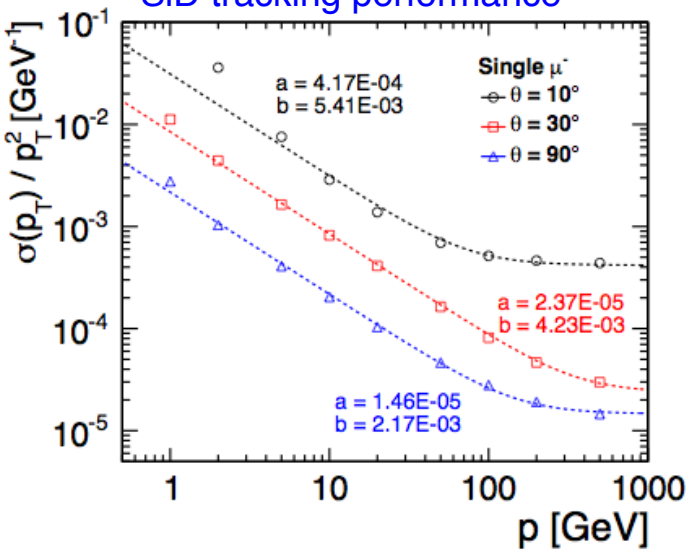
- Higgs mass measurement through recoil
  → requires $\sigma(p_T)/p_T^2$=2-5x10^{-5}/GeV/c
- Particle-Flow Algorithm (PFA) requires efficient tracking, good two-track separation in high-rate environment
- detectors optimized for high BR^2/σ







SiD tracking performance



SiD silicon tracking

All silicon tracker

- barrel: 5 single-sided strip layers, 0.2 m < R < 1.22 m
- endcaps: 4 false double layers, 0.8 m < z < 1.64 m

Sensors:

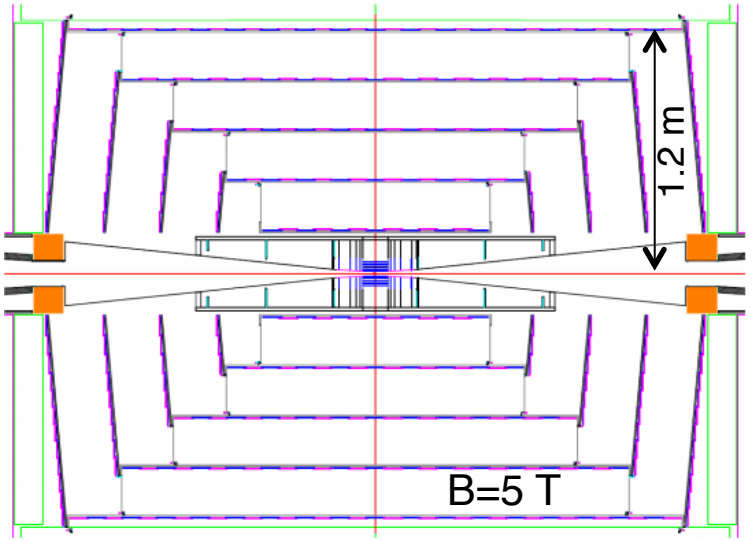
- 10x10 cm^2 sensors, 50 µm pitch, d=300 µm, A/C coupl.
  Hamamatsu prototypes exist

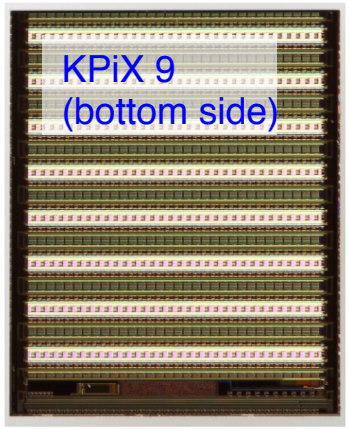
Readout:

- 2 KPiX-A r/o chips per sensor: 1024 ch., 4 buffer / ch.
- single ILC bx time stamping (~500 ns)
- <20 mW / chip (with power pulsing)
- 600 W total power → gas cooling

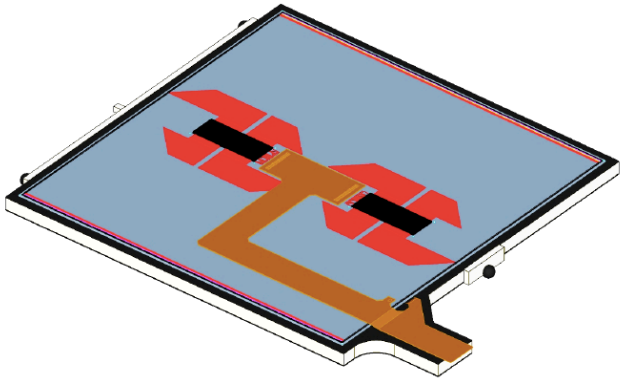
Integration:

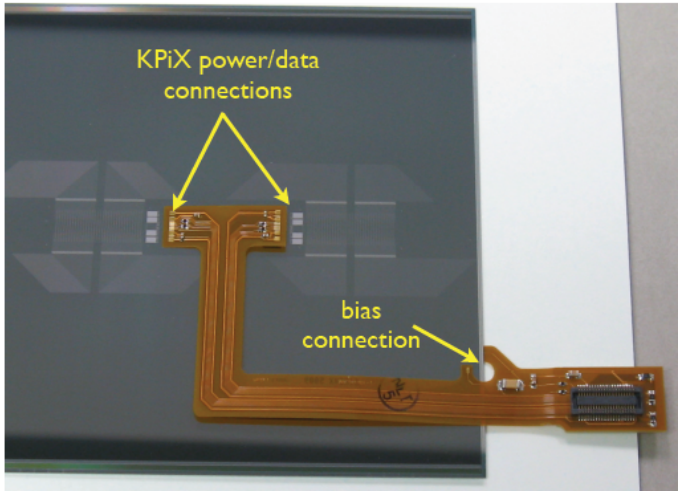
chip on sensor, integrated pitch adapter
(SiLC development, also used for ILD and CMS upgrade)
→ no sensor overlap needed





Chip-on-sensor module





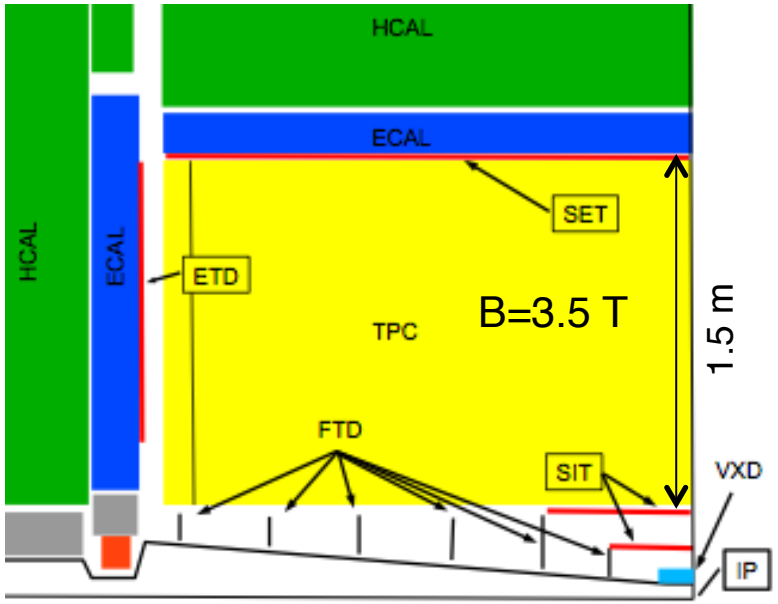
ILD silicon tracking

Si strip tracking around TPC and in forward region:
- 3 barrel + 5 fwd false double layers + 1 fwd single layer

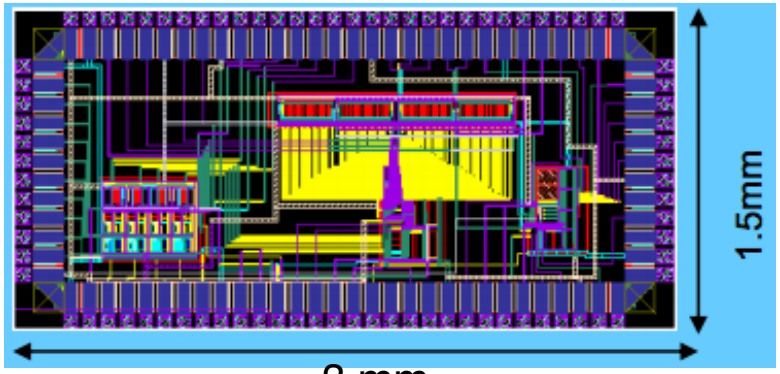
Sensors:
- 10x10 cm^2 sensors, AC-coupled p-on-n, 50 µm pitch, edgeless (<=100 µm inactive edge), d=200 µm

Readout:
- SiTR ASIC in 130 nm (SiLC development)
- analog pipeline, low-noise OpAmp, 8-bit ADC
- prototype exists
- 65 nm technology foreseen for next generation
- 6-9 mW/cm^2 power dissipation → air cooling

Integration:
- SiLC integrated pitch adapter (same as for SiD)
- Fibre Bragg Grating Monitoring alignment system (IFCA)



SiTR-130-4 readout chip prototype



Fibre Bragg Grating Monitoring and alignment system