Development of CMOS Pixel Sensors for Tracking Devices at the ILC

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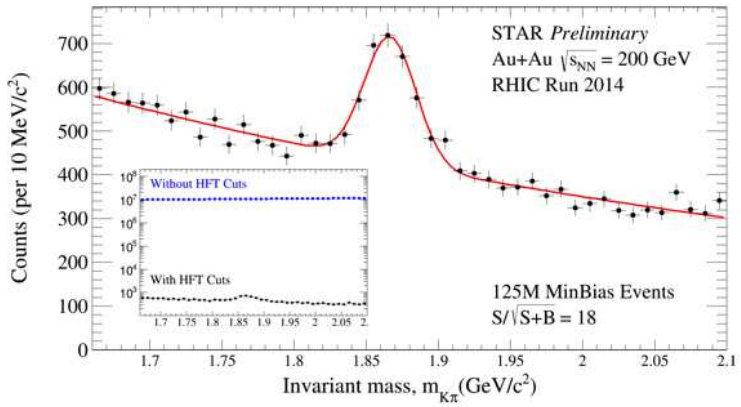
Contents

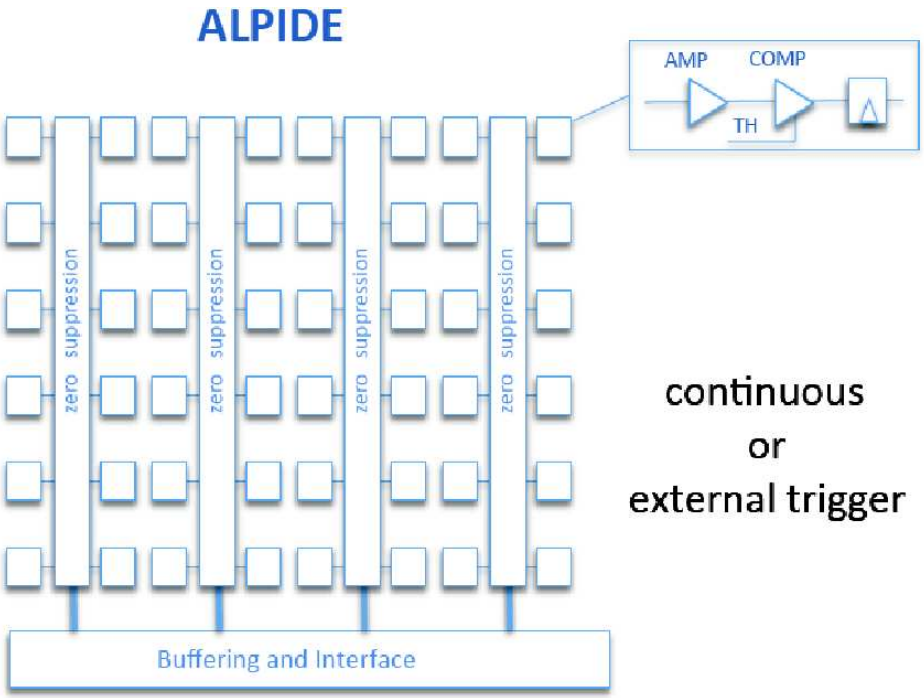
Context of CPS Development

- **Main current R&D activity of PICSEL team :**
  - R&D of CPS in a 0.18 μm quadruple-well CMOS process
  - targetted applications : vertex detectors AND trackers
  - driving R&D framework : ALICE-ITS upgrade followed by CBM-MVD
- **3 chips under development in 0.18 μm CIS process :**
  - MISTRAL: rolling shutter similar (but faster) to ULTIMATE/STAR-PXL (0.35 μm twin-well process)
  - ASTRAL: same as MISTRAL but with in-pixel discrimination (twice faster & less power consuming)
  - ALPIDE (ITS baseline): asynchronous r.o. (HPS like), 5 X faster & 2 X less power than ASTRAL (tbc)
- **Follow-up of STAR-PXL data taking :**
  - 2 years of successful physics run with ULTIMATE (still 1 one year more) :
    $\hookrightarrow$ vertexing with 400 sensors ($360 \cdot 10^6$ pixels covering 0.15 m^2)
  - rolling shutter archi. & added value of CPS for physics assessed & validated

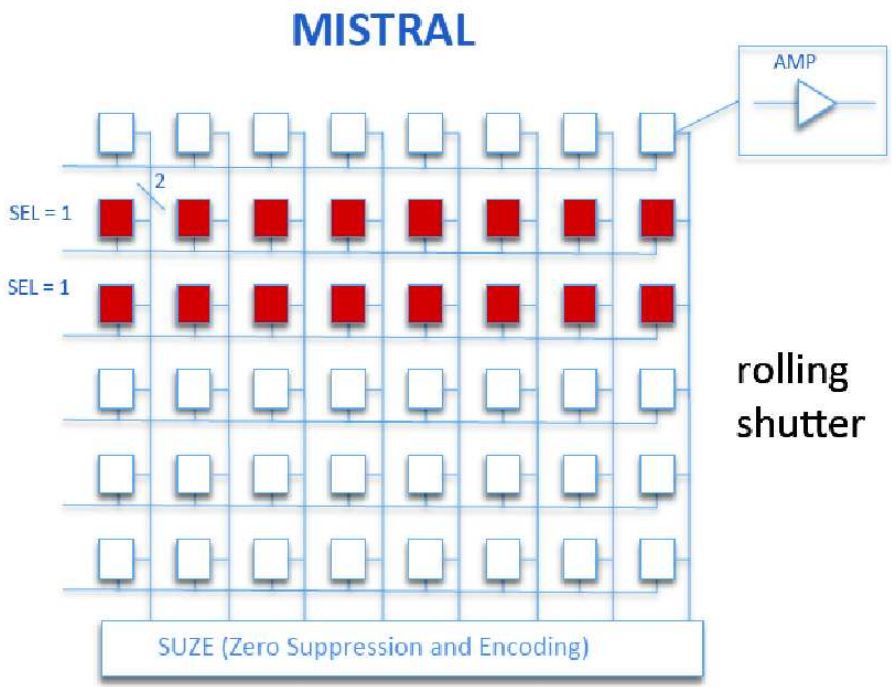


- **Next step : use CPS for trackers**
  - larger sensitive areas $\Rrightarrow$ enhanced need of sensor response Uniformity, Power saving, Robustness
  - larger distance to IP $\Rrightarrow$ alleviated requirements on :
    Occupancy handling (read-out Speed), Radiation tolerance, Spatial resolution, Material budget

ITS Pixel Sensor : Two Architectures



continuous
or
external trigger



rolling
shutter

Pixel dimensions	**27μm x 29μm**	**Pixel dimensions**	**36μm x 65μm**
Event time resolution	**4μs**	**Event time resolution**	**20μs**
Power consumption	**$<$ 50mW/cm^2**	**Power consumption**	**$\lesssim$ 90mW/cm^2**
Insensitive area	**$\sim$ 1mm x 30mm**	**Insensitive area**	**1.5mm x 30mm**

- **Both chips have identical dim. (15mm x 30 mm) as well as physical and electrical interfaces:**
  - position of interface pads
  - electrical signaling
  - steering, read-out, ... protocoles

Progress made since April 2015 (ALCW – KEK/Tokyo)

- **Performance assessment of large pixels suited to trackers**
- **Sensor design :**
  - exploiting relaxed spatial resolution and radiation tolerance requirements of outer layers
  - focusing on enhanced power saving and robustness requirements
- **2 chips extensively tested on beam :**
  - MIMOSA-22 $\equiv$ small prototype (64 x 64 pixels) featuring **large** pixels
  - FSBB $\equiv$ full scale building block of final sensor
    composed of 416x416 **small** pixels (already extensively tested)
    featuring the complete signal sensing & processing (sparsification) circuitry
- **Layout of complete sensor adapted to trackers finalised :**
  - made of 4 FSBB operated in parallel
  - each FSBB composed of 208x208 large (36x65 μm^2) pixels

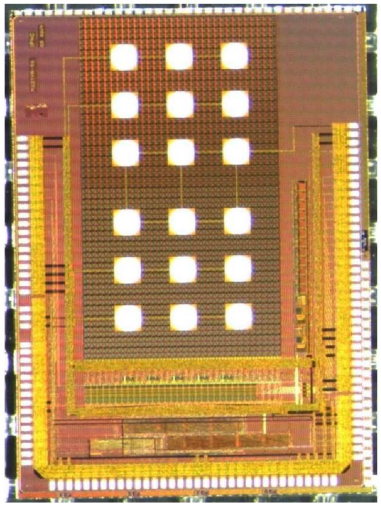
Main Features of the Sensors Studied on Beam

- **Full scale sensor building block :**
  - complete (fast) read-out chain $\simeq$ ULTIMATE
  - pixel area ($\sim$ 1 cm^2) $\simeq$ area of final building block
  - same nb of pixels (160,ooo) than complete final tracker chip
  - fabricated with 18 μm thick high-resistivity EPI
  - BUT : pixels are small (22 x 32.5 μm^2) and
    sparsification circuitry is oversized (power !)
  - **Tested at DESY (few GeV e$^-$) in June'15**
    and CERN-SPS (120 GeV "pions") in Oct. '15

FSBB-M0bis

- **Large-pixel prototype without sparsification :**
  - 2 slightly different large pixels :
    - 36.0 μm x 62.5 μm
    - 39.0 μm x 50.8 μm
  - pads over pixels (3 ML used for in-pixel circuitry)
  - fabricated with 18 μm thick high-resistivity EPI
  - BUT : only $\lesssim$ 10 mm^2, 4,ooo pixels, no sparsification
  - **Tested in Frascati (450 MeV e$^-$) in March & May'15**

MIMOSA-22THRb

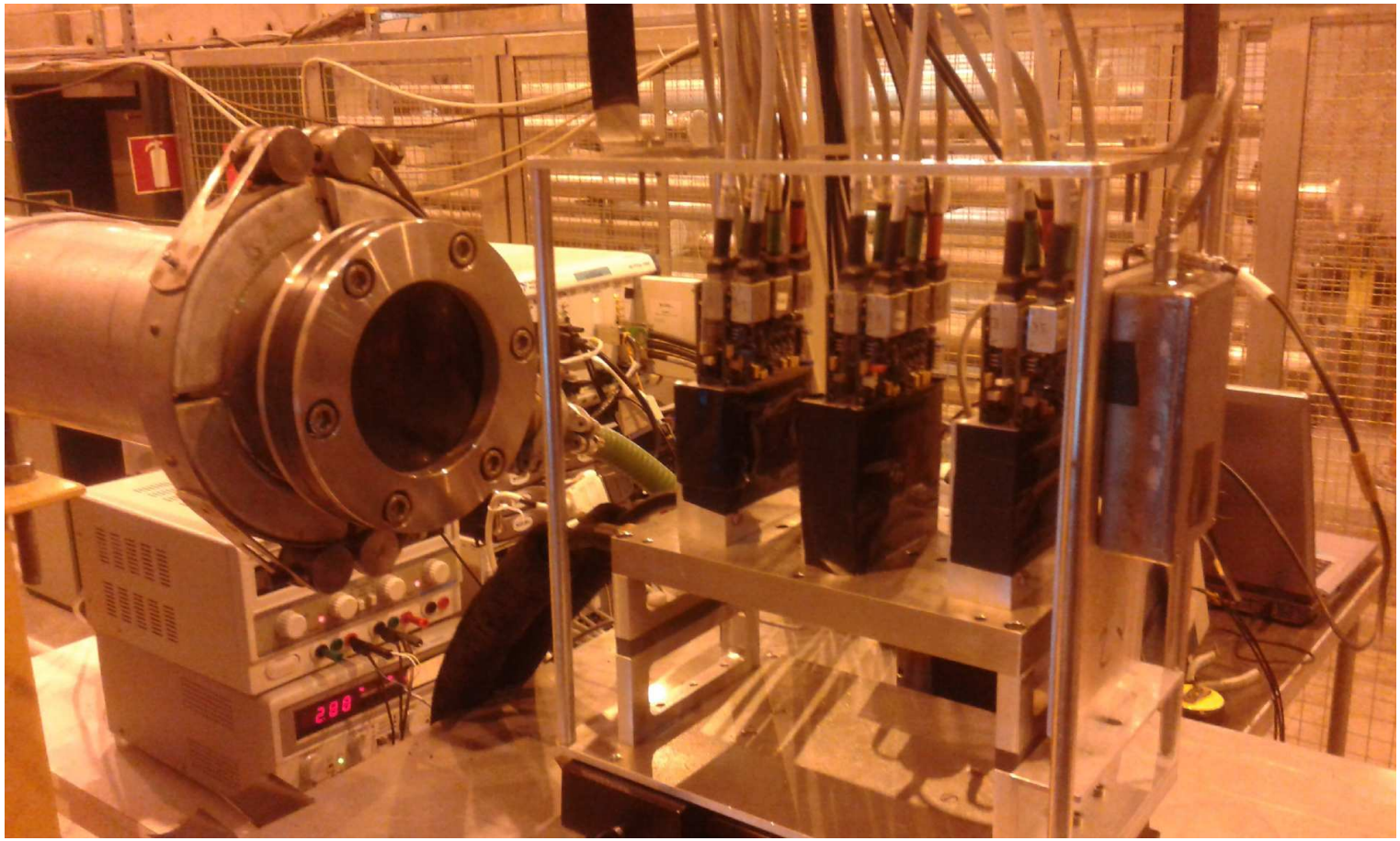


Main Objectives of MIMOSA-22THRb and FSBB-M0 Prototyping

Parametres investigated	MIMOSA-22THRb7/6	FSBB-M0bis
Sensing node geometry	X	X
Epitaxial layer parametres	x	X
In-pixel signal processing	X	x
on 3 ML (Pre-Amp, clamping)	X	–
Pads over pixels	X	–
Large pixel detection efficiency	X	–
at 30°C (incl. after OB radiation load)	X	–
Large pixel single point resolution	X	–
Complete signal sensing & processing chain	–	X
Fake rate (160,ooo pixels)	x	X
Impact of voltage drop	–	X
Cluster encoding data size	X	x

FSBB Tests at the CERN-SPS in Octobre 2015

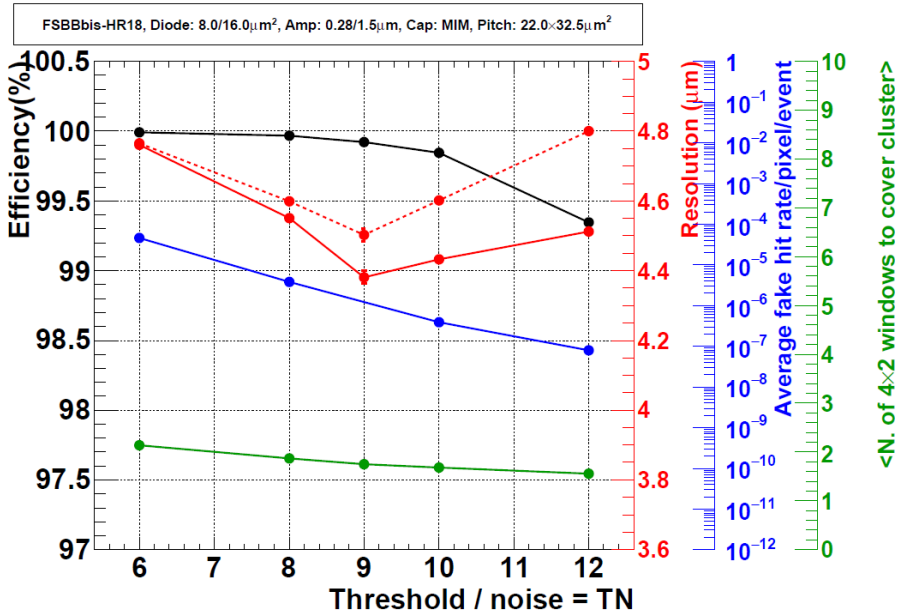
- **Beam Telescope made of 3 pairs of FSBB Planes on T4/H6 (120 GeV π^-)**



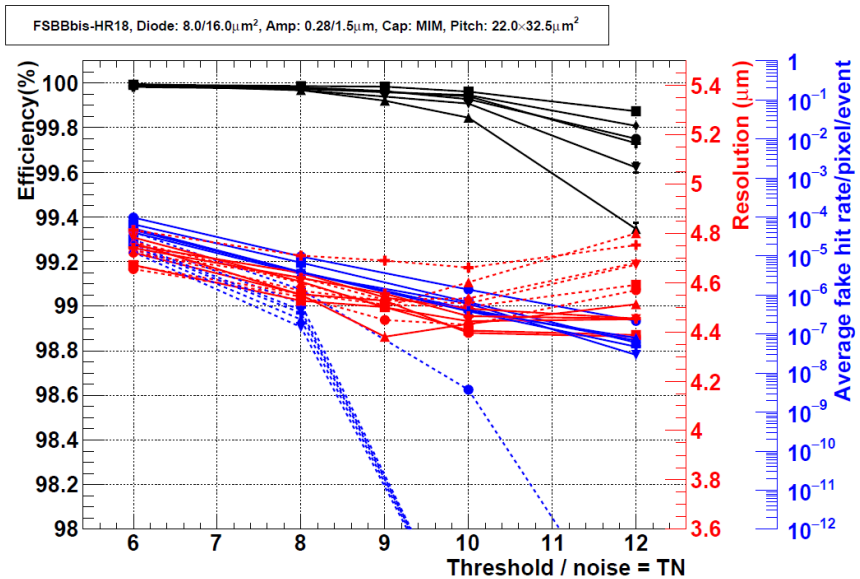
- **Measurements performed as a function of discriminator threshold :**
  - detection efficiency vs fake rate (noisy pixels)
  - spatial resolution associated to binary encoding of 22 x 32.5 μm^2 pixels
  - radiation tolerance at 30°C coolant temperature (doses $\gg$ ILC values)

Main FSBB-M0 Detection Performances (1/3)

- **Detection performances vs discri. threshold :**
  - detection efficiency wrt tracks reconstructed in BT
  - fake rate (pixel noise fluctuations above threshold)
  - single point resolution wrt impact extrapolated from BT
    (2 directions : // column or // raw)
  - average nb of encoding windows per hit
    (for the purpose of data size minimisation)

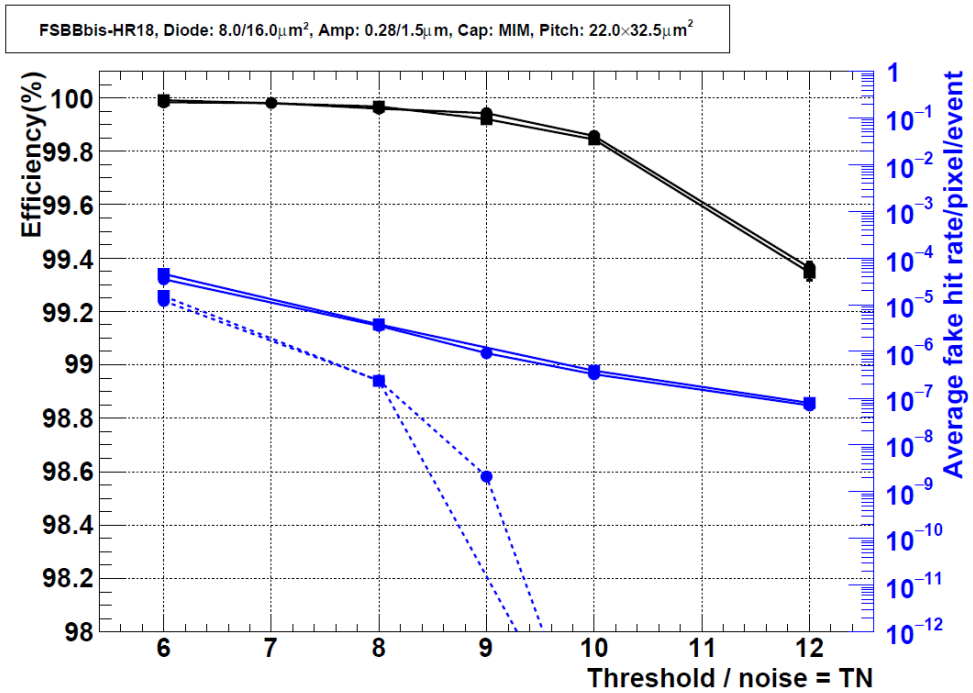


- **2 cases shown on figures :**
  - response of 1 of both DUT (top fig.)
  - response of all 6 (”identical”) sensors
    composing the BT (bottom fig.)
    ↪ indication of uniformity over large detector areas

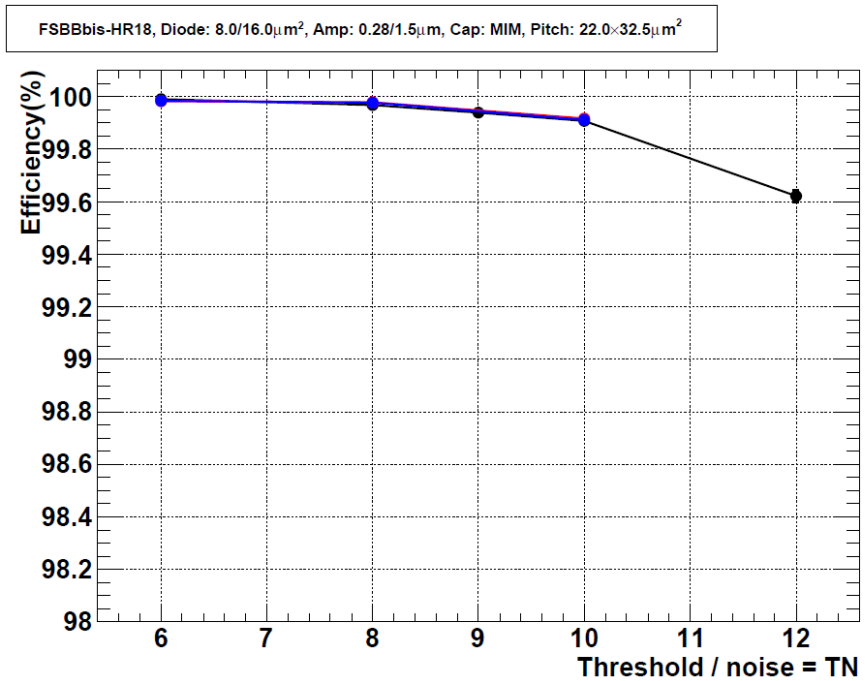


Main FSBB-M0 Detection Performances (2/3)

- **Study of detection efficiency stability :**
  - Difference between SPS (120 GeV pions) & DESY (4.5 GeV electrons)
  - Effect of occupancy : from ∼ 1 hit/frame to ∼ 25 hits/frame



SPS vs DESY

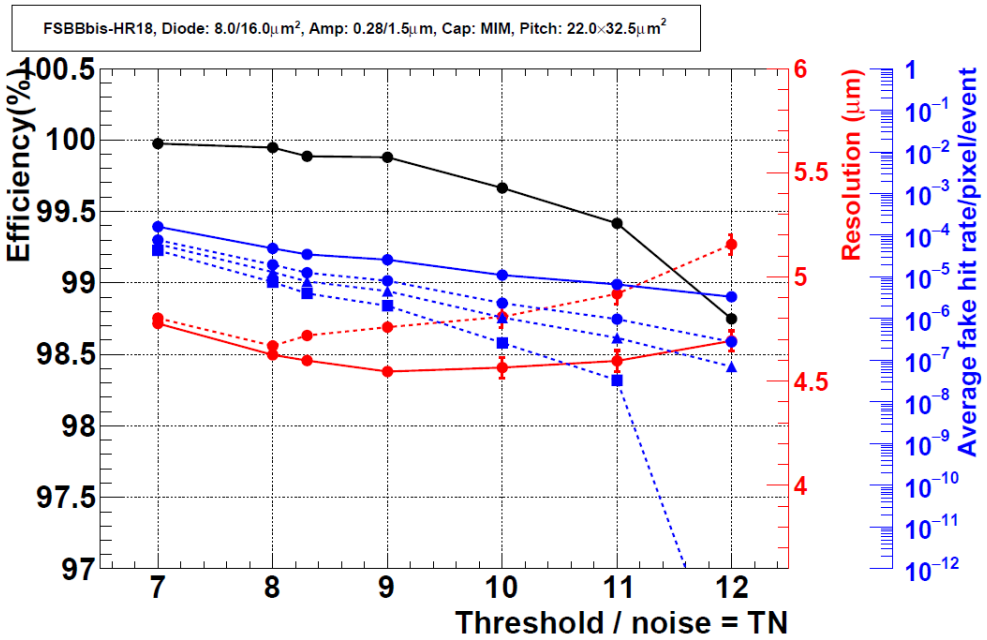


∼ 1 to 20-30 hits/frame

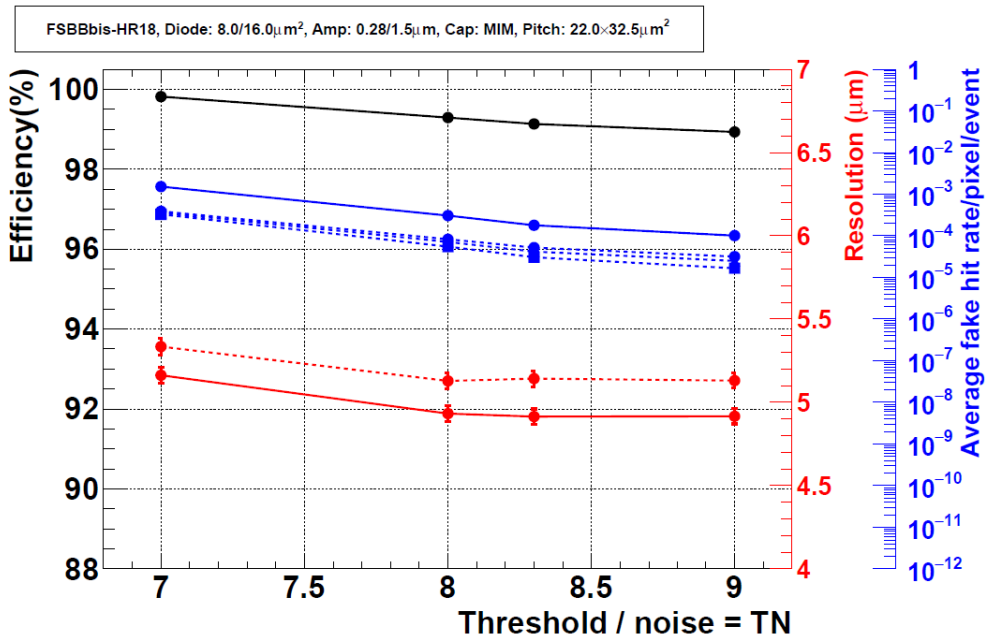
⇛ **No variation observed**

Main FSBB-M0 Detection Performances (3/3)

- **Study of radiation tolerance at T $\gtrsim$ 30°C :** loads relevant for the ALICE-ITS inner layers



$3{\cdot}10^{12}$ n_{eq}/cm^2 $\oplus$ 480 kRad

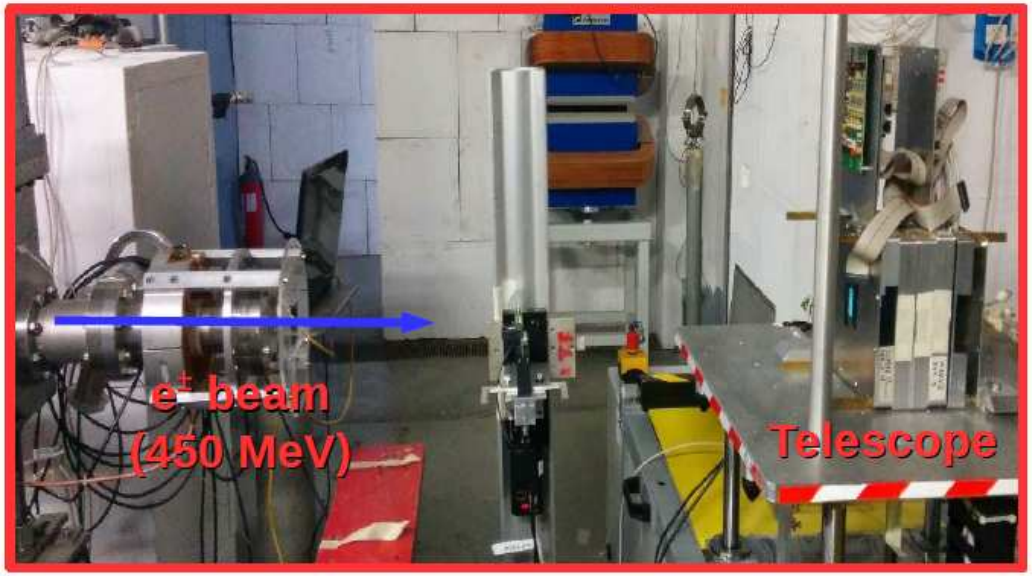


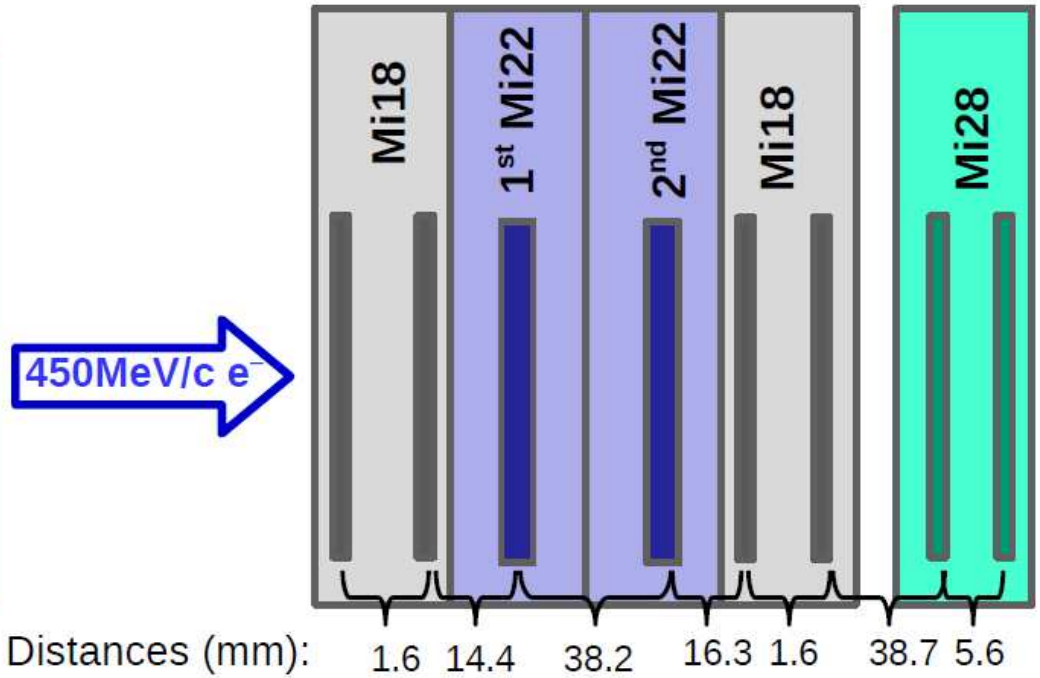
$1{\cdot}10^{13}$ n_{eq}/cm^2 $\oplus$ 1.6 MRad

$\Rrightarrow$ **Tolerance to O(100–1000) times ILC dose in L0**

MIMOSA-22 Tests at Frascati in May 2015

- **Beam Telescope made of MIMOSA-28 & -18 Planes at LNF (0.45 GeV e^-)**

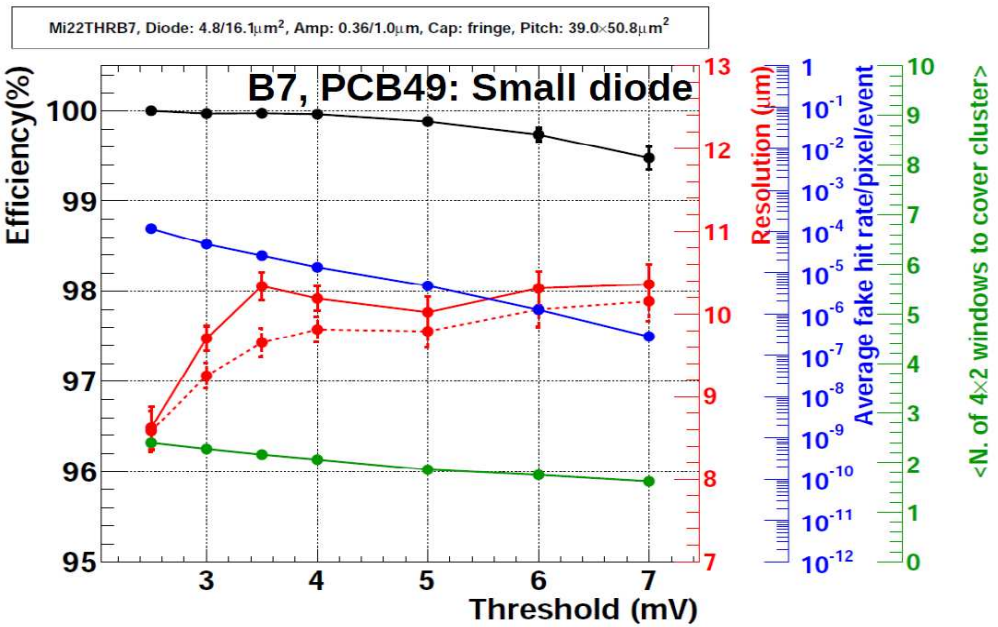


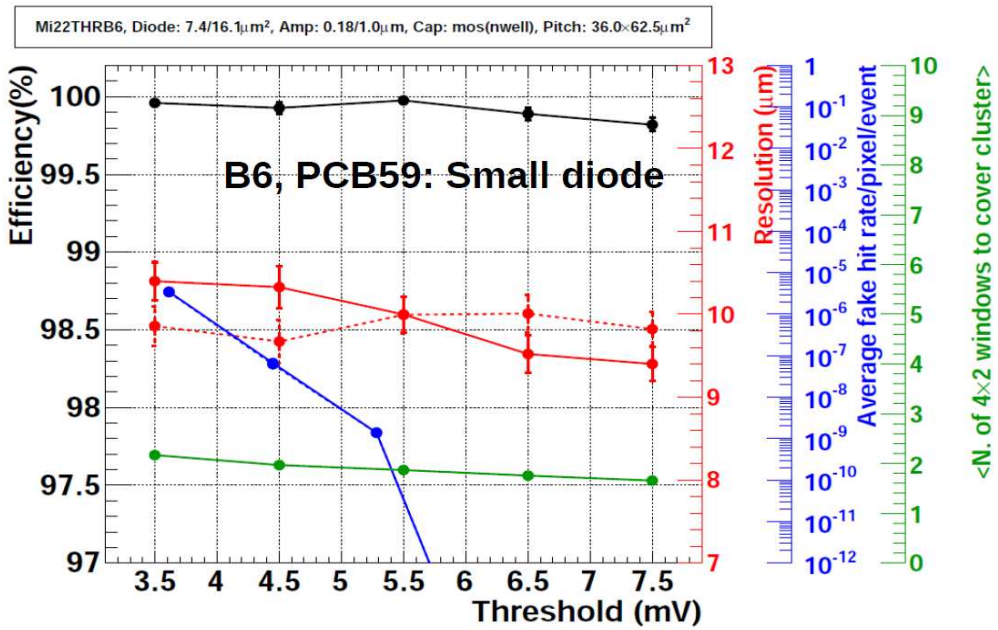


- **Measurements performed as a function of discriminator threshold :**
  - detection efficiency vs fake rate (noisy pixels)
  - spatial resolution associated to binary encoding of 36 x 62.5 μm^2 and 39 x 50.8 μm^2 pixels
  - radiation tolerance at 30°C coolant temperature (doses $\gg$ ILC values)

Main MIMOSA-22THRb Detection Performances (1/2)

Pixel type	Pixel dim.	Diode/Footprint	Pre-Amp T.	Clamping capa.	Integ. time
MIMOSA-22THRb7	39 μm x 50.8 μm	5/16 μm^2	N-MOS	MOS (N-well)	5 μs
MIMOSA-22THRb6	36 μm x 62.5 μm	7/16 μm^2	P-MOS	fringe (metal layers)	5 μs

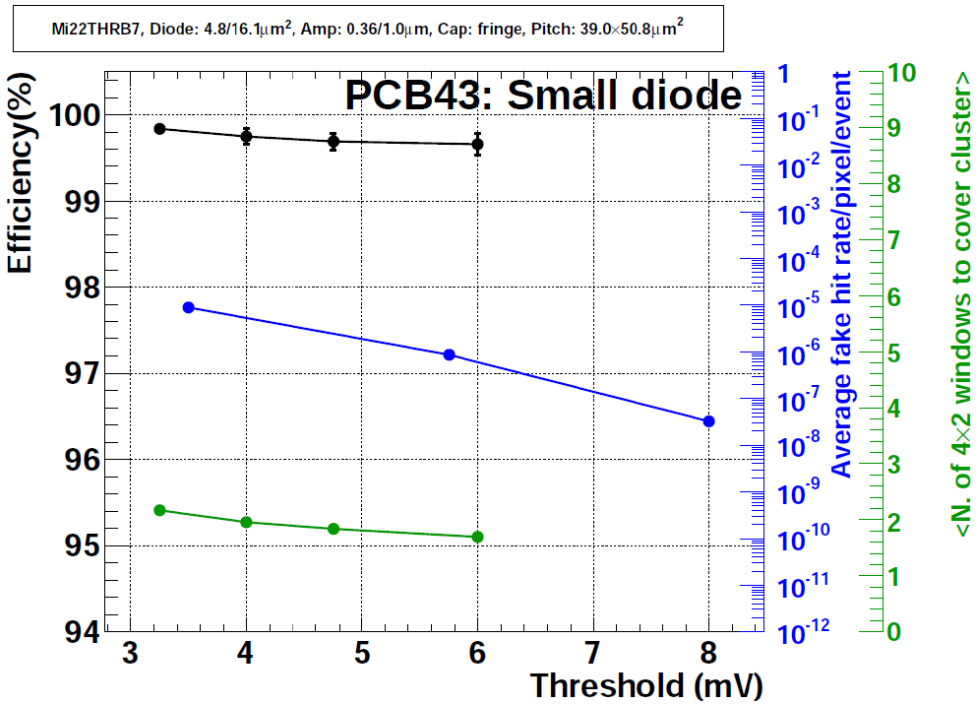




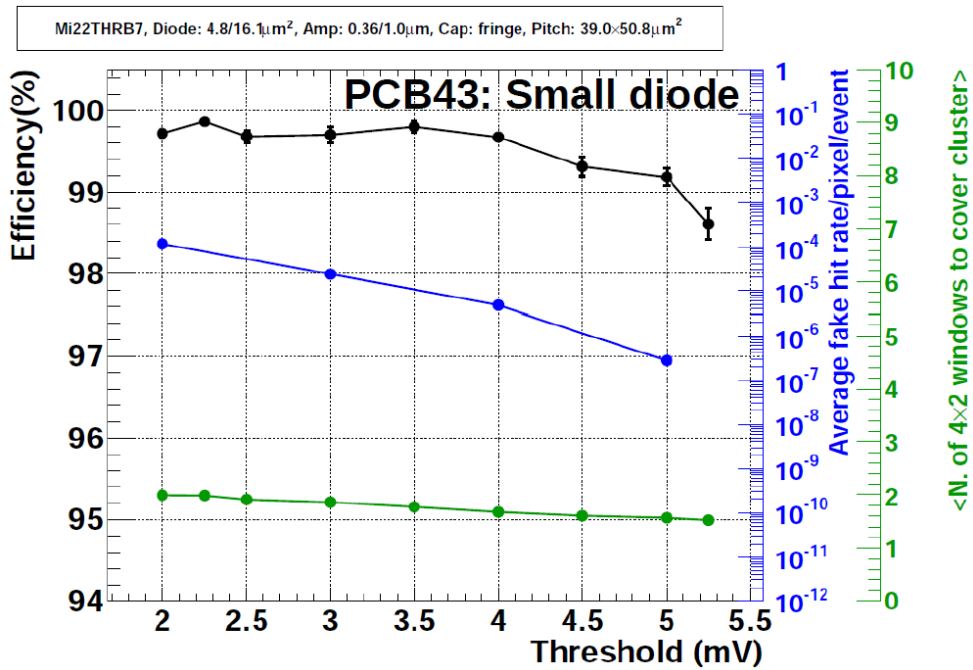
- **P-MOS vs N-MOS Pre-Amp input transistor :**
  - P-MOS: less RTS noise, higher gain and sensing node voltage
  - N-MOS: better pixel response uniformity, less temperature dependence, maturity (STAR)

Main MIMOSA-22THRb Detection Performances (2/2)

- **Study of radiation tolerance at T $\gtrsim$ 30°C :** loads relevant for the ALICE-ITS outer layers



$5{\cdot}10^{11}$ n_{eq}/cm^2 $\oplus$ 50 kRad

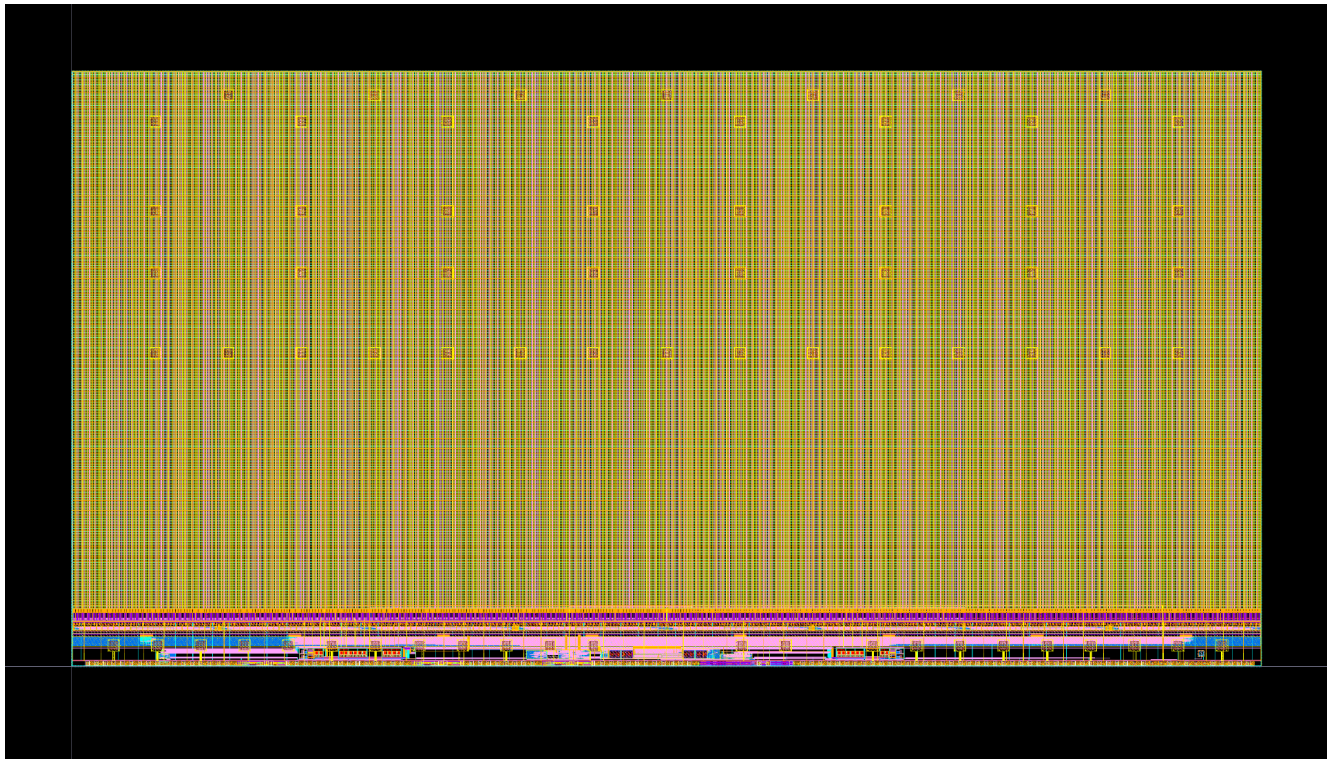


$1.5{\cdot}10^{12}$ n_{eq}/cm^2 $\oplus$ 150 kRad

$\Rrightarrow$ **Tolerance to O(100–1000) times ILC dose in main tracker**

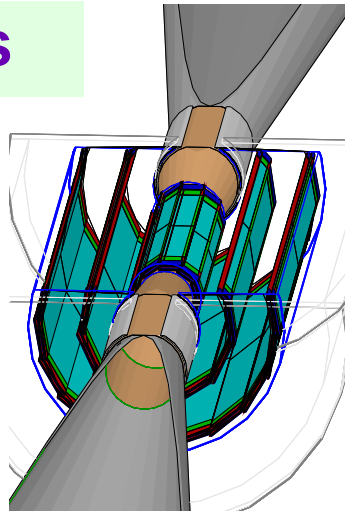
Final Sensor : MISTRAL-O

- **Combination of 4 FSBBs with MIMOSA-22THRb7 pixels**
- **Main characteristics :**
  - chip dimensions : 15 mm x 30 mm
  - Sensitive area = 13.50 mm x 29.95 mm
    - ↪ 1.5 mm wide side band (evolving towards $\sim$ 1 mm)
  - 832 columns of 208 pixels (1.6 10^5 pixels)
  - pixel dimensions : 36 μm x 65 μm
  - in-pixel pre-amp & clamping (fringe capa)
  - end-of-column signal discrimination
  - discriminators' output sparsification
  - fully programmable control circuitry
  - pads over pixel array

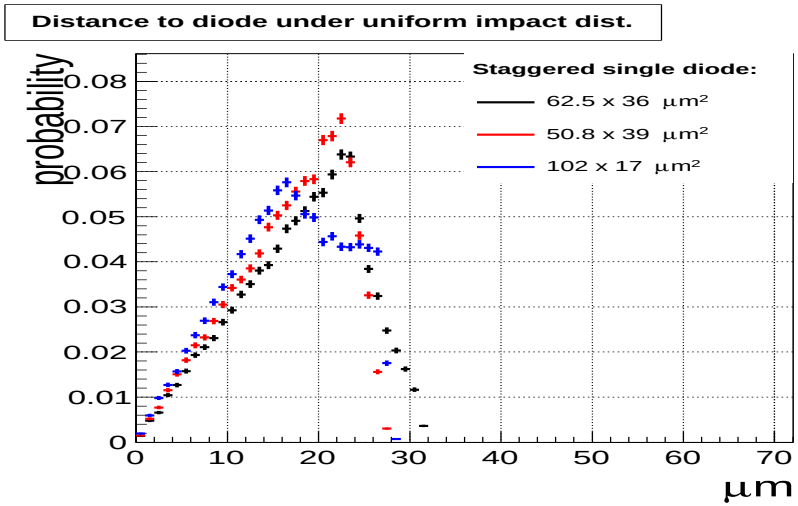


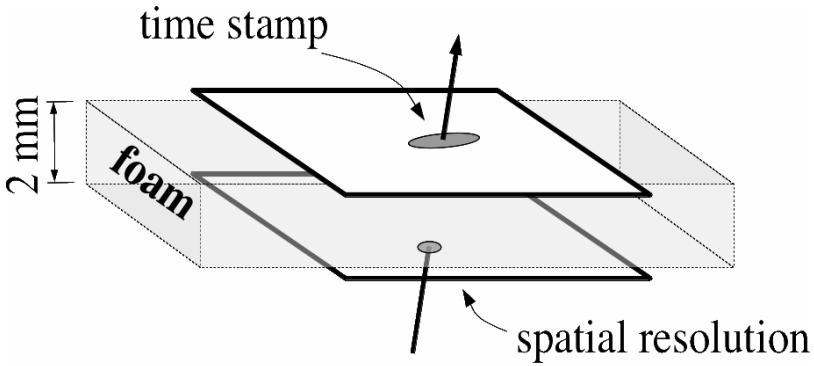
- **Typical performances :** (based on FSBB and MIMOSA-22THRb7 beam tests)
  - read-out time $\sim$ 20 μs
  - spatial resolution $\sim$ 10 μm
  - power density $\lesssim$ 90 mW/cm^2
  - radiation tolerance $>$ 1.5·10^{12} n_{eq}/cm^2 and 150 kRad at T $>$ 30°C

Extrapolation to an ILC Vertex Detectors



- VERTEX DETECTOR CONCEPT :
  - Cylindrical geometry based on 3 concentric 2-sided layers
  - Layers equipped with 3-4 different CMOS Pixel Sensors (CPS)



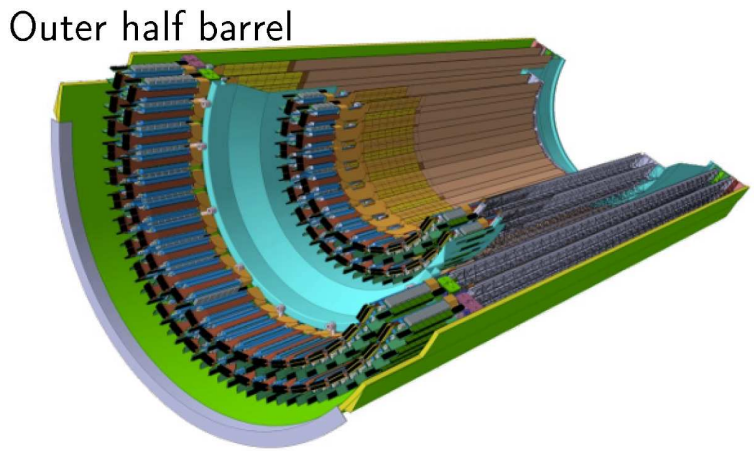


- CPS FOR DOUBLE-SIDED VXD LADDERS ACHIEVABLE WITH PRESENT KNOWLEDGE :
  - L0 pixels: 17x17 $\mu m^2 \Rrightarrow$ $<$ 3 μm & 64–32 μs
  - L1 pixels: 17x102 $\mu m^2 \Rrightarrow$ $\lesssim$ 5 μm & 5–2/1 μs
  - L3–L6 pixels: 25x51 $\mu m^2 \Rrightarrow$ $\sim$ 3.5 μm & 40 μs combined with 27x29 $\mu m^2 \Rrightarrow$ $\lesssim$ 5 μm & 4 μs
- NEXT STEPS OF THE R&D :
  - realise & operate double-sided ladders with 2 different CPS and check power cycling
  - continue exploiting CPS potential :

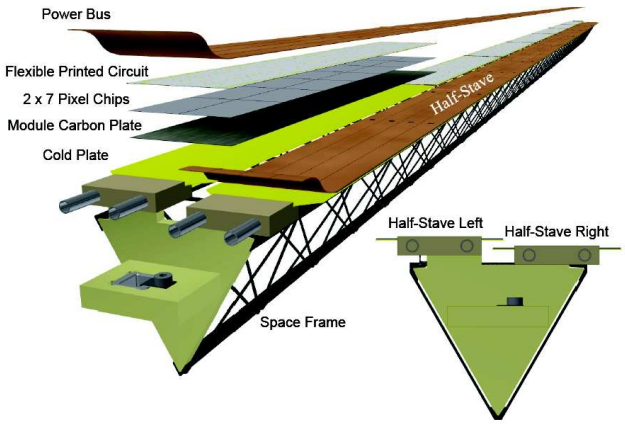
    $\Rrightarrow$ squeeze read-out time & power while keeping high spatial resolution (e.g. $<$ 3 μm)

Extrapolation to ILC Trackers

- ALICE-ITS CONCEPT :
  - Cylindrical geometry based on 7 concentric single-sided layers
  - Outer Barrel (4 layers; 10 m^2) serves as a tracker
  - All layers equipped with CMOS Pixel Sensors (CPS)
  - Baseline sensor (ALPIDE) : 5 μm & 4 μs
    (not yet validated on detector ladder)
  - Outer Barrel material budget $\lesssim$ 1% X_0/layer
  - Stave length up to $\sim$ 1.5 m



- CPS FOR DOUBLE-SIDED TRACKER LAYERS ACHIEVABLE WITH PRESENT KNOWLEDGE :
  - transposing the ITS concept to an ILC exp.
    allows for 5 μm resolution
    and 4 μs read-out time
  - alternative : use ITS sensor (5 μm & 4 μs)
    on one ladder side and a faster
    (time stamping) version based on
    elongated pixels on the other side :
    $\sim$ 1 μs seems achievable (tbc)



SUMMARY & OUTLOOK

- **Validation of CPS for high resolution vertex detectors carries on through STAR-PXL data taking campaigns :** results of 2 years of physics runs confirm high resolution DCA

- **Development of CPS for a tracker (ALICE-ITS upgrade) finalised**
  $\hookrightarrow$ uses powerful CMOS process & well suited epitaxial layers ($\gtrsim$ 20 μm thick; $\sim$ 1–8 kΩ·cm)

- **Large pixels developed for trackers are proven to have good detection efficiency**
  $\hookrightarrow$ they may be suited to pixelated trackers at ILC

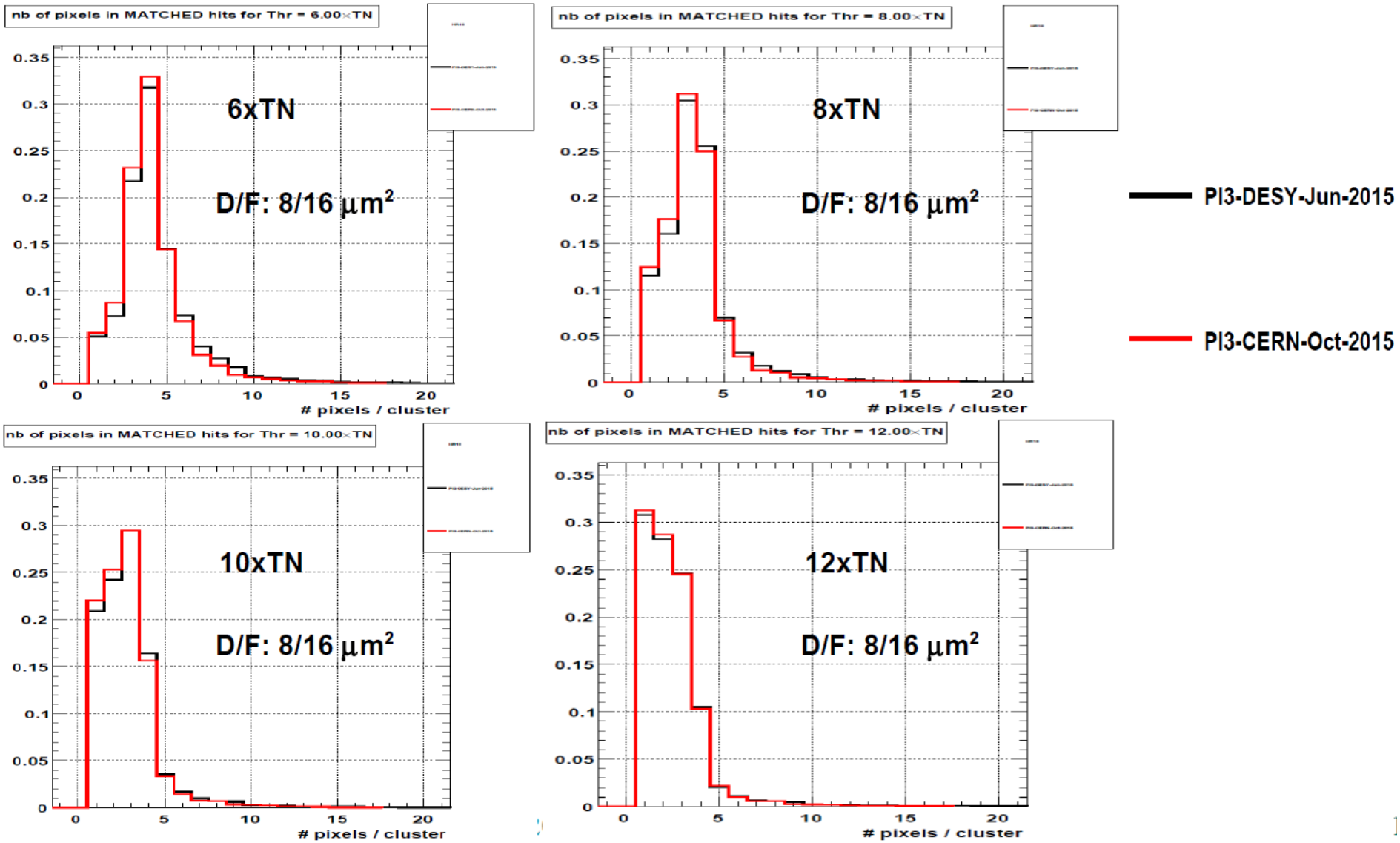
- **CMOS process used for ALICE-ITS upgrade allows deriving fast r.o. ($\sim$ 1 μs) concept**
  for inner layer of an ILC vertex detector $\longmapsto$ **Goal :** few-bunch (1-2) tagging while keeping $\sigma_{sp} \sim$ 3 μm

- **Next steps :**
  - start deriving CPS for VXD in 2016/17 via CBM-MVD
  - realise a double-sided ladder prototype based on 2 different sensors (1 precise, 1 fast) to investigate the time-stamping concept

Layer	σ_{sp}	t_{int}
ILD-VXD/In	$<$ 3/4 μm	30-40/1 μs
ILD-VXD/Out	$\sim$ 3.5/4 μm	80/120 μs

FSBB Cluster Multiplicity

Comparing DESY vs CERN results for one of the planes (Plane 3)



Comments on ILD Vertex Detector Requirements

- **Expected N(hits)/cm^2/BX at 500 GeV & 1 TeV with anti-DID, for each ILD-VXD layer (DBD) :**

Layer	1	2	3	4	5	6
0.5 TeV	6.3$\pm$1.8	4.0$\pm$1.2	0.25$\pm$0.11	0.21$\pm$0.09	0.05$\pm$0.03	0.04$\pm$0.03
1 TeV	11.8$\pm$1.0	7.5$\pm$0.7	0.43$\pm$0.13	0.36$\pm$0.11	0.09$\pm$0.04	0.08$\pm$0.04

- **Occupancy in L1 and L2 :**
  - L1 : 17 μm $\times$17 μm pixels (cluster mult. $\simeq$ 5)
    Pixel occ. at 500 GeV $\simeq 10^{-4}$/BX $\Rrightarrow$ 10^{-2}/50 μs
  - L2 : 17 μm $\times$102 μm pixels (cluster mult. $\simeq$ 3)
    Pixel occ. at 500 GeV $\simeq 2\times10^{-4}$/BX $\Rrightarrow$ 10^{-3}/2.5 μs
  - 1 TeV : twice higher occupancy
  - Luminosity upgrade : 4 times higher occupancy
  - Large uncertainties (MC stat., anti-DID uncertainty, etc.)

$\Rrightarrow$ **Safety margins required on param. governing occupancy**