VERTEXING

AND

TRACKING

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SiD Collaboration Meeting

LCWS15

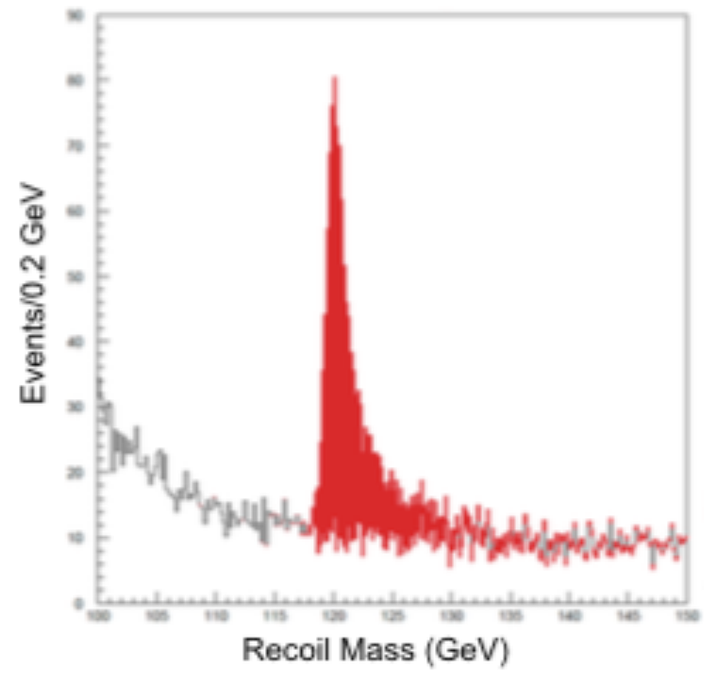
Outline

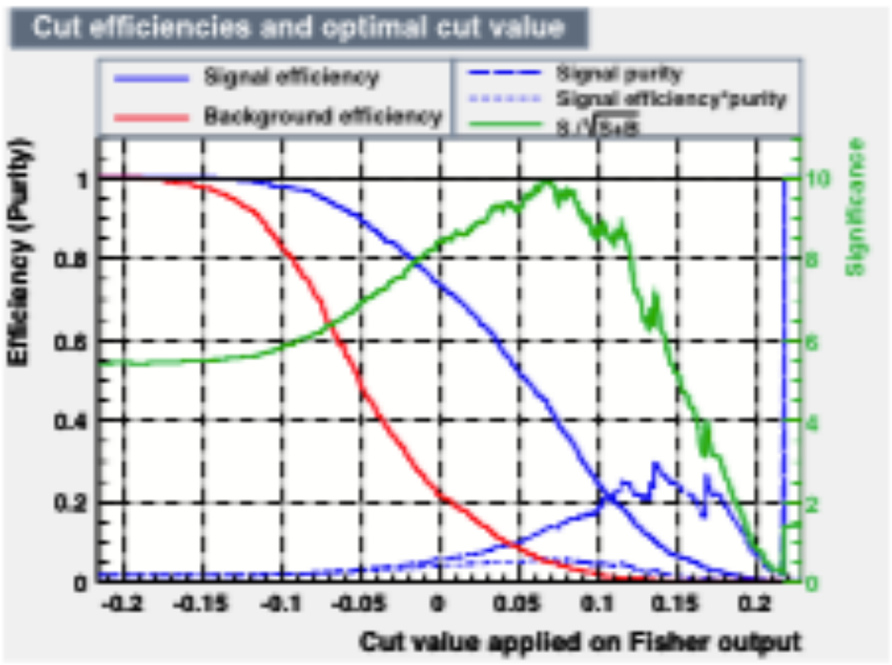
1. Overview of SiD vertexing and tracking
2. Status of vertexing R&D
3. Status of tracking R&D
   - *Progress within SiD community*
   - *Relevant developments elsewhere*
4. Summary

Physics Drivers

- Higgs recoil from Z->μμ
  - $\Delta p/p^2 \leq 5 \times 10^{-5}/\mathrm{GeV}$
- Flavour tagging
  - Impact parameter resolution

$$5 \oplus 10/p \sin^{3/2}\theta \ \mu\mathrm{m}$$

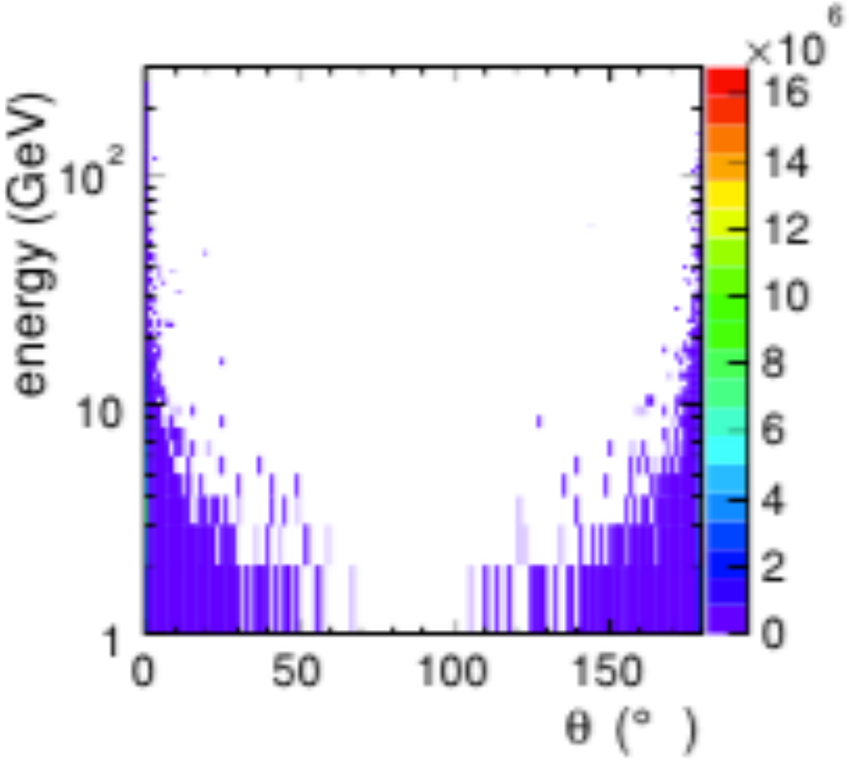




- Low material in inner detector
- Minimal services
  - **Low power**

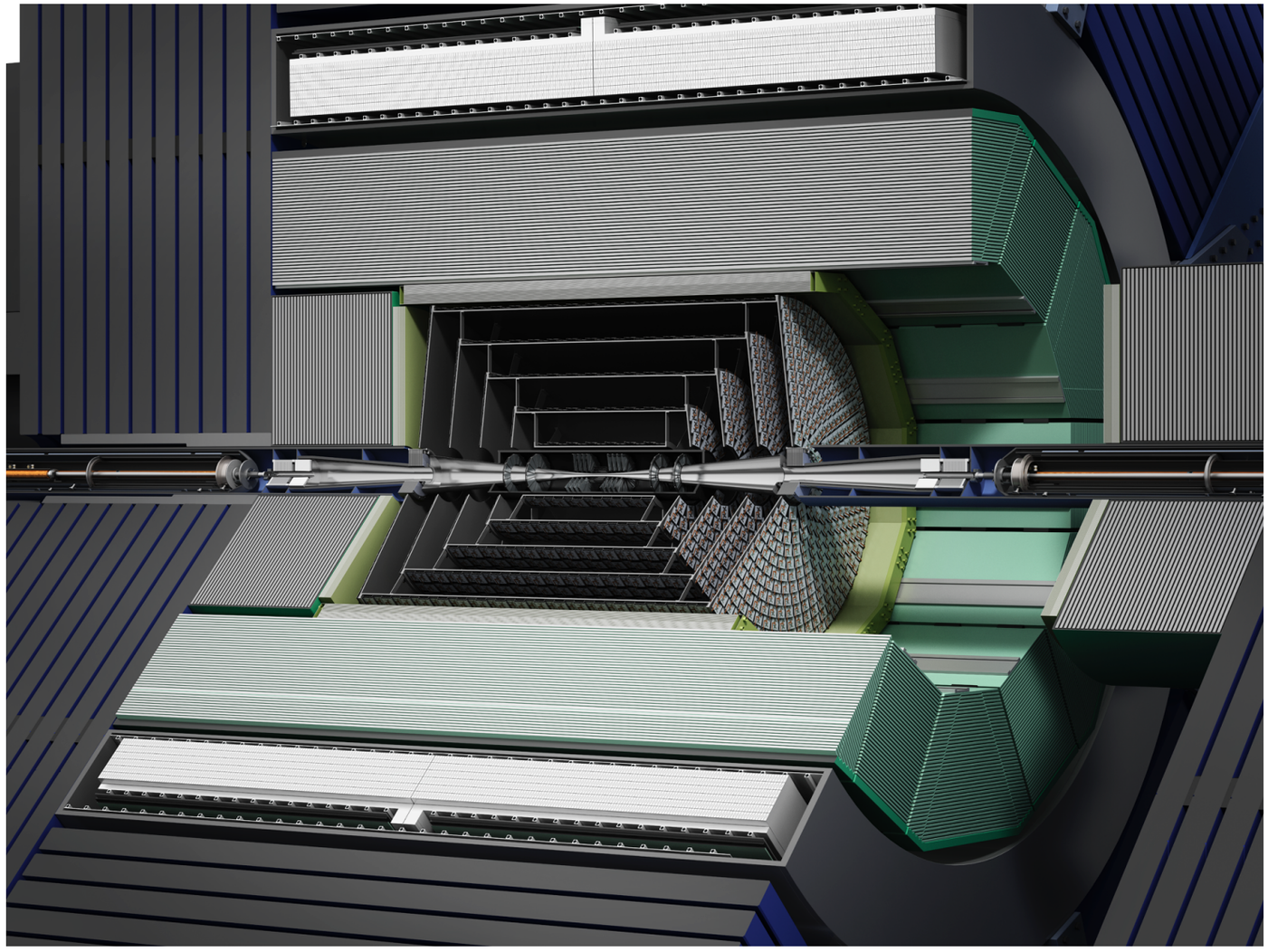
Constraints

- Beam structure:
  - 1312 bunches
  - 554 ns spacing
  - 5 Hz repetition



- Backgrounds
  - Beamstrahlung
    - Low-p_T e^+e^- pairs
      - ~10^5 pairs per bunch
  - $\gamma\gamma$ collisions
    - ~1 hadronic events per bunch
    - **Speed/timing, granularity**
  - **Tension with low power**

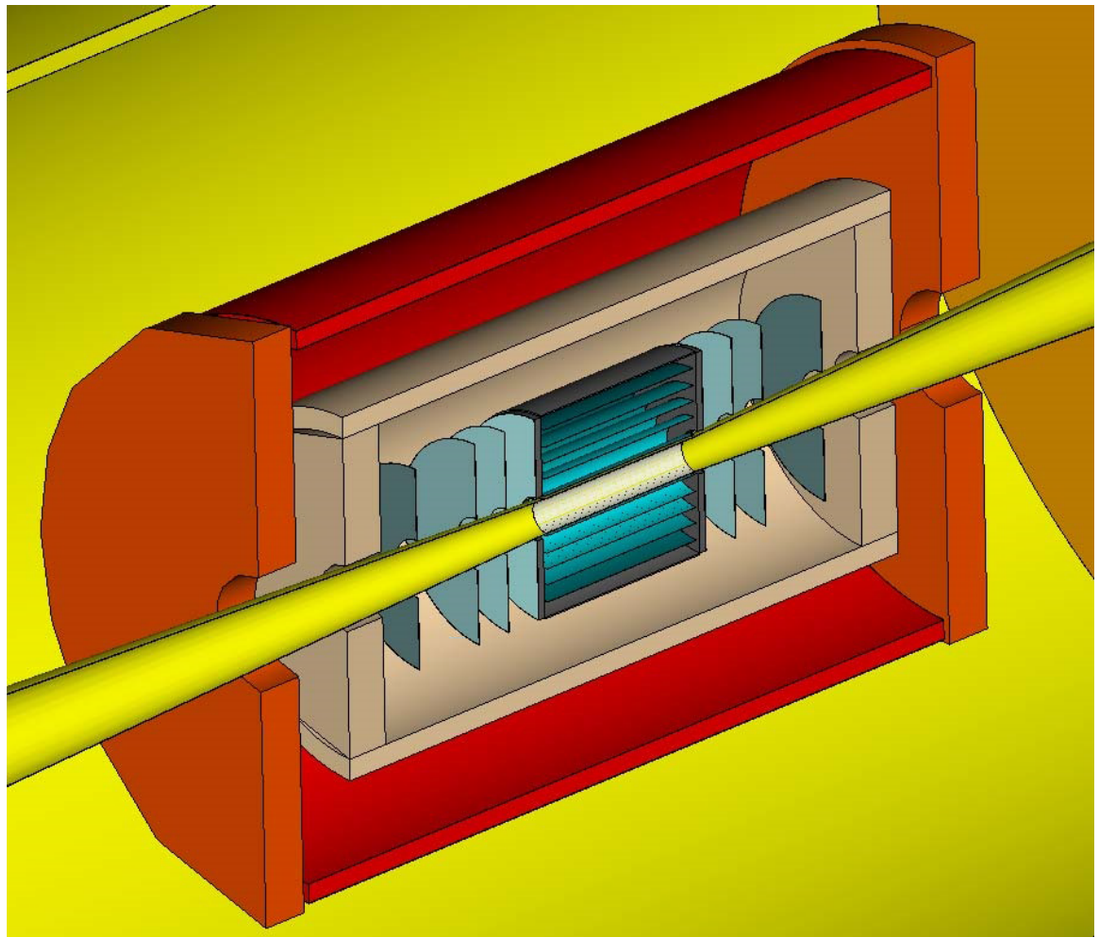
Baseline



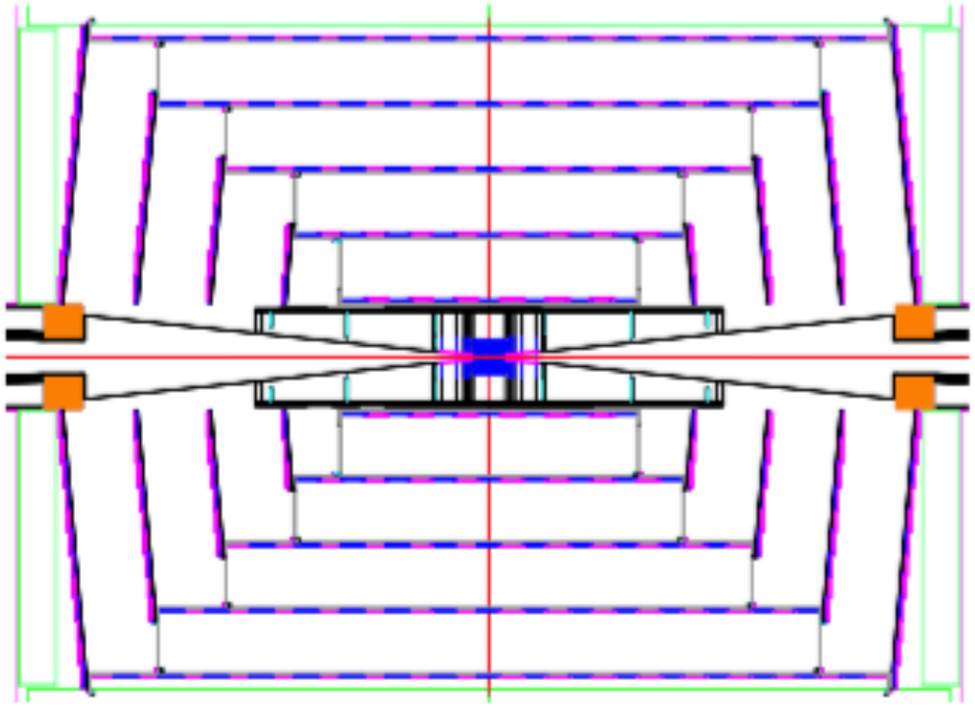
* Low mass
  * 10-20% X_0
  * Gas cooled
* Bunch-X timing

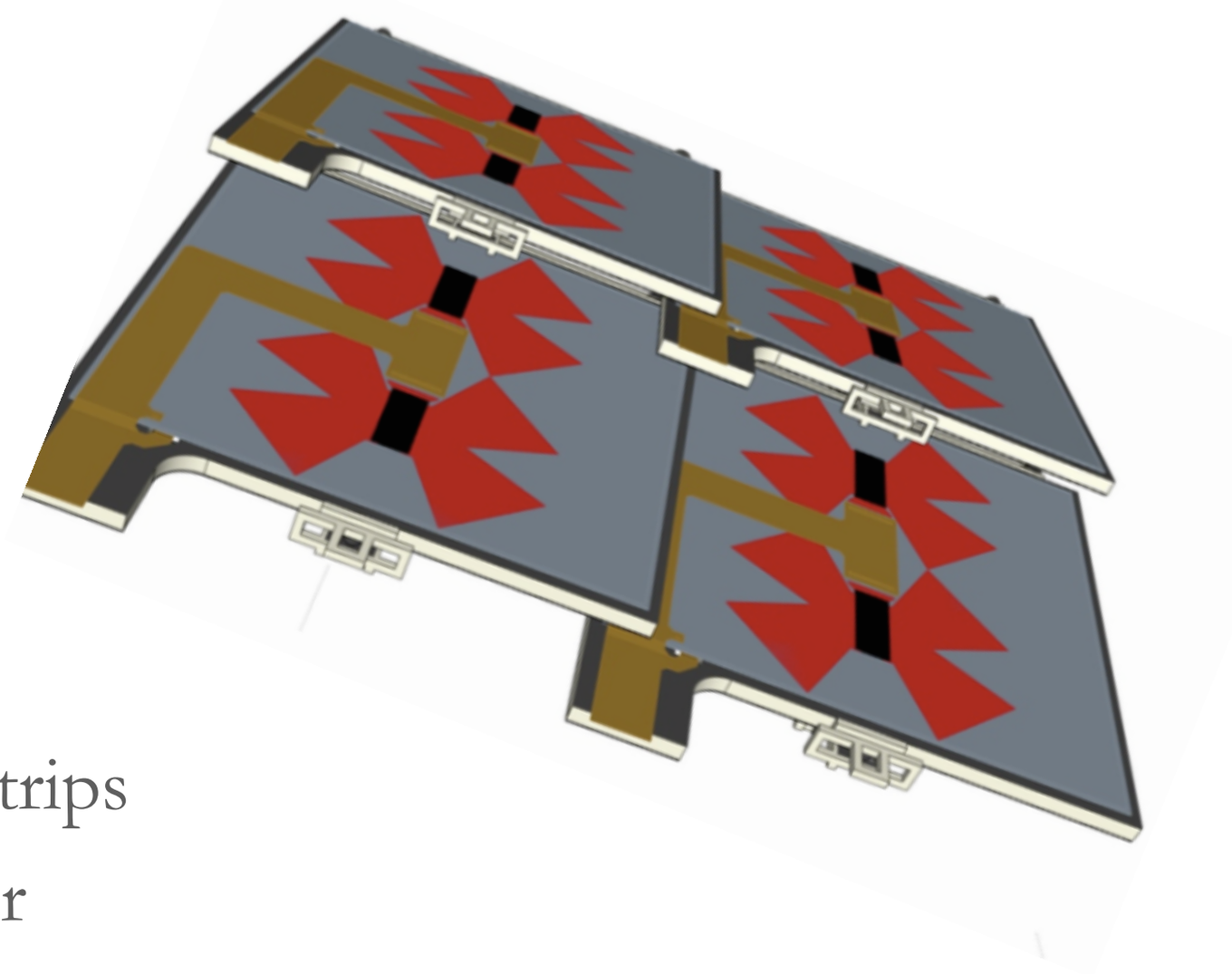
Vertex Detector

- "Short" barrel
  - 5 layers
  - 15 cm long
- Endcaps
  - 4 disks each
- 20μm×20μm pixels
- Single-bunch timing
  - **Various technologies under consideration**



Tracker





- 5 layers of silicon strips
  - ~1% X_0 per layer
  - 50μm readout pitch with intermediate strips
  - KPix frontend ASIC

Vertex Sensors

- Many pixel R&D programmes active at some level
- 3μm resolution with fast timing
- Pulse power to reduce heat load

CCD
Fine Pitch (ILD)

DepFET
(ILD)

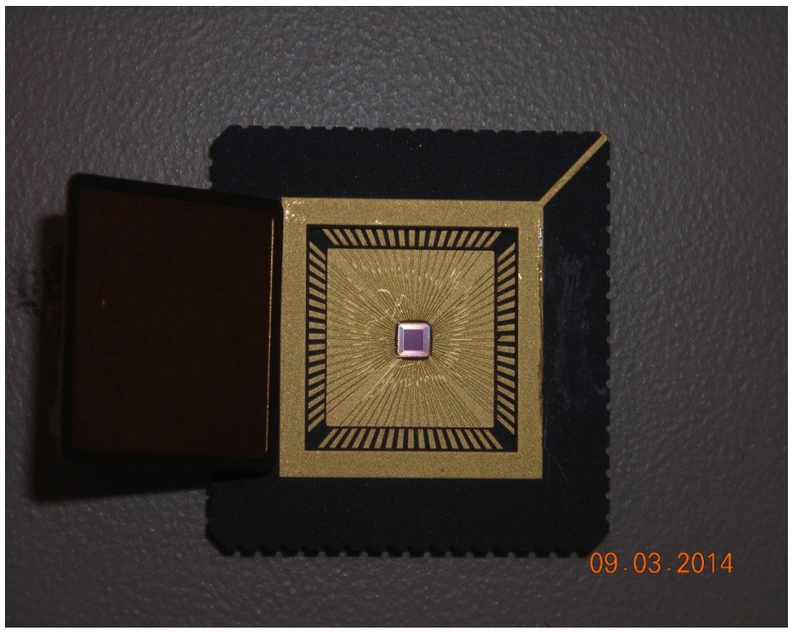
CMOS

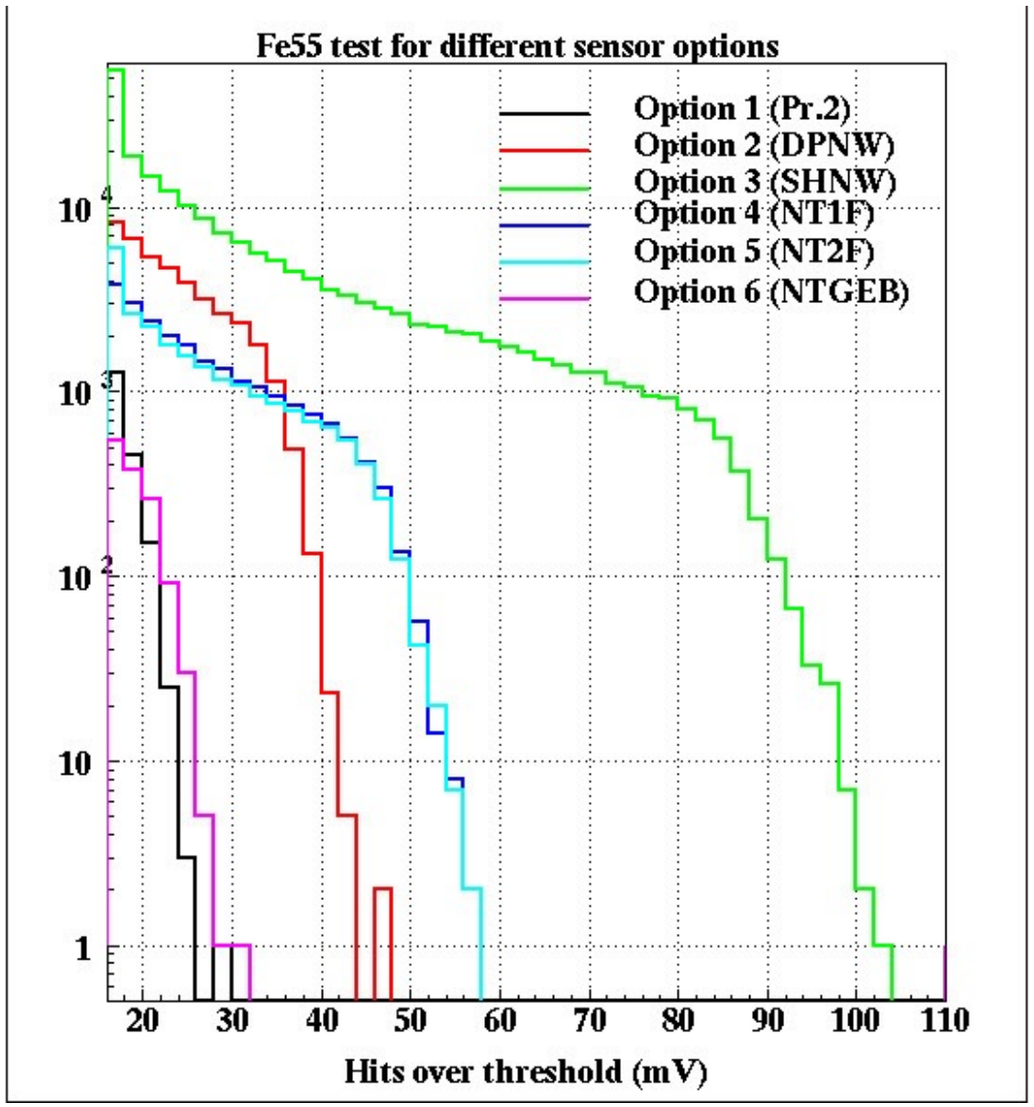
Hybrid ⟷ Monolithic

CLICpix (CLIC) | 3D | Chronopix | MIMOSA

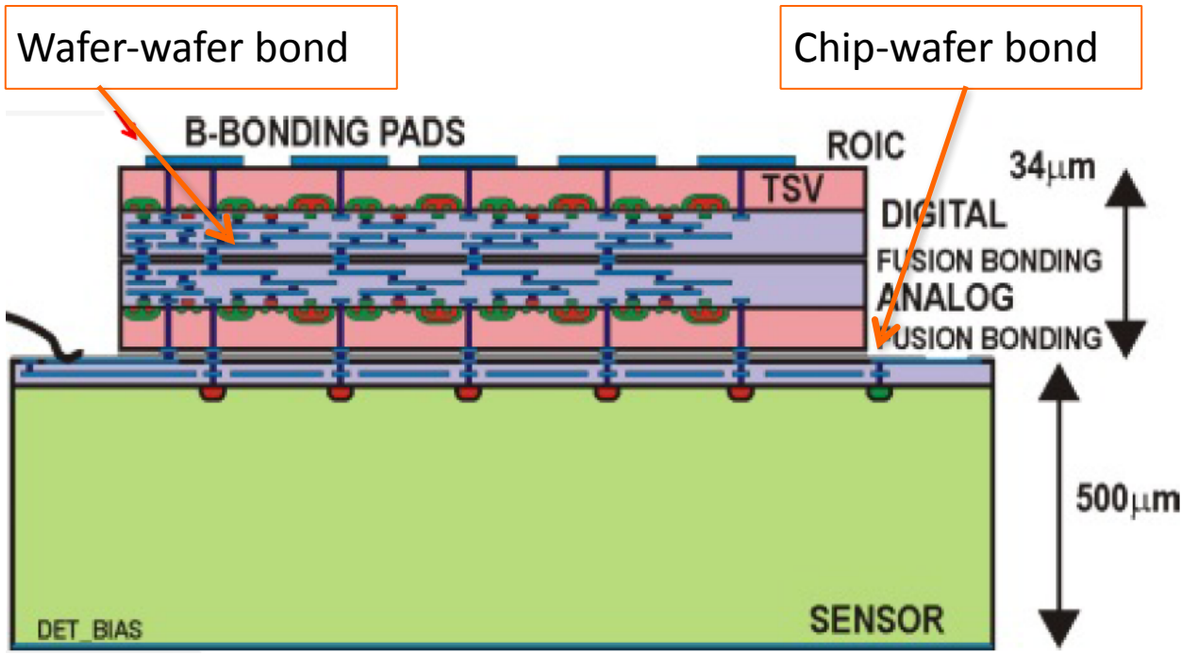
Chronopix

- 3rd generation prototype
  - 25μm×25μm pixels in 90nm CMOS
  - Bunch-by-bunch time-stamping
  - Noise and cross-talk controlled

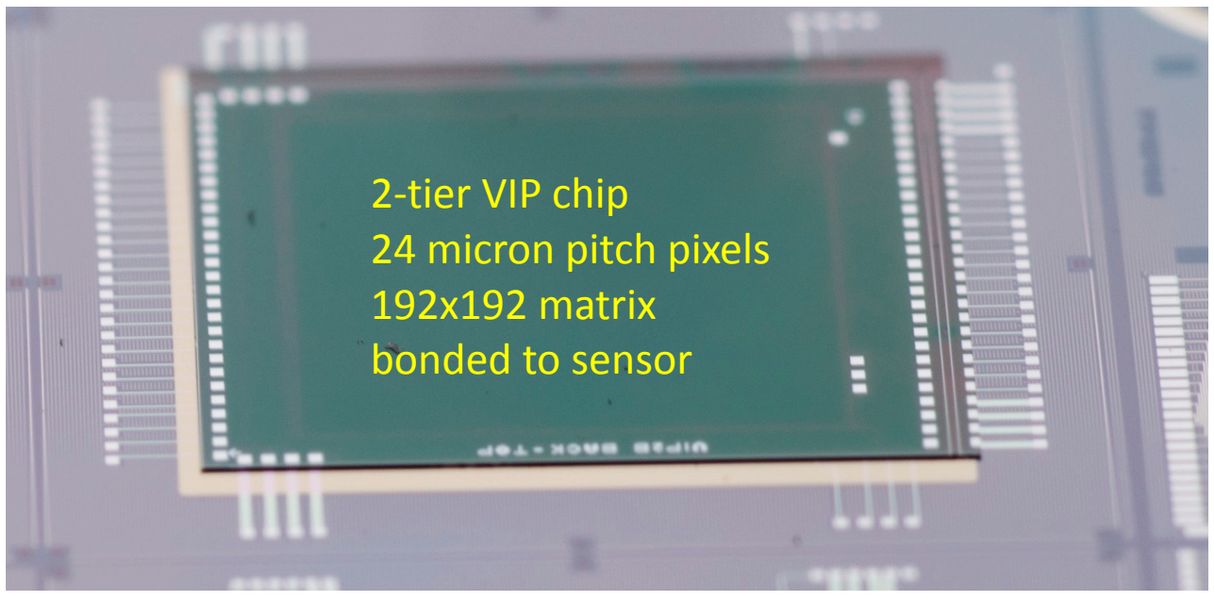


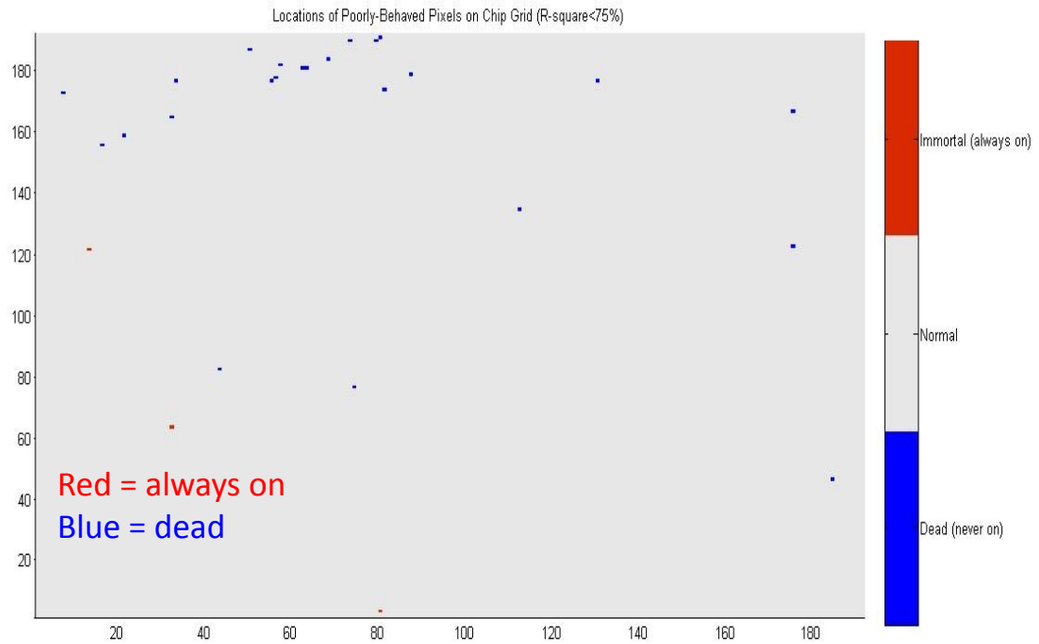


3D Project



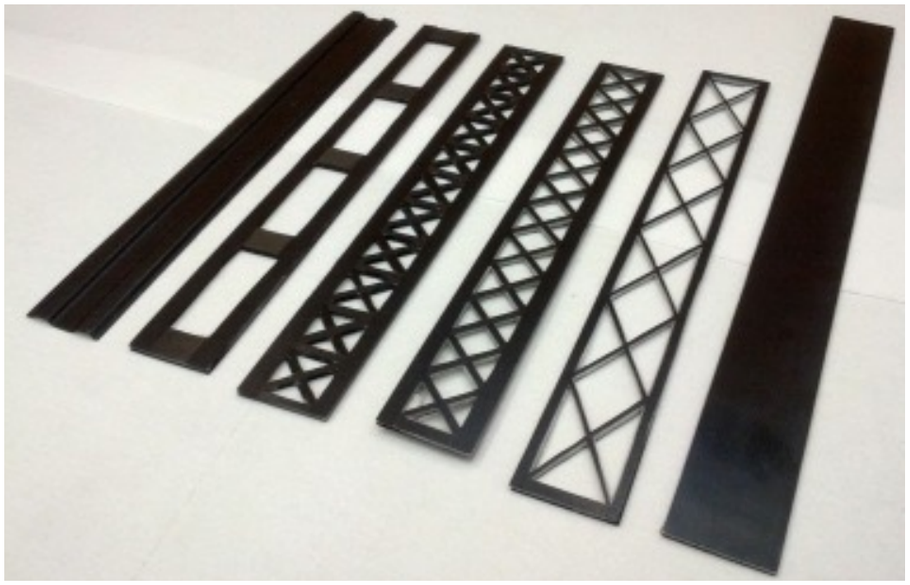
* Vertical integration using TSVs
* Three layers bonded
* Production could be commercialised



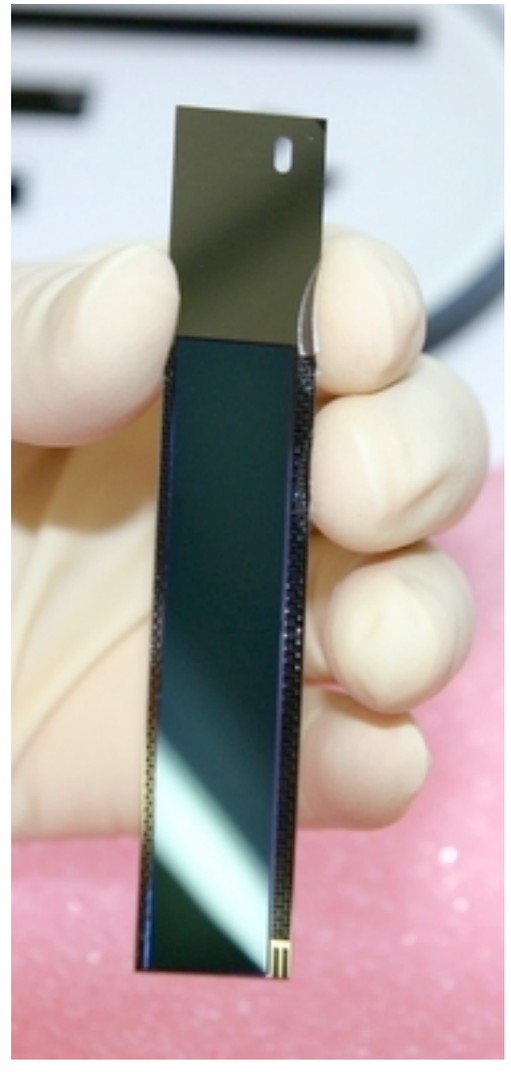


Mechanics

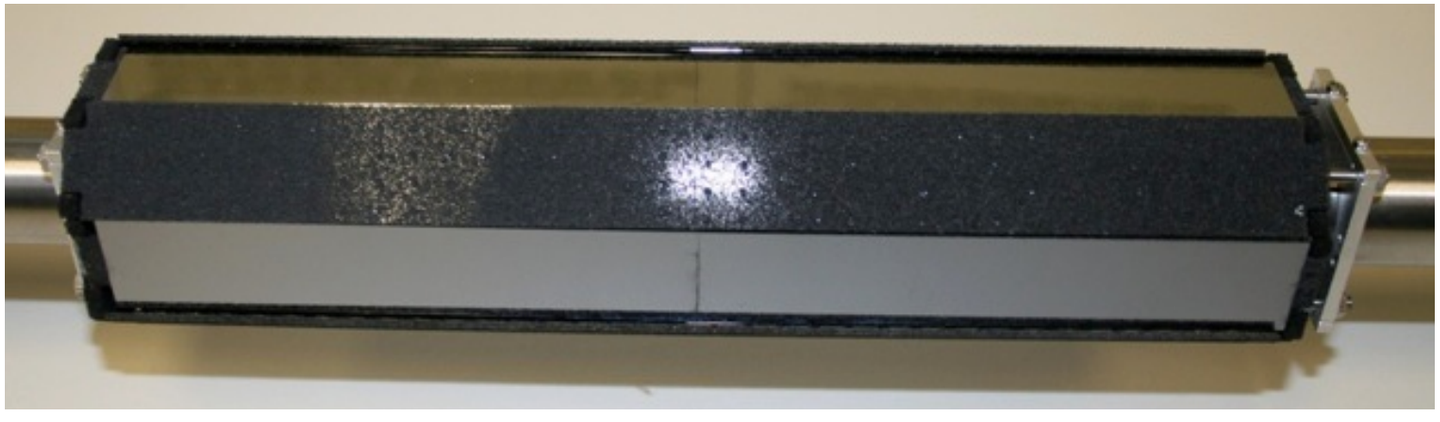
* Aiming for 0.1-0.3% X_0 per layer



Advanced Carbon Fibre (CLIC)



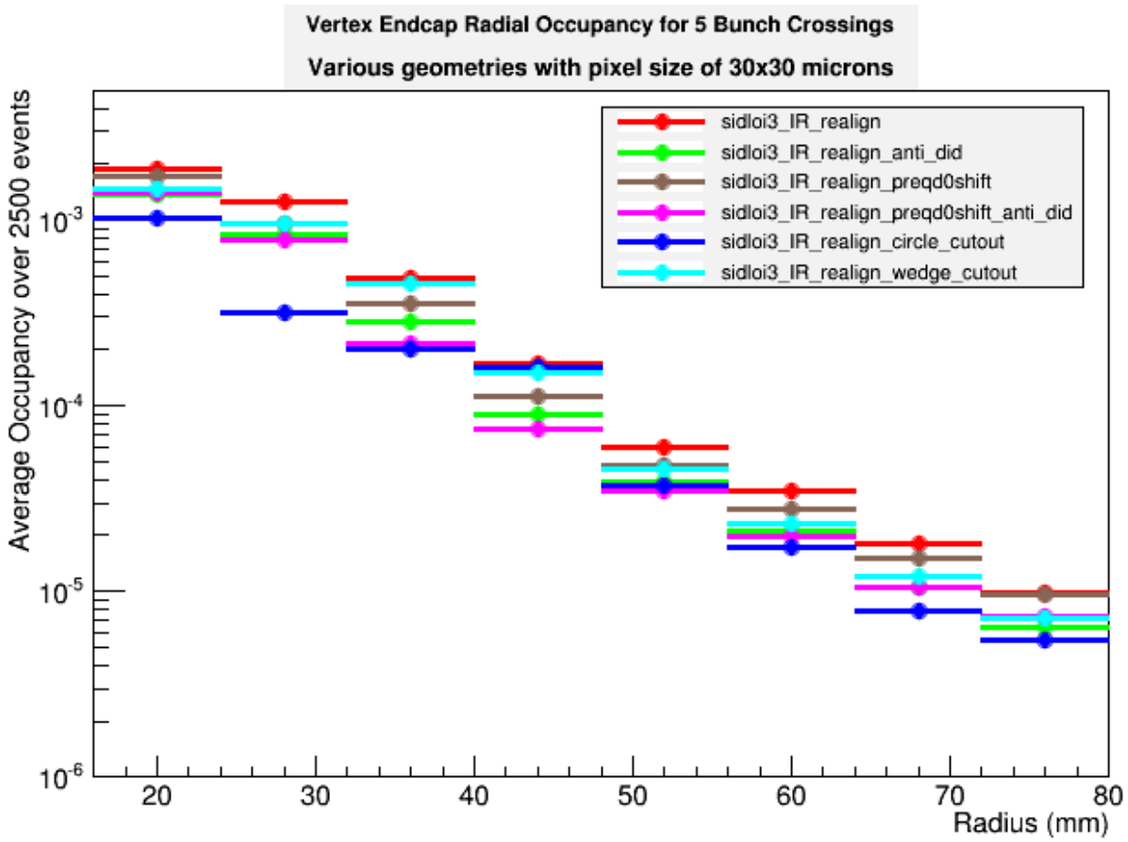
Silicon Only (DepFET/SiD)

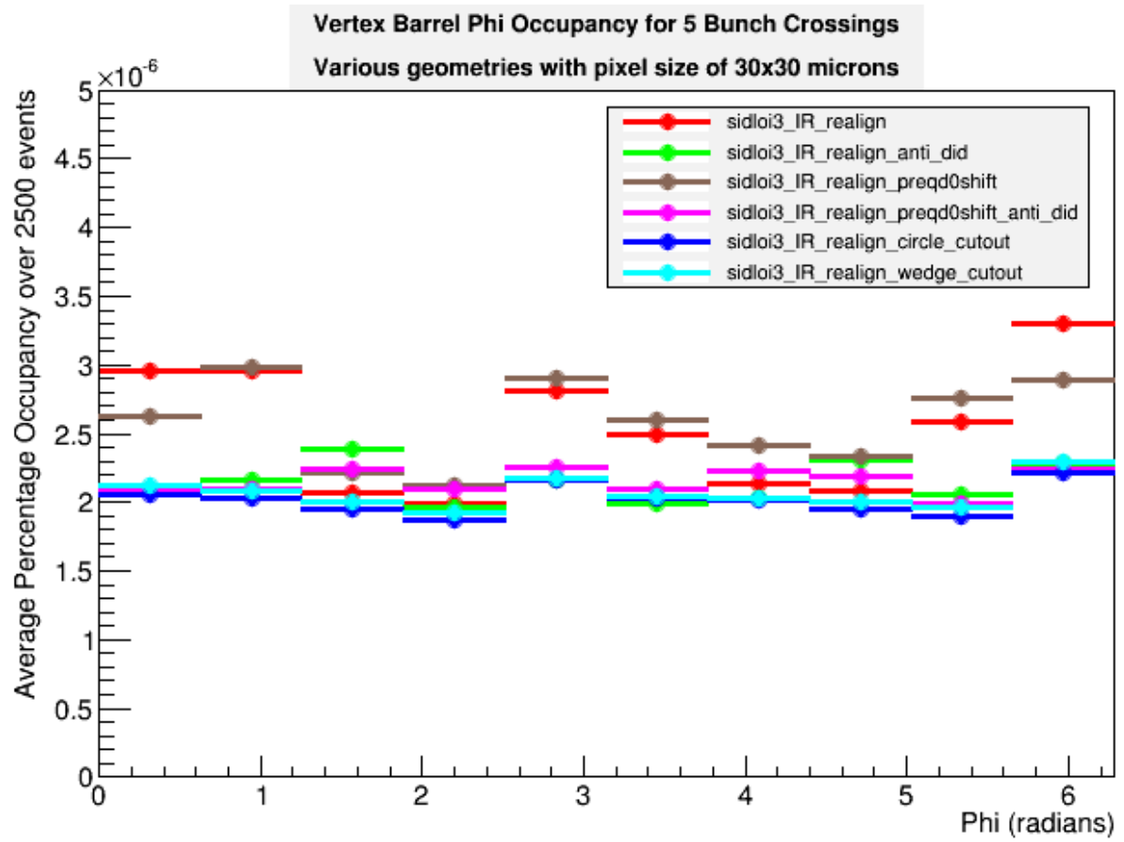


Ceramic Foam (LowMass/PLUME)

Occupancy

- Ongoing studies
  - Looking at effect of configuration changes
  - See talks tomorrow and Friday



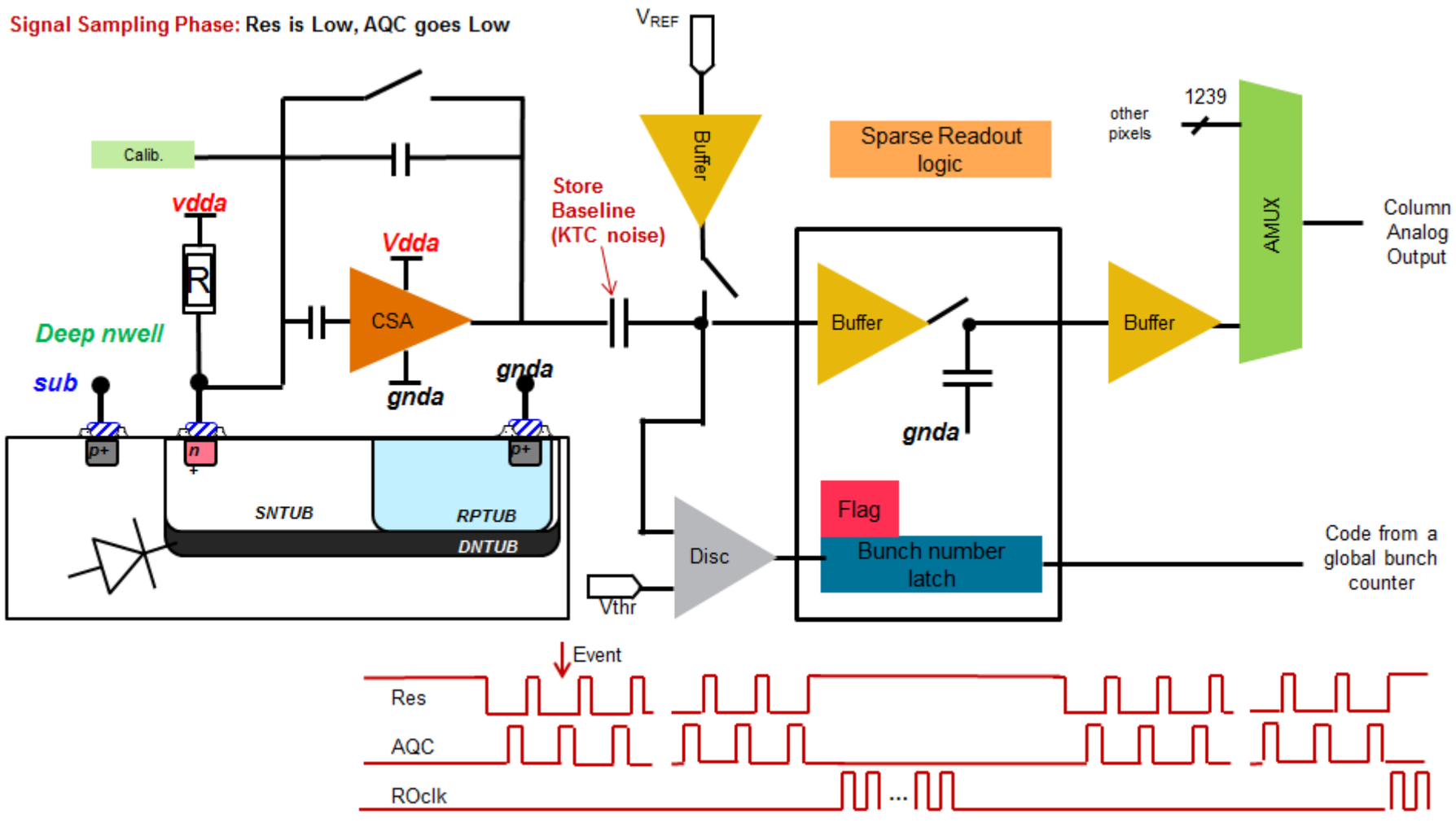


Pixel Tracker

- Obvious advantages for pixelating tracker
  - More robust pattern recognition
  - Thinner sensors so reduced mass
  - Standard CMOS so may be cheaper
- **Can power consumption be kept down….???**
- Various groups now working on this
  - Overlap with LHC upgrades
- **Needs detailed simulation**

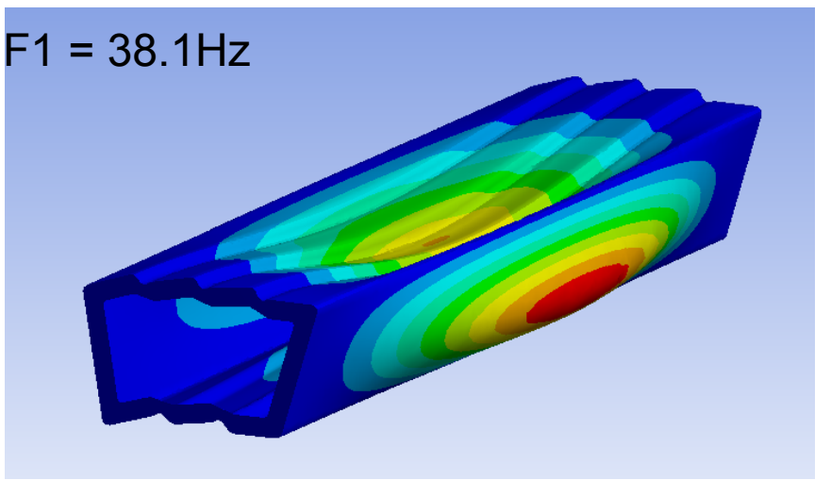
MAPS KPIX

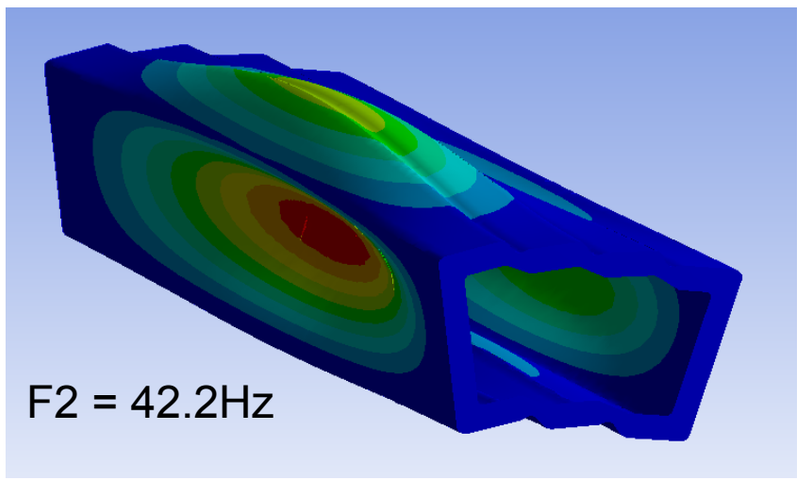
* SLAC KPIX-M 50μmx500μm pixels, S/N>20

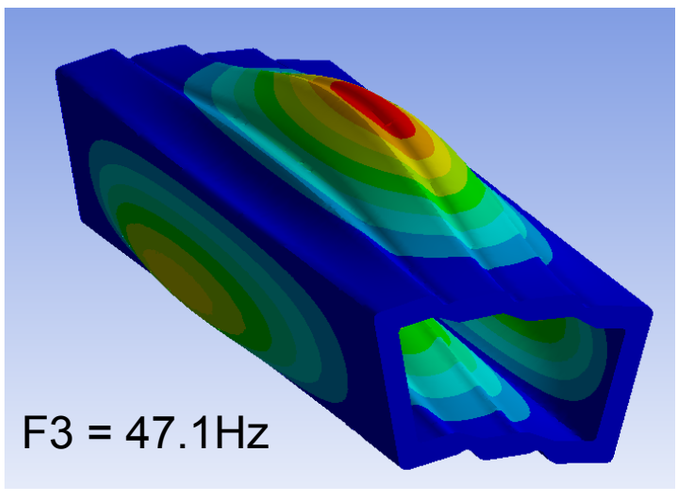


UK Pixel Tracker

- Simulations
  - Required spatial and temporal granularity
- Mechanics
  - Can sufficient gas flow be guaranteed?
  - FEAs of box channel structure
  - May be able to prototype…?







Summary

- SiD baseline vertex and silicon tracker design
- Low mass, single bunch timing
- Steady progress towards vertex technology
- CMOS pixel tracker real possibility
- Hope to validate soon