The Si-W ECAL system will not be modified (except at its interfaces)

- Can be considered as a black box
- Known hardware & software interfaces
- External master system provides necessary signals/software orders
- Conversion from 5 MHz to 50 MHz **not** provided (can be external or internal to the main supervisor)



Si-W ECAL hardware interface

- Connector and electrical format and waveforms: to be implemented into the master system
- LEMO 00 connector for SPILL signal, TTL 5V, active low
- LEMO 00 connector for TRIG_ext signal, TTL 5V, active high (clock synchronization OR stop_acquisition in TB mode)
- 50 MHz LVDS clock (SMA or LEMO 00.302 or hdmi) : to be tested
- LEMO 00 connector for BUSY signal, TTL 5V active low : to be re-implemented





IA

Si-W ECAL software interface

- Commands can be sent to a server at a given port with a documented format (see calicoes documentation)
- Master must handle a central state machine sending transition requests to subsystems through normalized communication format (XML for example) over TCP/IP
- A conversion module can be written for interfacing master and ecal server, listening port can be changed.



INC

Synchronization

- Fine clock phase shift must be provided by the master
- Slow clock can be shifted by increments of 20ns (50MHz period) in the DIF (UK procedure established in 2008-9)
- Ecal slow clocks can be aligned thanks to an internal procedure

Time (BCID) measurement

- BCID is provided by skiroc and is included in the raw data
- It is reset at each start spill
- It is incremented at 2.5 MHz, could be a lower frequency according to studies on long slab. Possibility of using 5 MHz is not guaranteed.
- Can be incremented on each TRIG_ext instead of the slow clock (option)

Start of acquisition

- Occurs after a known latency after start of spill transition
- Limited duration of few ms (ILC mode)
- Up to stop spill transition OR first external trigger (TB mode)



