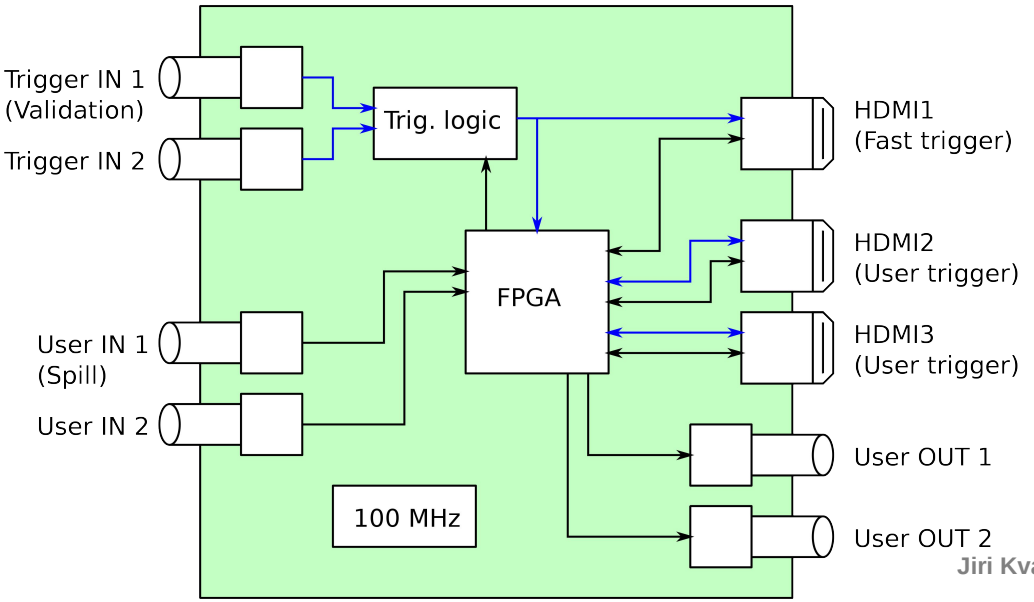
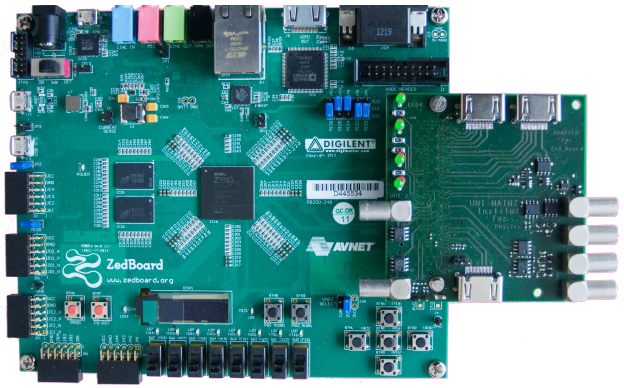
# ScCAL News

- New DAQ hardware (Wing-LDA) ready
  - Now inly 1 LDA connected to the CCC
- Short bamtest this week @ DESY

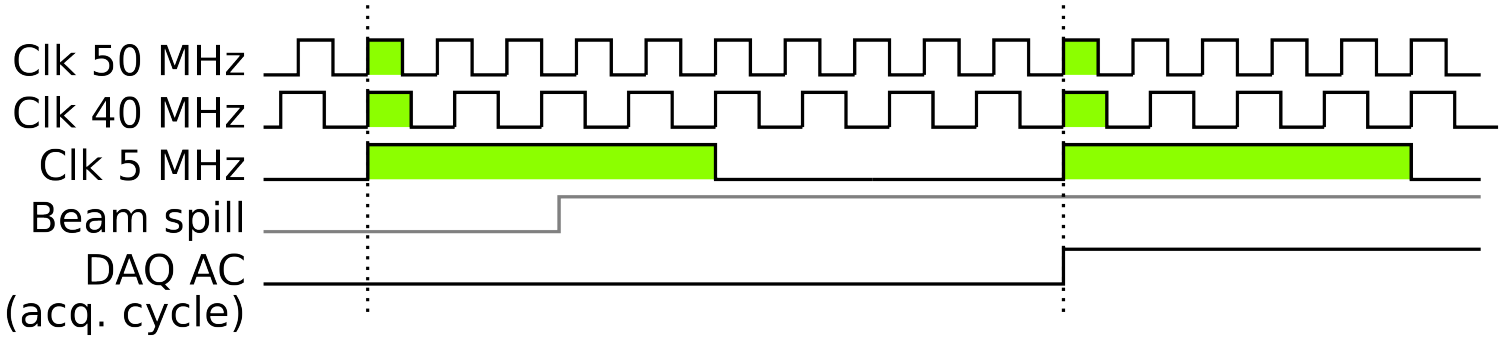
# Sc CCC revised

- ScCCC = CCC mezzanine on Zedboard
- 2 HDMI fully configurable (directly connected to the FPGA)
- 1 HDMI has fixed trigger validation output
- HDMI signals DC coupled, directly connected to FPGA
- User lemos: 2 in, 2 out
- 2 lemo trigger inputs (XOR-ed to single trigger)
- ScCCC can become slave and connect to the master via HDMI
- A hardware platform for master CCC?
  - Has lemos (clk, spill, busy for SiECAL) and HDMIout (ScCAL, SDHCAL)



# Multiclock operation




- Synchronous operation can be achieved easily with different clocks
- Defined common rising / falling edge of the clock
- Master CCC has to control the Readout Cycle / Acquisition Cycle
- Acquisition cycle is
  - Started with beam spill
  - Stopped when at least 1 detector busy/ramfull
  - Started when all detectors are ready (with a new cycle)
  - Stopped when beam spill is gone