News

News :

• SDHCAL restarted yesterday and ready for next beamtest

• Small test setup with all daq for 9 chambers in development (almost finished) for test purpose and Gif++ prototype

Common CCC

At least my view of it…

Physically : could be a DCC (advantages: fpga large enough and many available)
Connectors :
hdmi connectors for whose who use it
2 lemos available
Possible to add a mezzanine for other connectors/ more lemos
Interface to DAQ pc :
Embedded usb
Can imagine tcp/ip (wiznet chip for example) on the mezzanine
Inputs :
Busy from all detectors
Busy from the DAQ
Trigger from PMs or whatever (optional)
Beam start/stop (optional)
Outputs :
Clocks to all detectors (with correct electrical standard for each detector)
Triggers (optional) , act as a fanout or level adapter
Synchronous commands to all detectors (with correct protocol for each detector) :
Resync/Reset command/signal to all detectors
Power pulsing commands (optional)
StartAcquisition command (can be removed according to Busy use)

Misc

Run in SDHCAL :
One absolute Bunch crossing counter that is started at beginning of first acquisition (48 bits @ 5MHz -> ok for a few days) : used to sort different acquisitions in time
Plus one acquisition counter (24 bits@5M-> a few seconds) that is cleared at each start acquisition

1 hour for run duration seems maybe a bit too few (and more or less costless to increase it

Spill counter : can be deduced from absolute BCID and acquisition counter

Timestamp in pc : implemented in sdhcal data but not used for now

Deadtime : a few clock at start acquisition (a few tens of µs if running in power pulsing at power on, adjustable in software)

HDMI : OK (data not used in SDHCAL, data stream goes to usb)

8b/10b : not implemented

Busy : OK