



CALICE DAQ TF meeting

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Topics

1. News from each technology
2. Master clock (concluded)
3. Run/Spill structure
4. Acquisition cycle
5. BX synchronization
6. HDMI connection
7. busy
8. TB plan
9. AOB

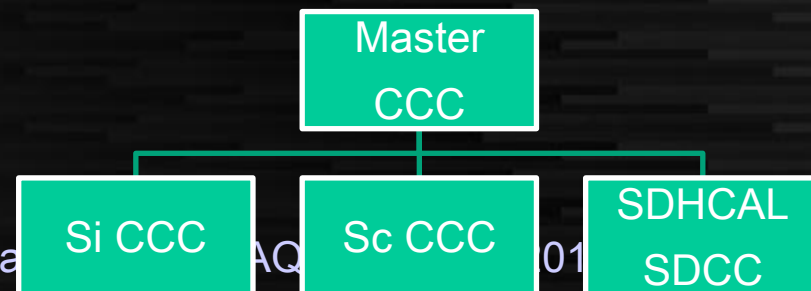
Things to discuss (shown in kickoff)

- Common master clock frequency
 - To assure simultaneous BX counting
- Common BX clock frequency
- BUSY treatment
- → Common CCC? or just clock synchronization?
- High level DAQ software (EUDAQ?)
 - Run control, event building, run number, monitoring,...
- Common data format (LCIO class)

- Partial or optional sharing of firmware and software
- etc.

2. Master clock (concluded)

- Master CCC provides clock to each system
- 5 MHz base clock (considered BX)
- Interface
 - Si: LEMO, have to be converted to 50 MHz
 - Sc: LEMO or HDMI, 5 MHz OK
 - SDHCAL: HDMI, 5 MHz OK



3. Run/Spill structure

- Definition of run
 - Set of acquisition with ‘same’ condition
 - Should be maximum $O(1 \text{ hour})$ or $O(1 \text{ day})$?
- Run number (proposal)
 - XXXYYYYY, XXX is the common TB number
- Spill (from accelerator)
 - in ILC: spill = ‘acquisition cycle’
 - in TB: spill corresponds to multiple AC
 - Do we need a spill counter?
(CCC may be able to count, offline sharing?)

4. Acquisition cycle

- ‘Acquisition Cycle’ or ‘Readout Cycle’
 - Term (AC or RC)
 - Count – 0 from the beginning of run (or beginning of TB?)
- Confirm consistent numbering
 - Timestamp in PC? (easy but not accurate)
 - Other ideas?

5. BX synchronization

- Frequency
 - Si: 2.5 MHz (can be changed in TB mode???)
 - Sc: 250 kHz in TB mode
 - SDHCAL: 5 MHz
- Dead time exists from 'start_acq' to real BX0
 - Si – about 452 usec, can be changed by DIF FW
 - Sc – about 12 usec in CC
 - SDHCAL
 - Si-Sc difference calibrated by data analysis

5. BX sync. (cont.)

- Do we need real 'synchronization'?
- An idea
 - 'Pre-spill' comes via FAST command
 - To prepare power pulsing etc.
 - Spill by another FAST command or Analog line
 - 'Ext trigger' line??
 - Anyhow, need FW of every system
 - Not easy??

6. HDMI connection

- Just confirm
 - clock (CCC→DIF): pin1: +, pin3: -
 - ext_trig (CCC→DIF): pin15: +, pin16: -
 - command (CCC→DIF) pin4: +, pin6: -
 - busy (DIF→CCC) pin7: +, pin9: -
 - data (DIF→LDA) pin10: +, pin12: -
- 8b/10b encoding
 - Si/SDHCAL: Yes
 - Sc: No (will be implemented?)

7: busy

- Status
 - Si: being checked, oscillating
 - Sc: OK, not oscillating
 - SDHCAL:
- Master CCC will collect busy from all to veto the spill (stop/start next AC)
 - We may want to add busy from PC as well
 - Can individual CCC give busy to master?
Si: OK in spec., Sc: SDHCAL:
- Oscillating or not oscillating or accept both

8: TB plan

- SDHCAL in this April-May
 - Si may attend, but low probability now
 - More in Autumn??
- ScCAL in July and August

9. AOB