SciCAL DAQ status

Hardware insight

- Overview
- Hardware + Firmware status
- Performance
- Plans

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CALICE meeting
MPI Munich, 10.9.2015

HELMHOLTZ ASSOCIATION

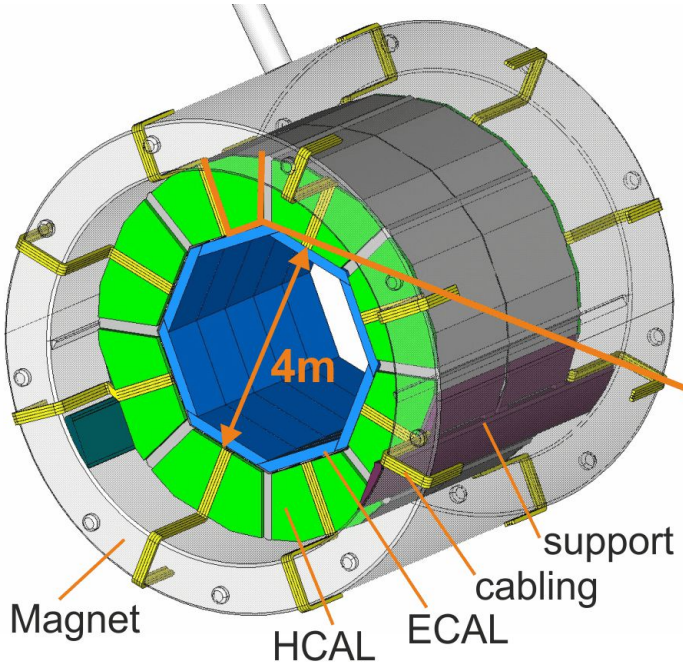
CALICE

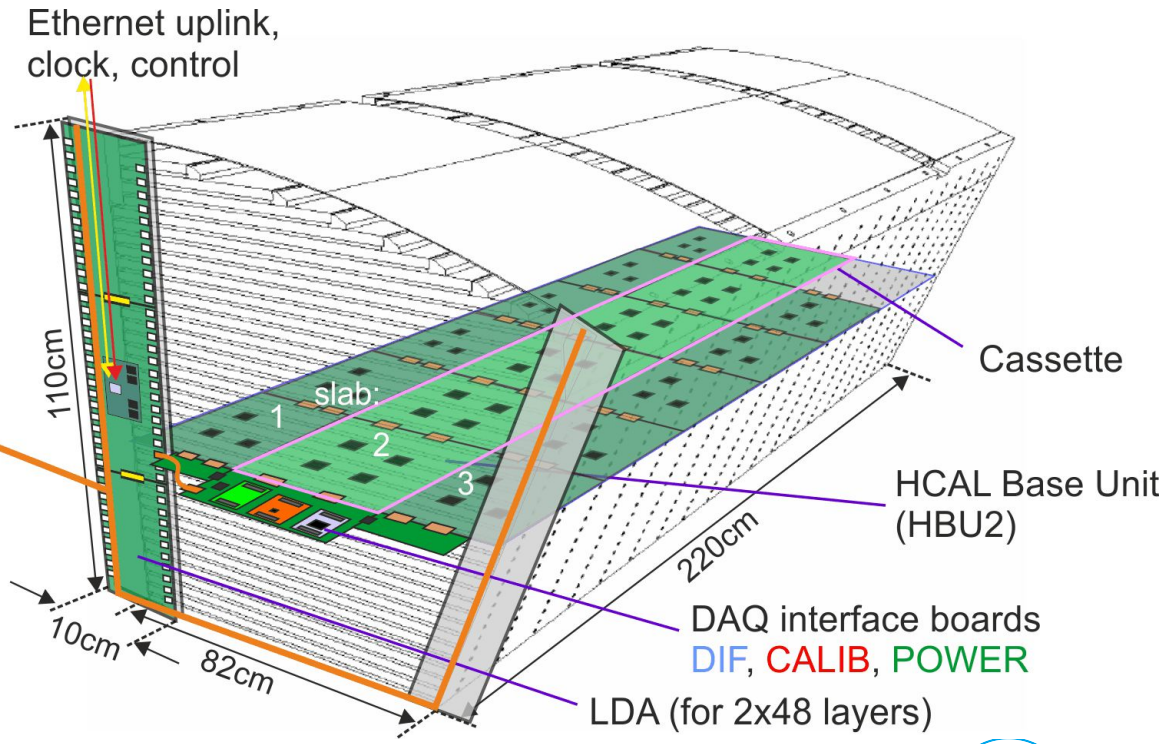
Fyzikální ústav Akademie věd ČR, v. v. i.

DESY

Motivation: The data acquisition

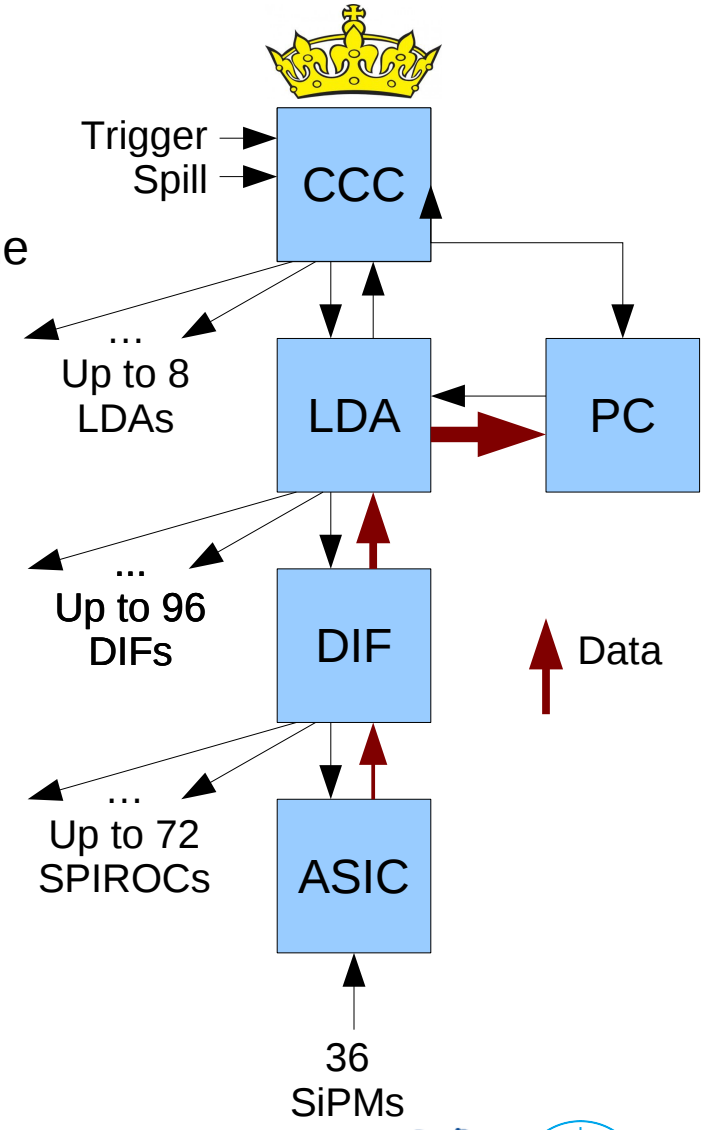
- We are developing a DAQ matching the final ILD needs
  - Control the detector (acquisition control, slow control)
  - Readout data from ASICs
- We need DAQ for both ILD and testbeam
  - Completely different timing requirements





Introduction: DAQ chain

- Chain of devices with a tree hierarchy:
- Clock and Control Card (**CCC**)
  - Provides master clock
  - Starts and stops the acquisition according to the spill level and readiness of all ASICs
  - Distributes trigger validation
- Link Data Aggregator (**LDA**)
  - Packet collecting
  - Packet processing (decoding, merging)
  - Send the packets over TCP to DAQ PC
- Detector InterFace (**DIF**)
  - Controls the ASICs (voltages, acq. state)
  - Collects data from all ASICs on HBU
  - Sends the data to LDA
- ASIC (**SPIROC 2b**, Omega group)
  - Reads out 36 SiPMs
  - Has 16 memory channels for ADC and TDC



DAQ Hierarchy

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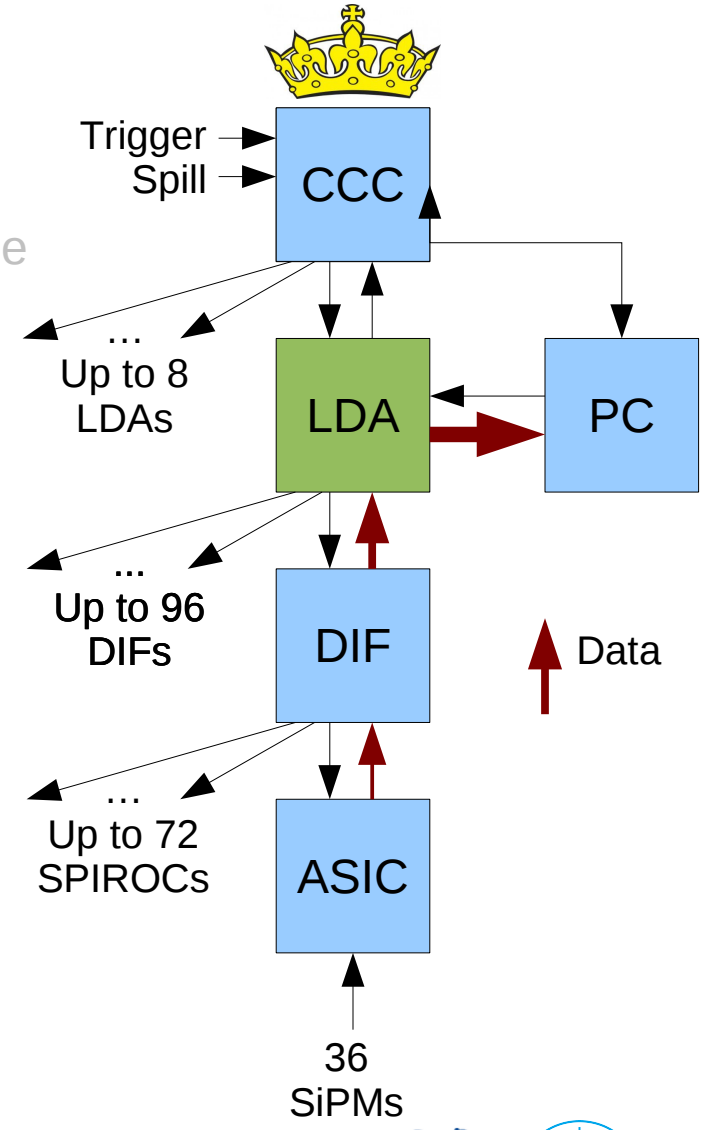
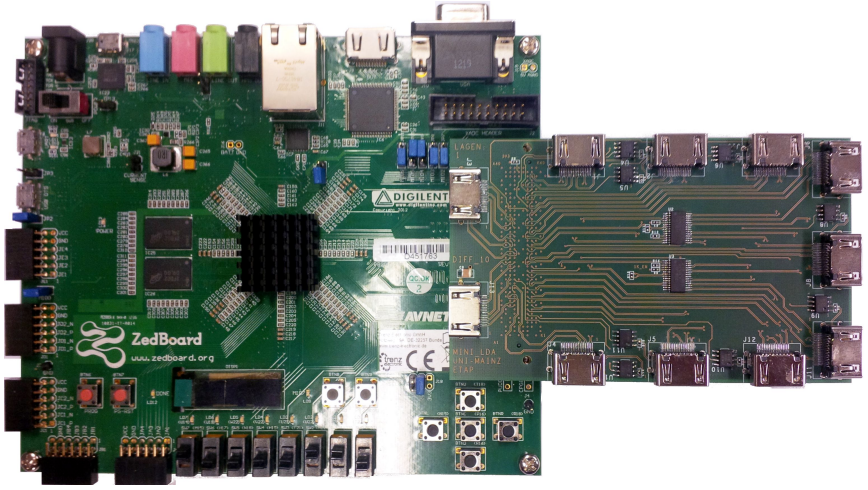
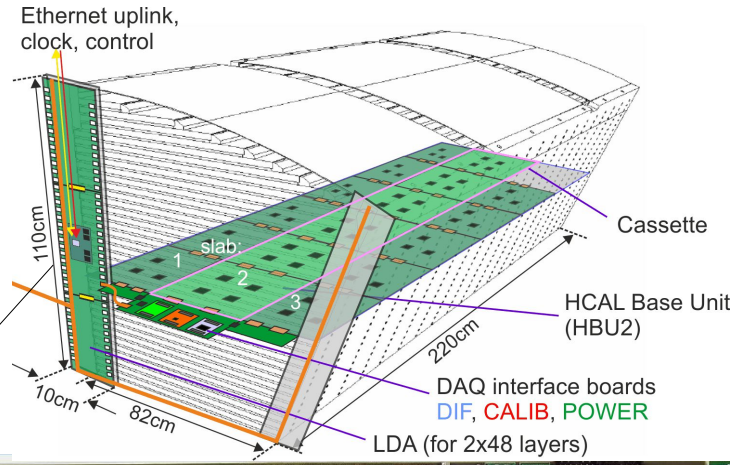
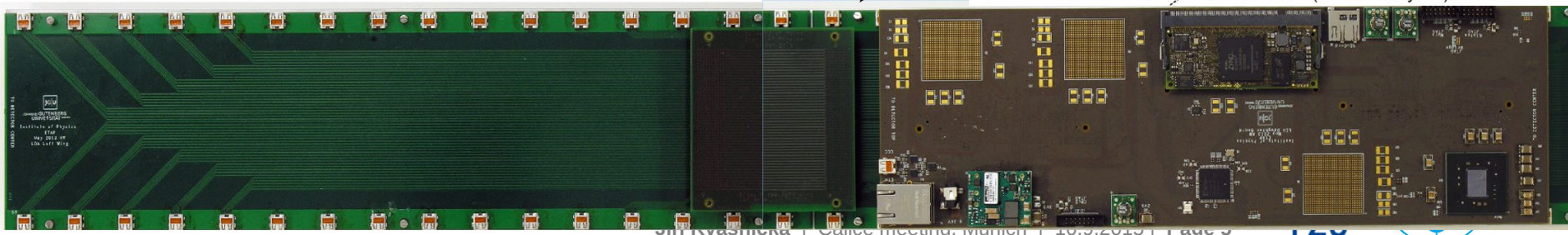


LDA (Link and Data Agregator)

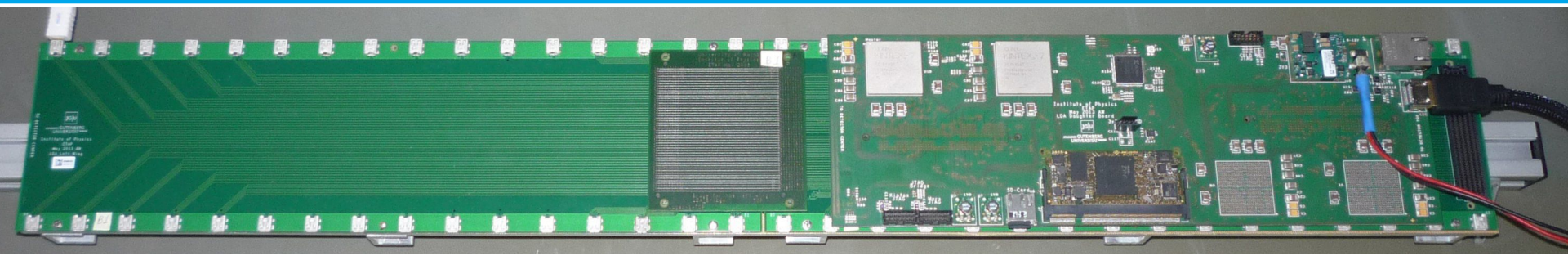
- Two Form factors:
  - Mini-LDA: generic (Zedboard + Mezzanine)
    - 10 HDMI ports
    - Commissioned November 2014
  - Wing-LDA: AHCAL geometry specific
    - 96 micro-hdmi ports
    - Commissioned April 2015
- Hardware: Uni Mainz
- Firmware+SW: DESY + FZU(Prague)
- Same SoC (Zynq 7020) in both form factors
  - SoC (System-on-chip): FPGA + CPU
  - FPGA: strong firmware code share
  - CPU: runs same software (Linux on Zynq) →transparent to the DAQ PC
  - Fast FPGA↔Processor data stream link **non-trivial**, cost us a lot of effort



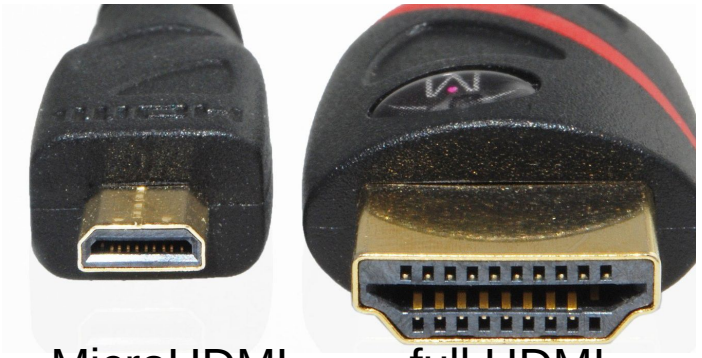




Wing-LDA

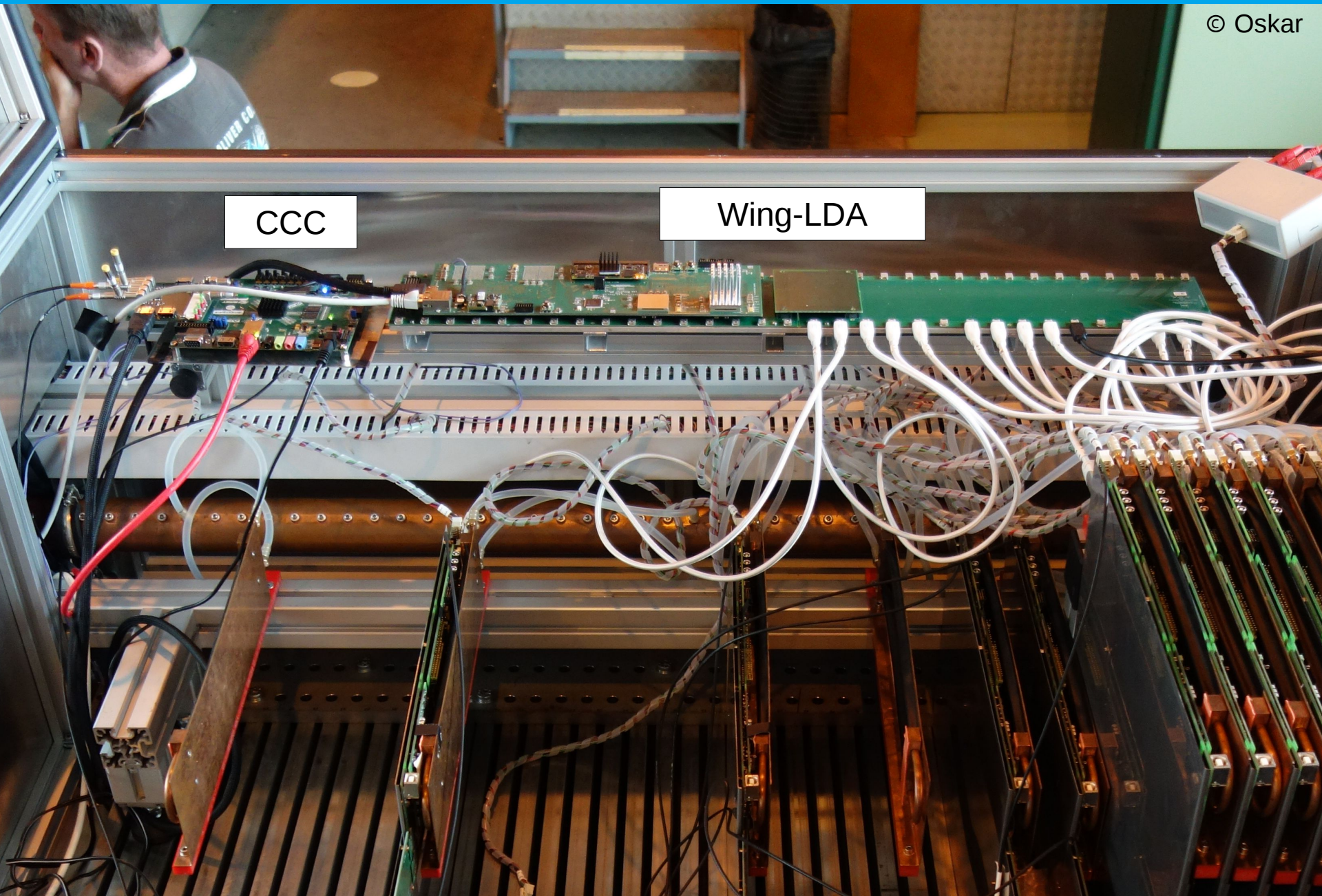


- Designed @Uni Mainz
- MicroHDMI connectors (96), AHCAL Geometry
- Uses commercial Mars ZX3 module (Enclustra)
  - Started with first, pre-production version
- Extra 4 slave FPGAs (Xilinx Kintex-7)
- Not easy to manufacture, all issues fixed
- Commissioned April 2015 (with 1 FPGA)
- Fixes since last meeting:
  - Gigabit ethernet operation fixed
  - HW packet generator (for benchmarking)
  - 1 bug in firmware (wrong parameter value, caused rare corruption of small packets)
  - 1 bug in software part (caused rare stream de-synchronisation under specific, heavy load conditions)
  - Heat-sinks added



MicroHDMI full HDMI

Wing-LDA mounted on the steel absorber, CERN SPS 2015



LDA performance (how fast can it be?)

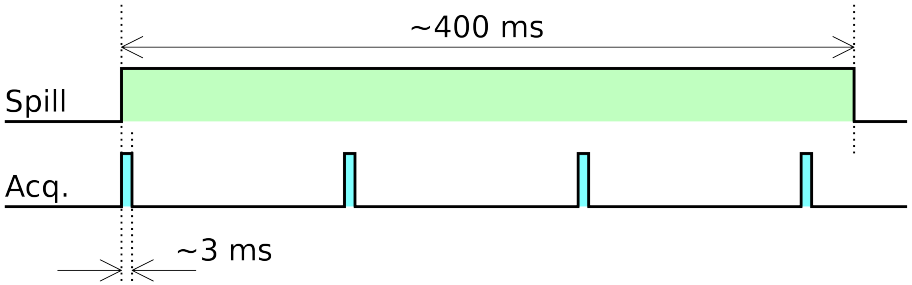
- New benchmarking module in wing-LDA (fake packet generator)
  - Programmable number of layers, asics, triggers
  - Internally generates packets at theoretical ~ 80 MB/s
- FPGA → processor DMA core: can follow at ~78 MB/s
  - Simple transfer from the device node in linux to /dev/null
  - Earlier loopback DMA test: ~200 MB/s
- TCP: processor → Labview: 6 MB/s
  - Measured with 100 Mbit ethernet operation (?)
  - Responsible part: “xldas” program running in the processor
  - Huge room for optimization (remove debug messaging, **do less processing**...)
- Comparison: LED calibration of the full stack (with big layers): 1.6 MB/s

- LDA performance summary:
  - LDA hardware is fast enough for now
  - DMA Data transfer from FPGA to processor is fast enough
  - LDA software is a bottleneck, but still ~4x faster then we can produce the data with all HBU layers we have today

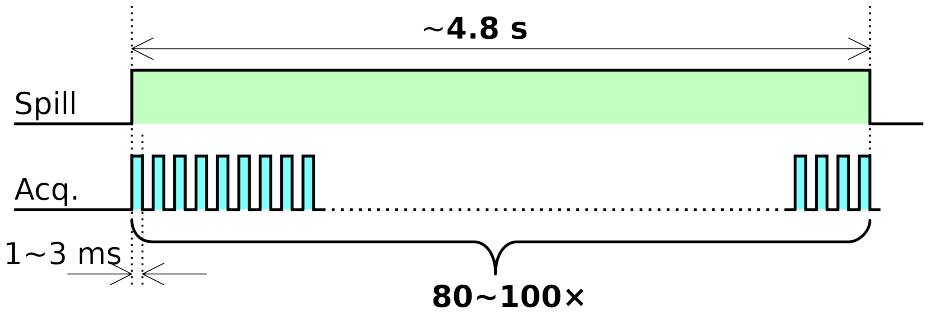
(MB = Mega Bytes)

Beamtest data rates: PS 2014, SPS 2015

TB Dec 2014 (CERN PS)



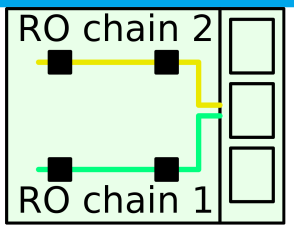
TB Aug 2015 (CERN SPS)



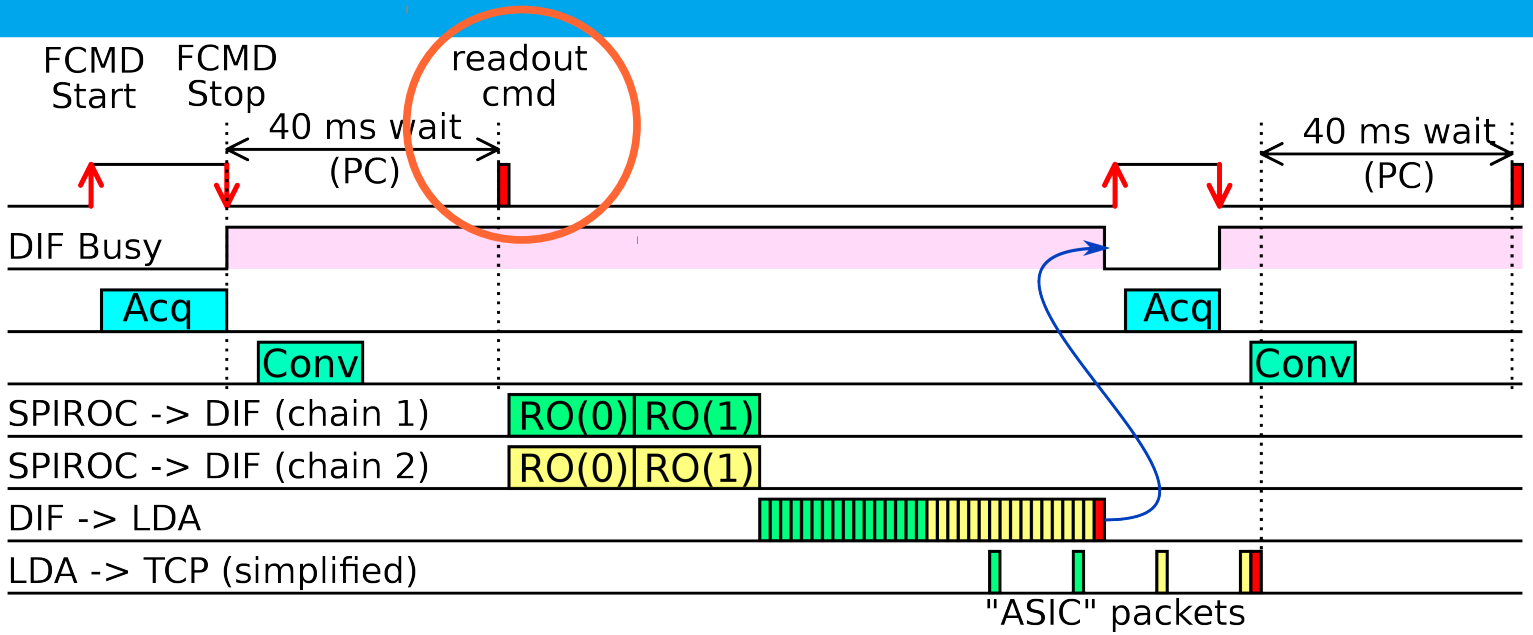
	Oct 2014 (USB)	Dec 2014 (HDMI[1])	Aug 2015 (HDMI[2])	Future ([3])
Sustained LED calib (16 mem. cells)	**1-2**	**3-4**	**6.2**	**12**
Sustained TB (no spill) RO/s	**2-3**	**~6-7 (est.)**	**~17**	**35**
Readouts per 400 ms spill	2	3-4	7 (Est)	14
Theoretical events per 400ms spill	30	45-60	105	210
Theoretical sustained phys.events/s	**~30**	**~100**	**~255**	**~525**

[1] Explicit RO command
[2] Automatic data send
[3] Foreseen DIF speedup

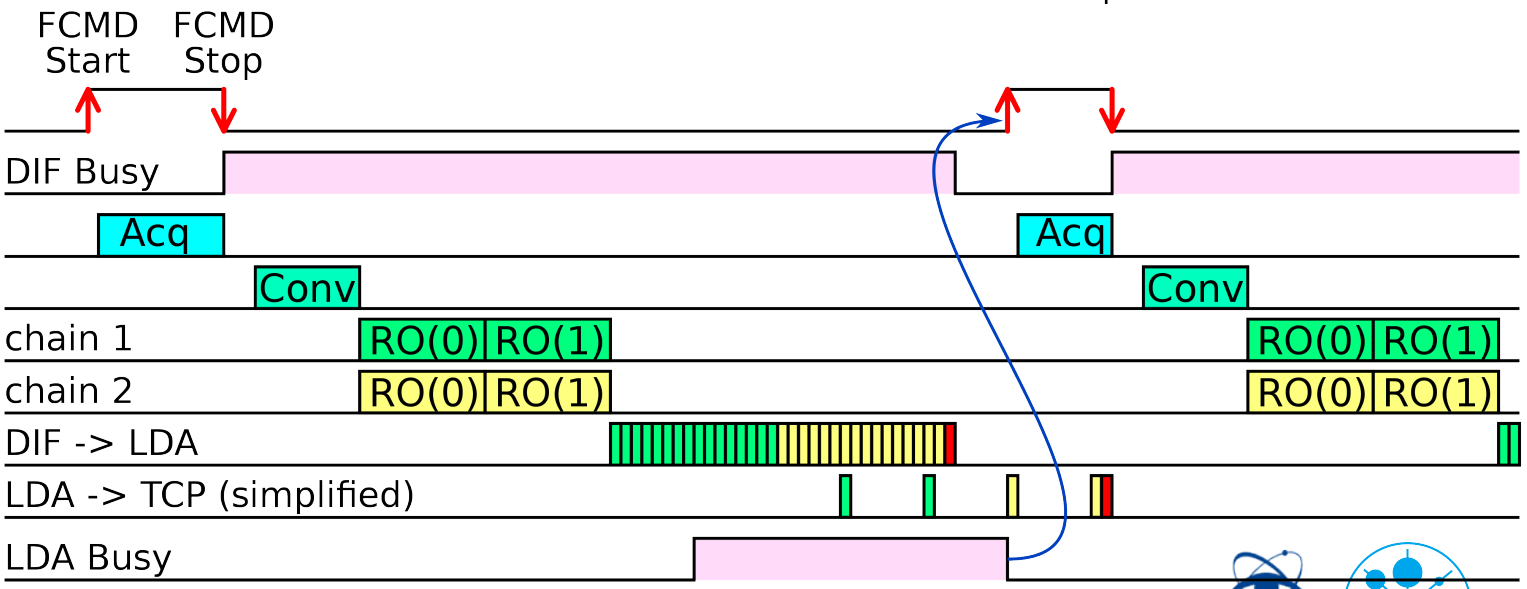
DAQ timing update



2014: Explicit Readout command

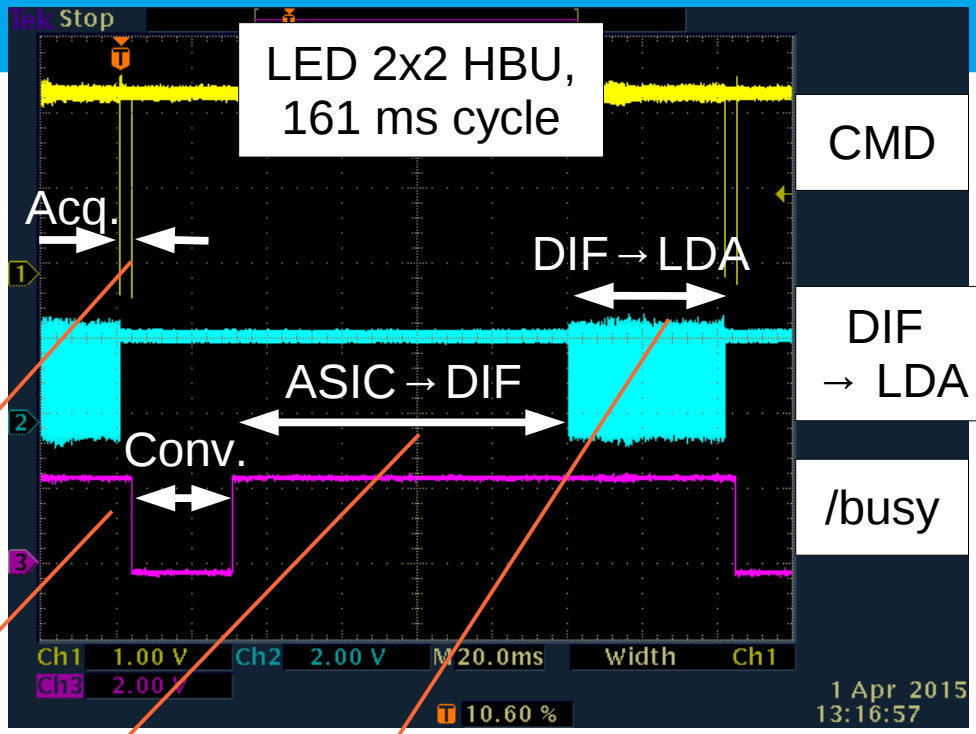


2015: Command-less

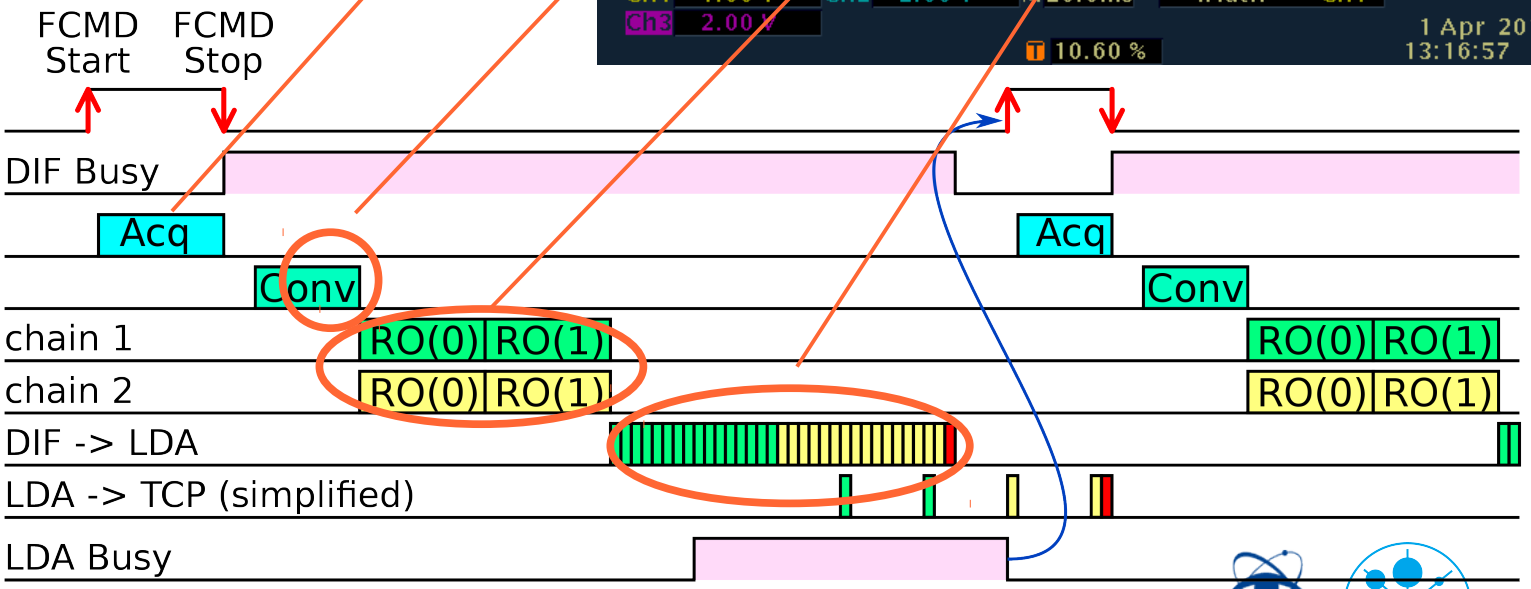


DIF speedup in detail

- Speedup → faster LED calibration
- Plan for DIF speedup:
  - Check for end of conversion: (?)
  - SPIROC → DIF data transfer: < 3×
  - DIF→LDA data transfer: 4×

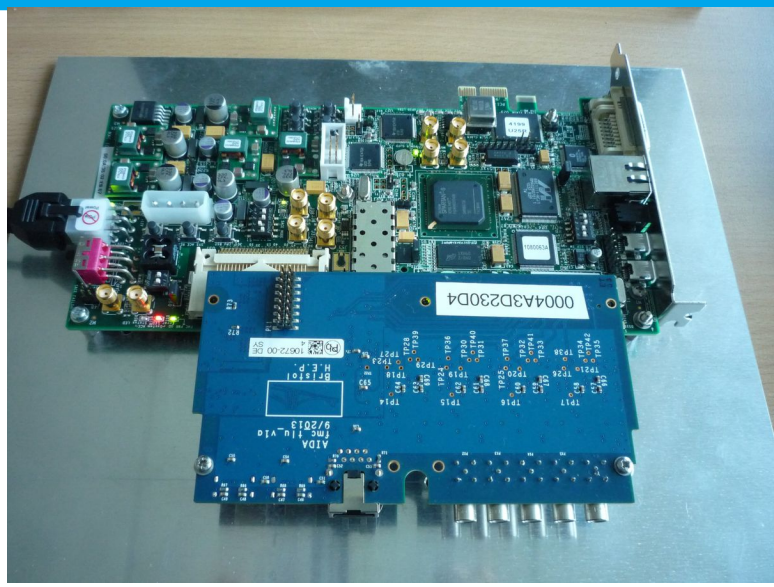


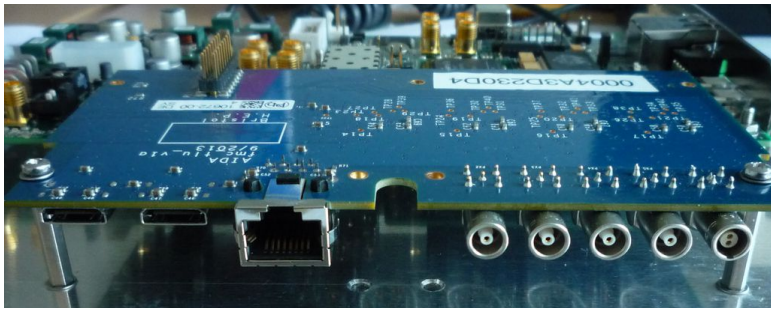
2015:
Command-less



DAQ tasks & plans (1)

- BIF (Beam interface)
  - Motivation: Avoid T0 inputs to HBU
  - Time stamping of trigger sources for later analysis (beam instrumentation, local trigger scintillators)
  - Currently exploring extendability of AIDA **mini-TLU** to this purpose
    - TLU: Trigger logic unit, used for eudet telescope
    - Custom mezzanine board on the ML605 board
    - Can do the timestamping
    - I hope for plug & play
  - Status: setting up the compilation environments (Xilinx and Mentor Graphics)
- Firmware for the new DIF (new FPGA)
  - First version: will based on current firmware
  - New clock distribution
  - incorporate new signals
- (current) DIF
  - Unify the firmware for 1 slab and 2 slabs
  - Optimize for power pulsing
  - Speedup
  - Implement packet CRC checksum calculation





DAQ tasks & plans (2)

- Common DAQ control
  - More hardware parts can do the job: Sc-CCC, GDCC, TLU
  - Interface between the common CCC and subdetector CCC agreed (see Taikan's slides)
  - Needs to be implemented
  - Sub-detector CCC interface needs to be implemented
- LDA
  - Currently commisioned, changes have **low priority**
  - Wing-LDA: Get running 2nd FPGA
  - DMA core: doesn't work with new Linux kernel 3.19 in vivado 2015.2 suite → needs fix
  - Fix the 6MB/s software bottleneck in xLDA
  - Wing-LDA: Equalize the output delays for 48 HDMI ports
  - Wing-LDA: Add more debugging to the FPGA – FPGA link
  - Add simple start-stop CCC functionality into the LDA so that the layer can be operated with just a single xLDA configuration (without the CCC)

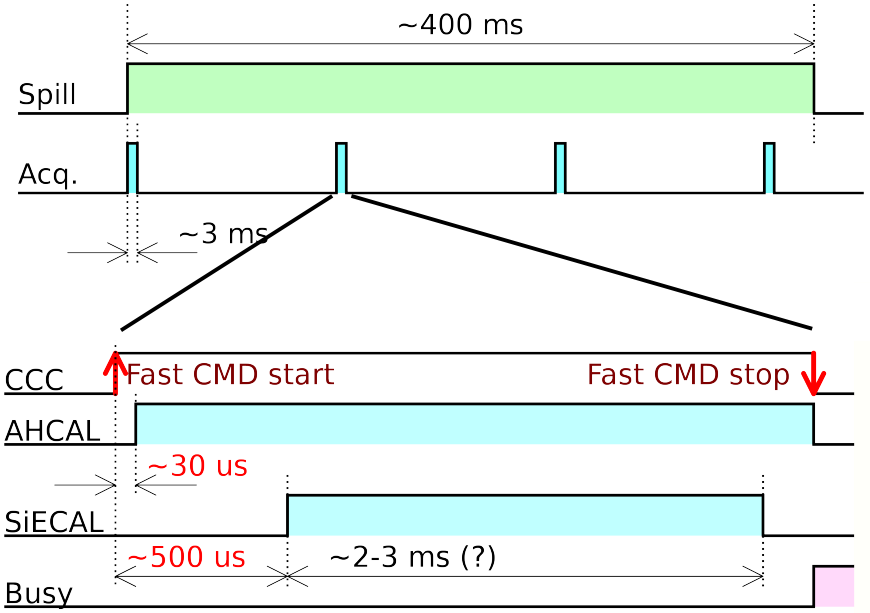
Summary

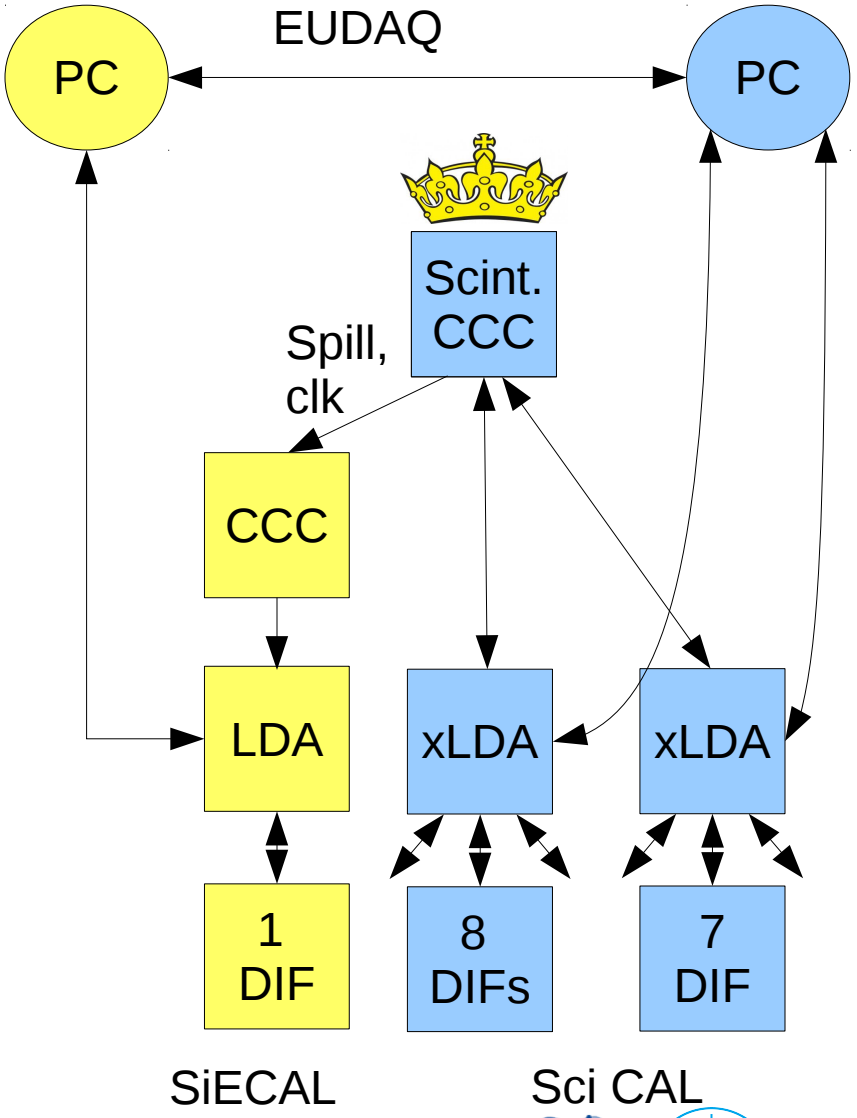
- Huge progress (We were still using USB a year ago)
- Stable DAQ hardware in 2 form factors (Mini-LDA + Wing-LDA)
  - Just small fixes since last meeting (April 2015)
  - 2 successful CERN testbeam campaigns
- Improving speed
  - 17 ReadOut Cycles/s with 15 layers (was 6~7 ROC/s Dec 2014)
  - DIF is now on turn for speedup
- Hardware plans
  - New DIF (Detector InterFace)
  - BIF (Beam InterFace)
  - Common (Master) CCC
  - LDA improvements

Backup

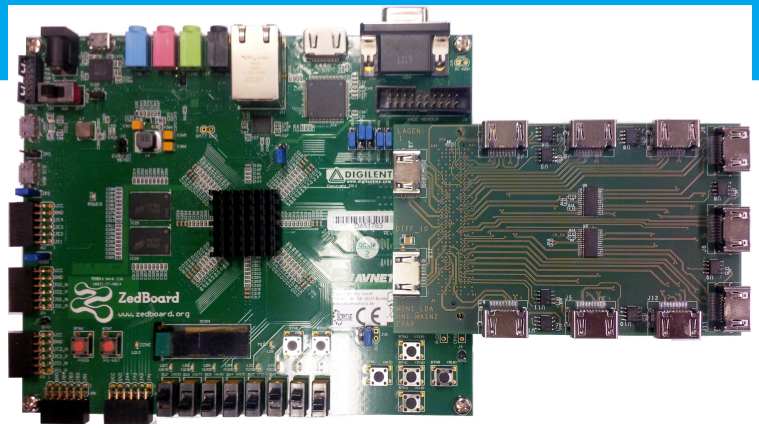
Common running with SiW ECAL @ CERN PS 2014

- AHCAL + SiW ECAL layer
- SiW ECAL System differences
  - 50 MHz clock (vs. 40 MHz)
  - No busy / Memory full (re-enabled in the Si ECAL DIF by Remi)
  - Only Spill input
  - 2.5 MHz BXID (vs. 250 kHz)
  - No TDC
- EUDAQ as common DAQ SW
- Common properly timed events found!



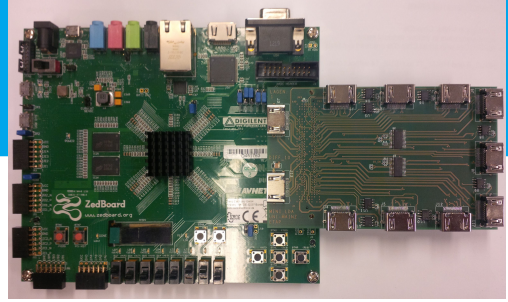


Mini-LDA

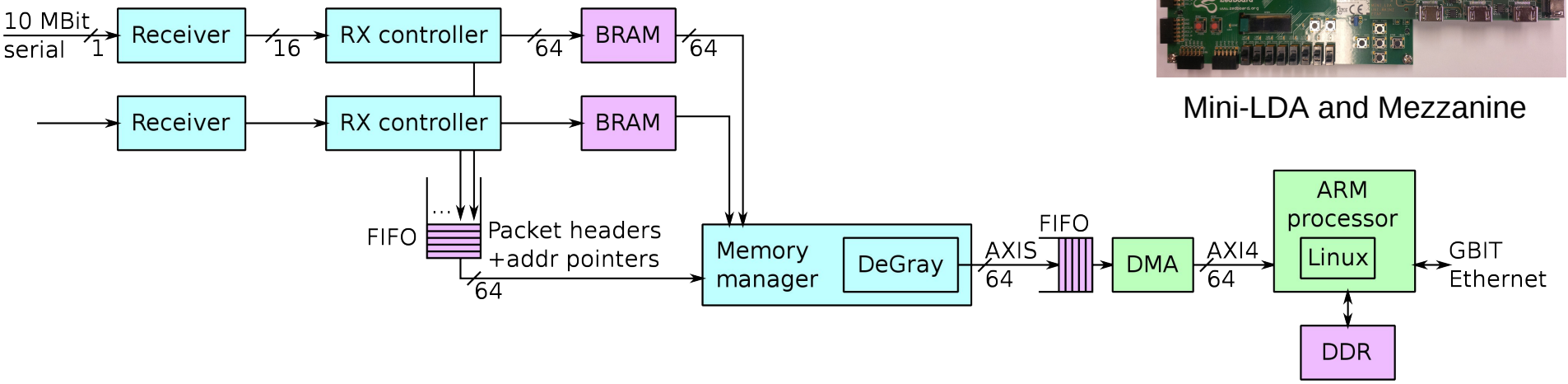


- Implementation done since Sep 2014
- Serious problems observed in the FPGA ↔ Processor link (GPIO):
  - Data corruption in the Linux memory
  - Performance limit reached
- FPGA ↔ Processor link had to be updated to DMA transfers
  - Used AXI4-Stream bus in the FPGA
  - Used Xilinx DMA IP core
  - 230 MB/s loopback speed (Linux user memory → DMA → FPGA → DMA → Linux)
  - 13 MB/s with small packets (random size, 8kB max) and TCP transfer
- Another bug (kernel memory leak) observed in Xilinx Linux DMA driver
  - Kernel module for the DMA transfers rewritten (just for “simple transfers”)
- Stable operation since Oct 2014

LDA Architecture 1 (DIF → AXI-stream)



Mini-LDA and Mezzanine

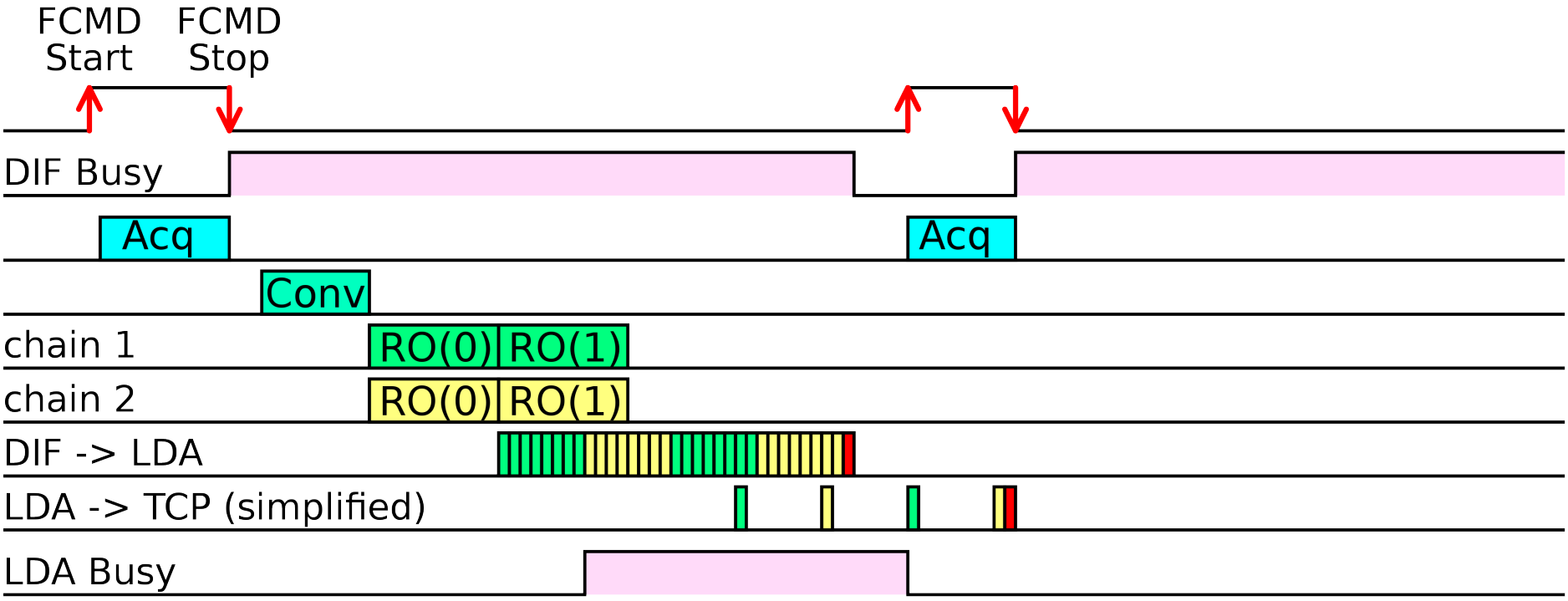


- 40MHz internal operation
- Each port has enough memory to hold complete layer data
- Small packets are merged In the “ASIC” readout packets
- Packet pointer is sent to the queue
- Memory manager collects all packets according to the pointers, decodes them and sends the to a large FIFO already on AXI-Stream bus
- Xilinx DMA core controls the transfer to the main memory

LDA Architecture 2 (AXI-stream → TCP)

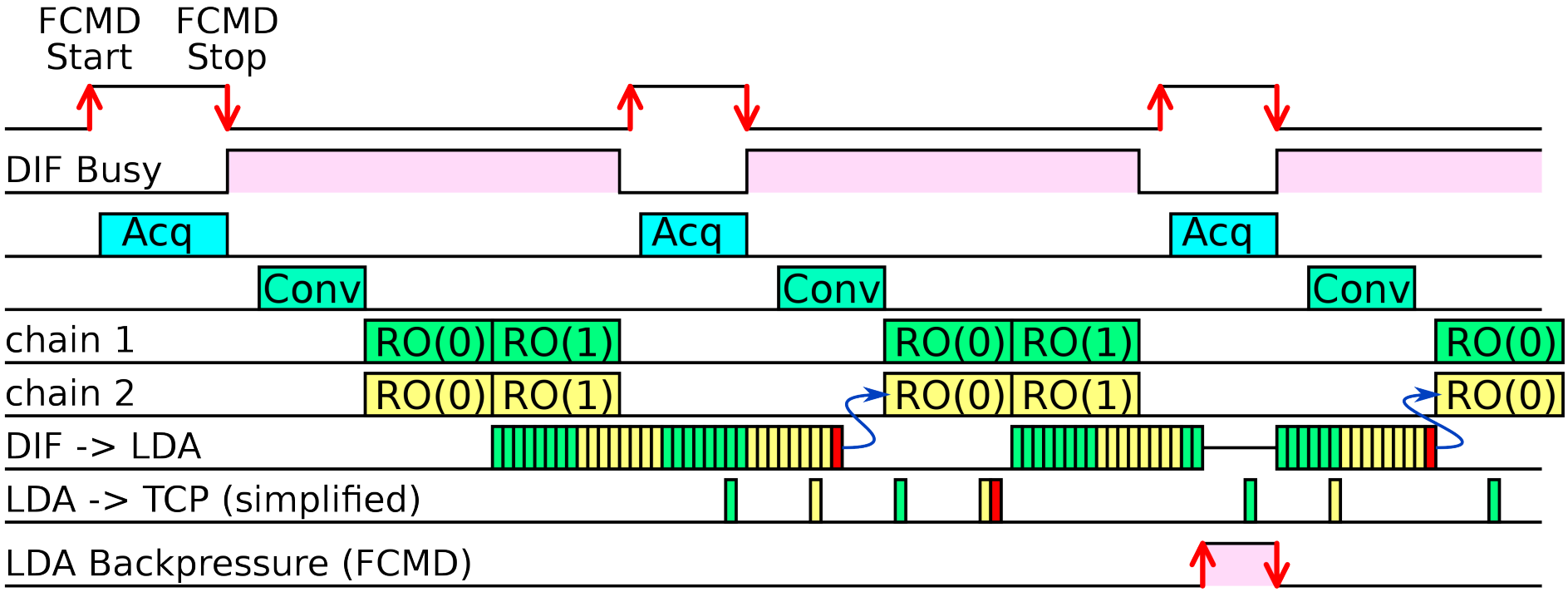
- DMA transfers are made by Xilinx DMA IP core
- First version developed with close cooperation with Mainz
- Bug in the Xilinx kernel driver observed => driver had to be rewritten
- Current version talks directly to the DMA core via IO calls from kernel
- Benchmark result
  - 210 MB/s via loopback in the FPGA and 128 kB packets (first version)
  - 13 MB/s with random packet generator (4B – 8kB)
  - 4000 transfers/s (poor performance => packets merged as much as possible in LDA)
- Performance not fine tuned, tuned for stable operation only

Parallel readout and sending data



- In principle we can start sending the data from DIF as soon as there is a full ASIC data in the DIF memory.
- => needs more effort on the DIF side

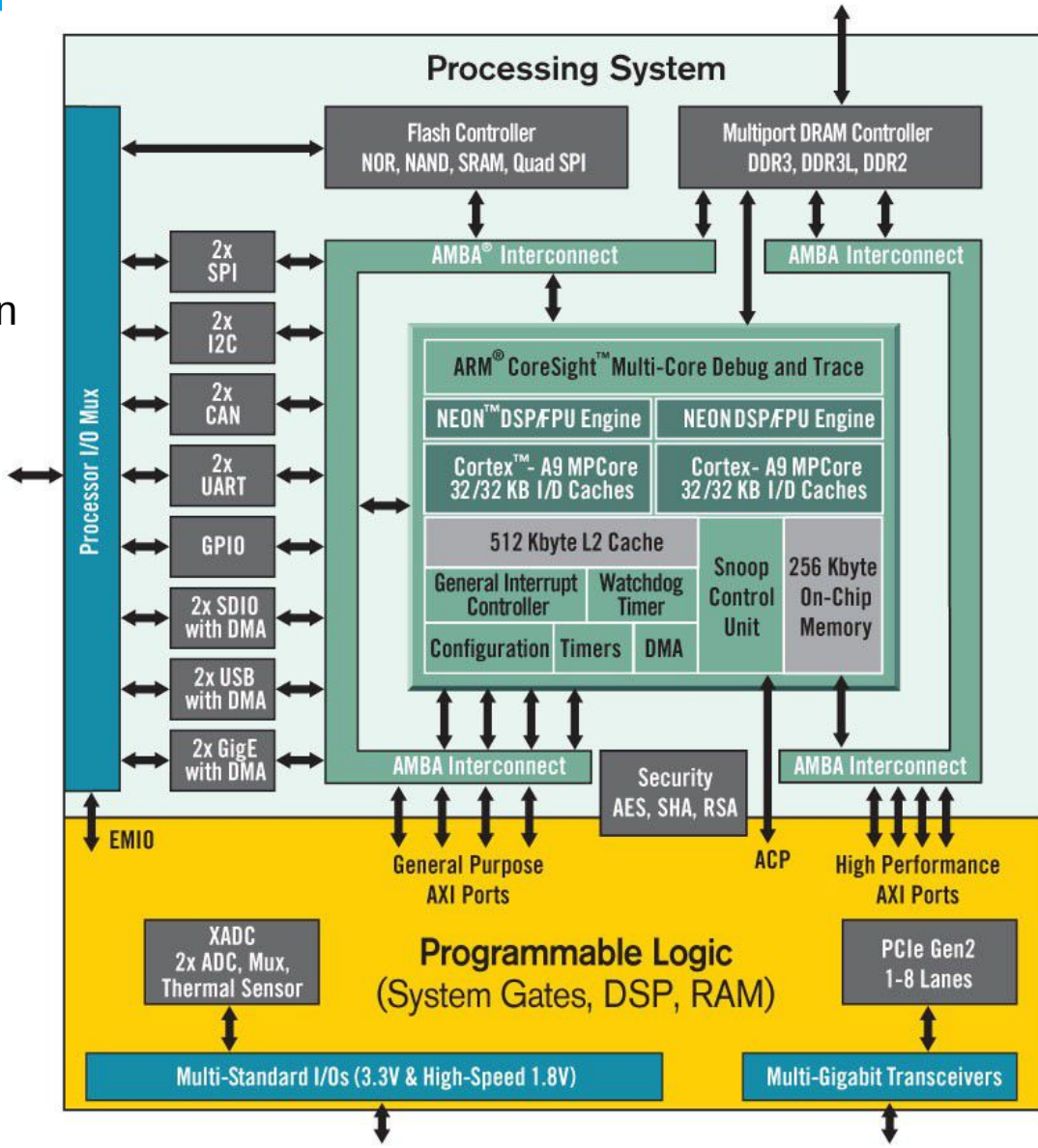
Independent data sending



- We can (the DIF is capable of) start new acquisition as soon as all SPIROCs are fully read out
- DIF → LDA transfer will run in parallel (on the background)
- LDA backpressure mechanism needs to be implement
- Danger of EMC noise during acquisition
- RO cycle number has to be provided by DIFs (not LDA)

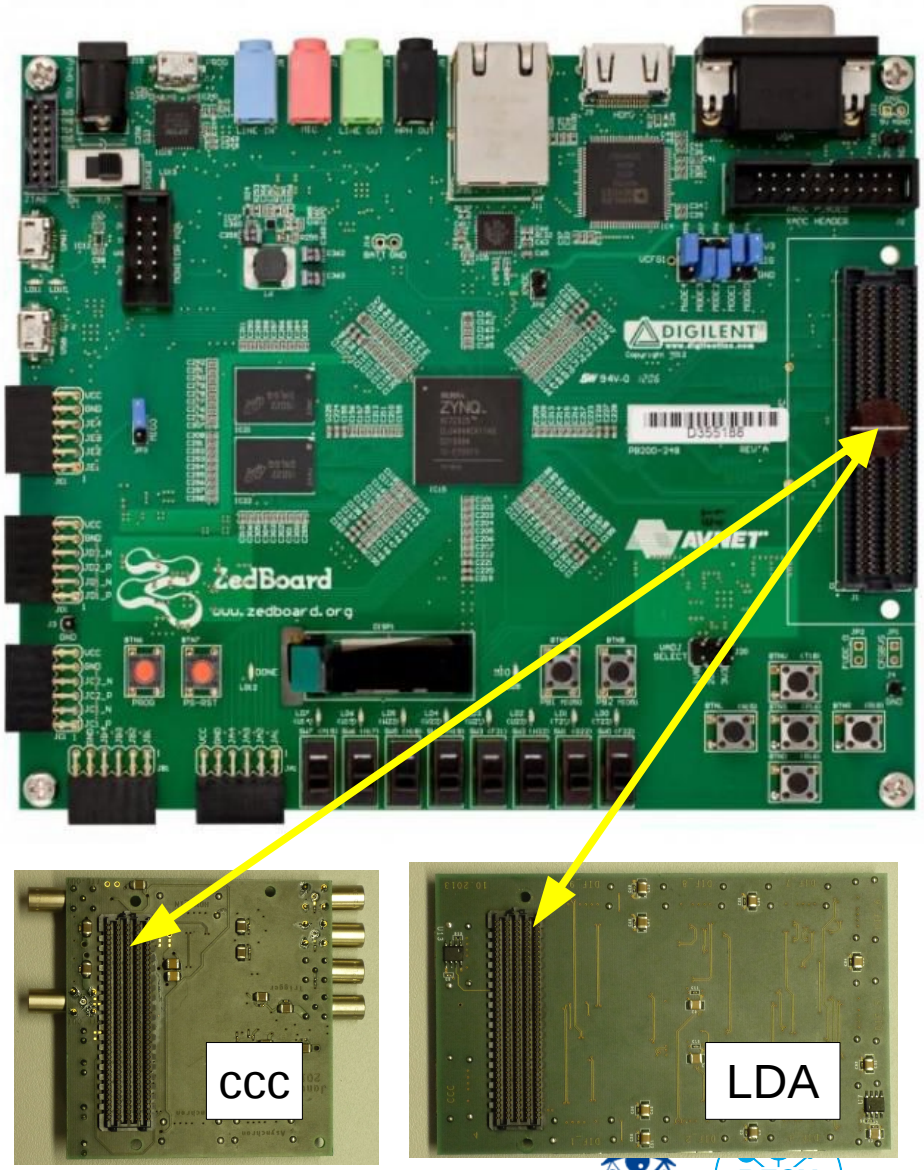
Zynq and SoCs (System On Chip)

- Xilinx ZYNQ SoC (XC7Z020)
  - FPGA (Artix-7 core)
  - Dual-core ARM processor
- Huge interconnect bandwidth
  - DDR Memory can be shared between FPGA and processor
- Can run a small Linux (~15 MB)
- Unique price vs. power
- Rising trend of FPGA vendors
- Not the only SoC in the world. Alternatives:
  - PowerPC IP in Xilinx Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6
  - ARM in Altera SoCs since 2012
- No Processor in FPGA? FPGA can become anything. Even a processor?
  - Xilinx: MicroBlaze
  - Altera: Nios
  - Many others: LEON, PicoBlaze, 8051, x86...



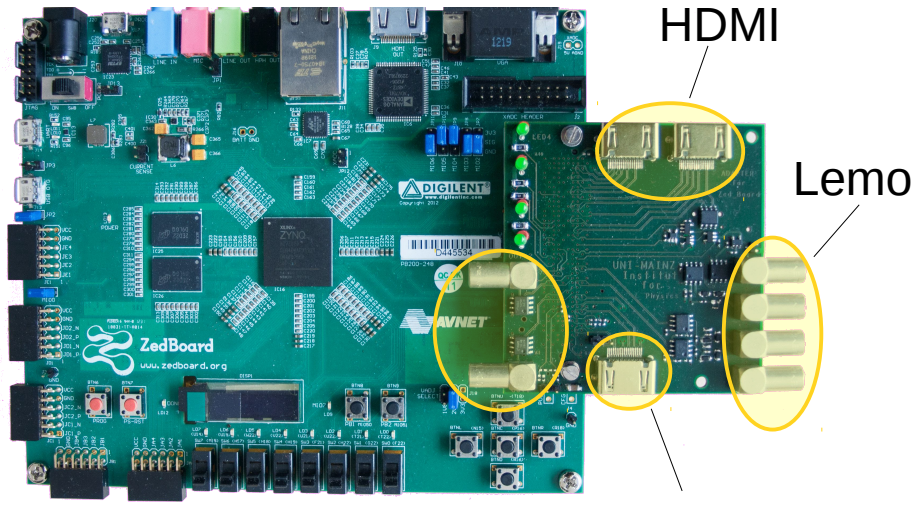
DAQ Hardware components: Zedboard + Zynq

- **Zedboard**: affordable commercial development board from Digilent
- 512 MB DDR3 memory
- 1 Gbit Ethernet
- FMC (FPGA Mezzanine card)
  - High pin count, high bandwidth
  - Custom mezzanines from Uni Mainz
- Xilinx **ZYNQ** System on chip (SOC)
  - FPGA (Artix-7 core)
  - Dual-core ARM processor
  - Can run a small Linux

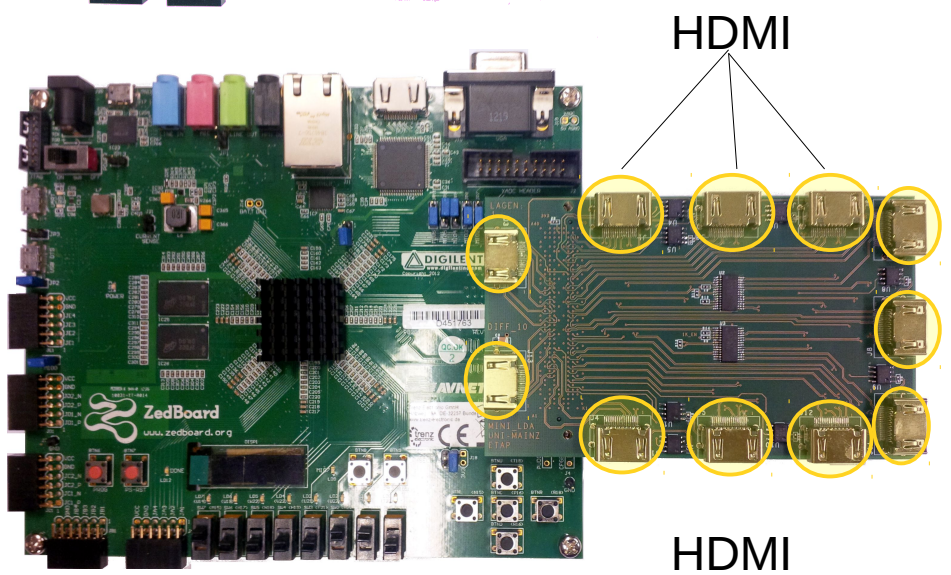


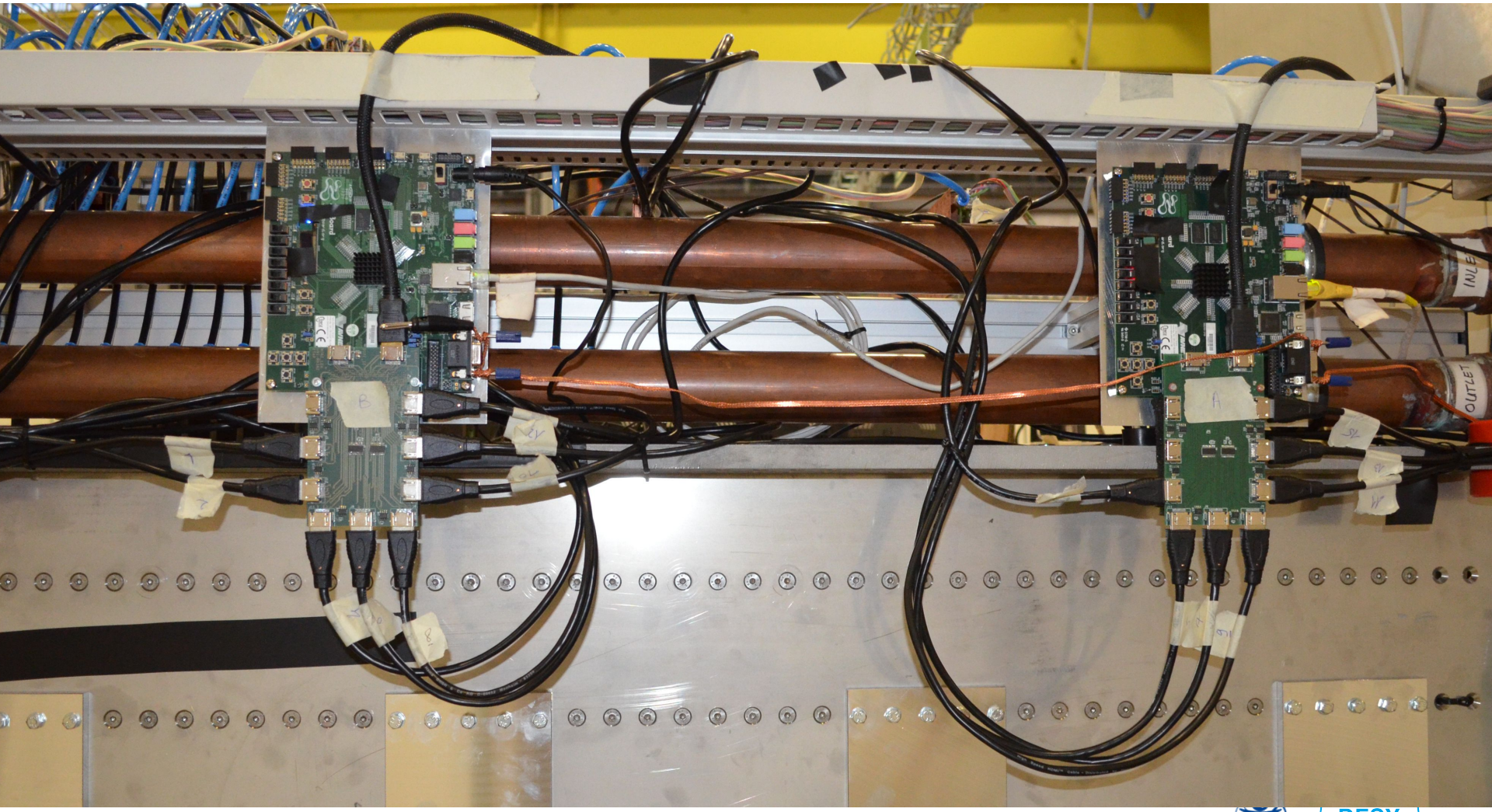
CCC + Mini-LDA Ports

- CCC (Clock and Control Card):
  - Zedboard + CCC Mezzanine (Mainz)
  - Clock source
  - Lemo inputs for trigger and spill
  - 2 configurable lemo outputs
  - 3 HDMI ports to LDAs
  - Accessed via TCP and Piconf software (Mainz)



- LDA (Link Data Aggregator):
  - Zedboard + LDA mezzanine (Mainz)
  - Hardware @Mainz, Firmware @DESY
  - 1 CCC HDMI ports
  - 10 DIF HDMI ports
  - Accessed via TCP
  - Linux simple data sender
  - Custom Linux kernel module for DMA transfers between FPGA and processor



Testbeam @ CERN PS, Oct / Nov 2014

> 15 layers connected to 2 Mini-LDAs