Reports on the 0.18um SiPM readout chip in HD

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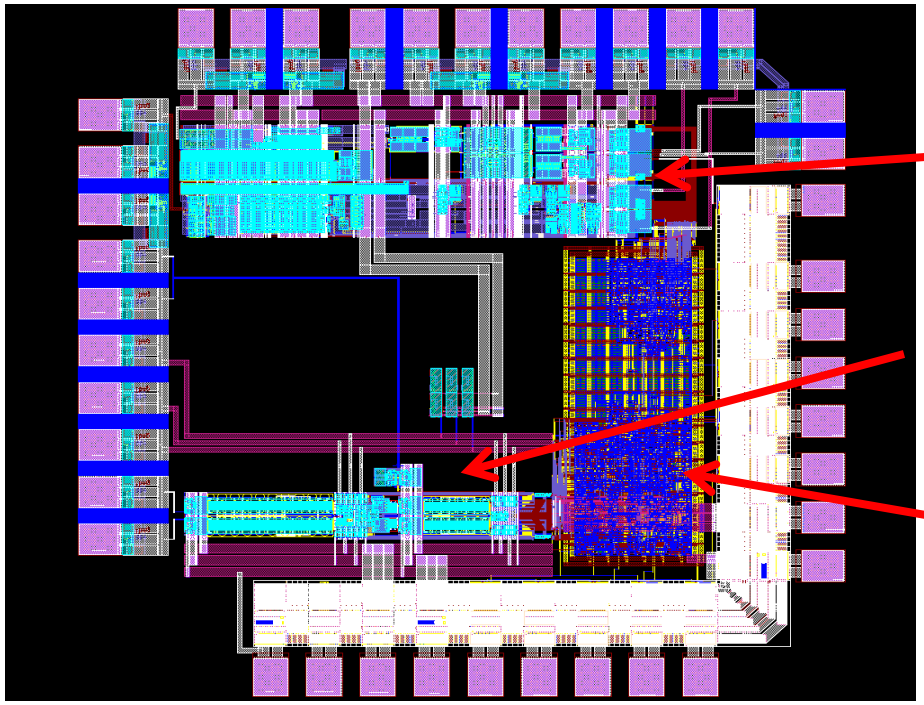
Reminder

- MiniASIC in UMC0.18u CMOS
- tapeout in March 2015, back in July
- one analog frontend channel for SiPM processing
- one SAR-ADC for digitization (10/12 bits)

miniASIC in March



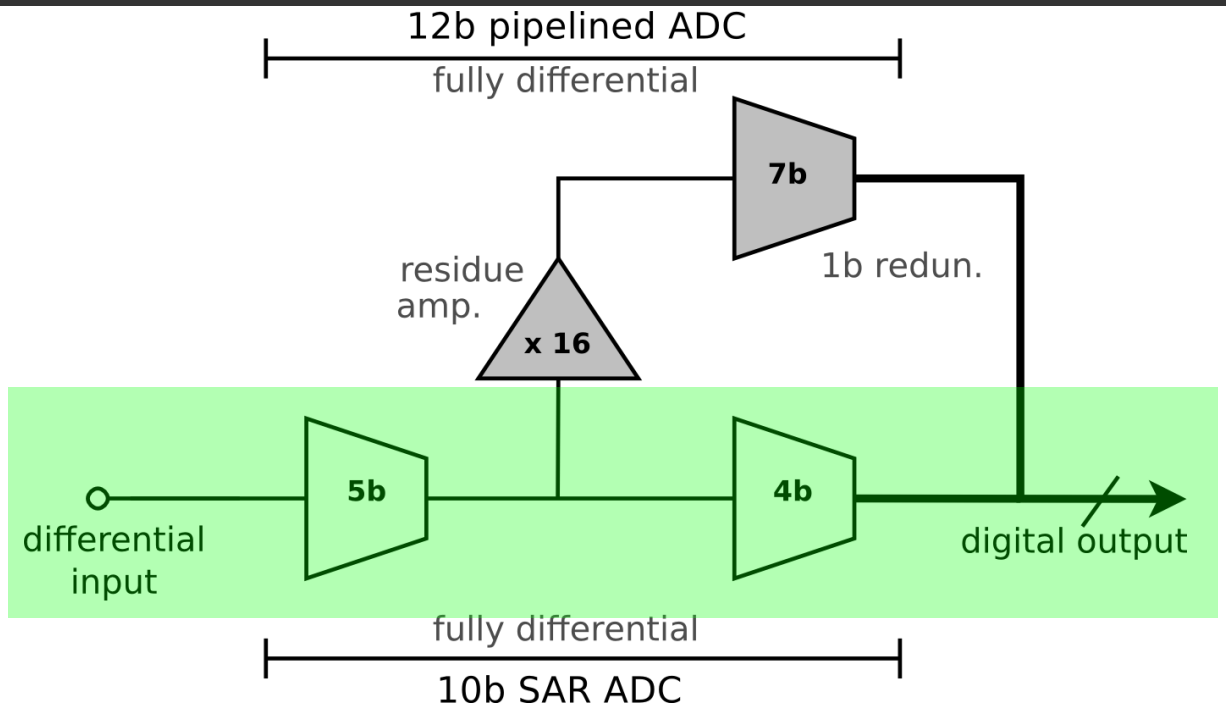
FE analog channel

ADC

digital part

chip on PCB(green)
readout by FPGA(red)

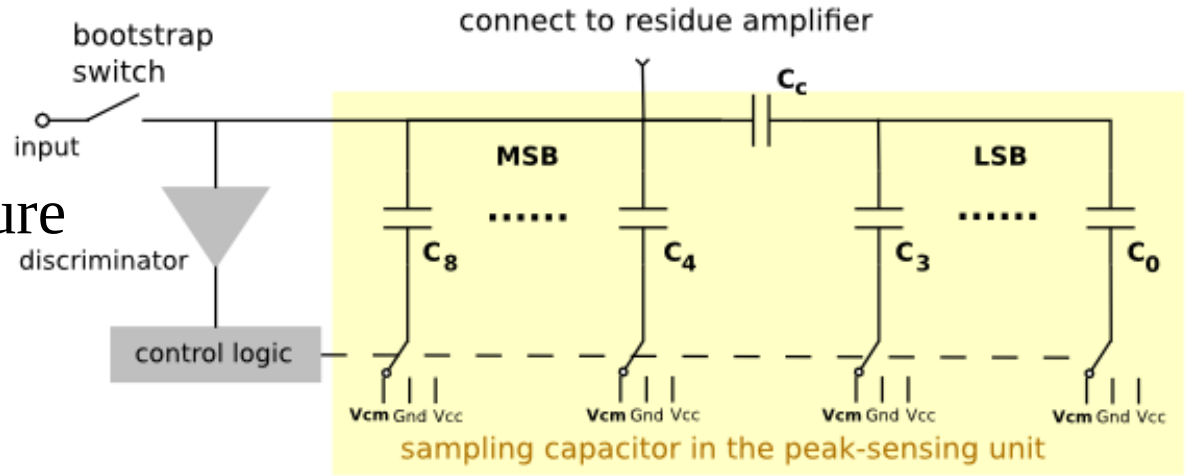
ADC measurements



10 bit for MIP signal
12 bit for SiPM pixels

only the green part
under test now

standard 5-4 SAR structure

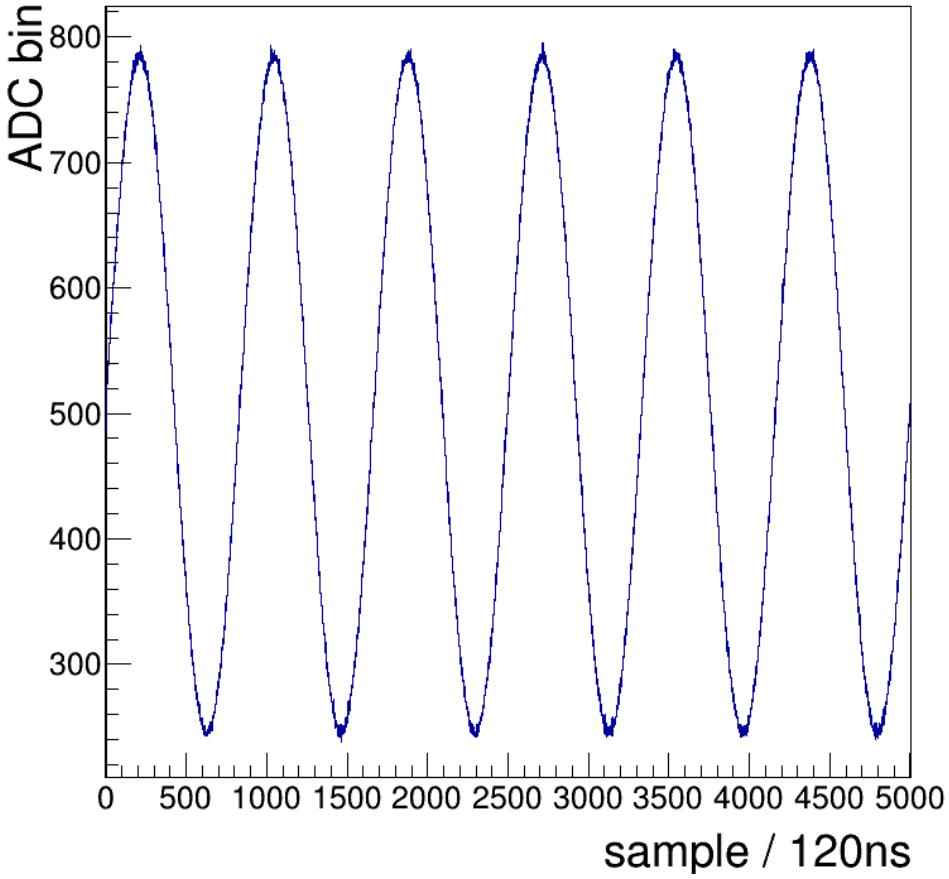


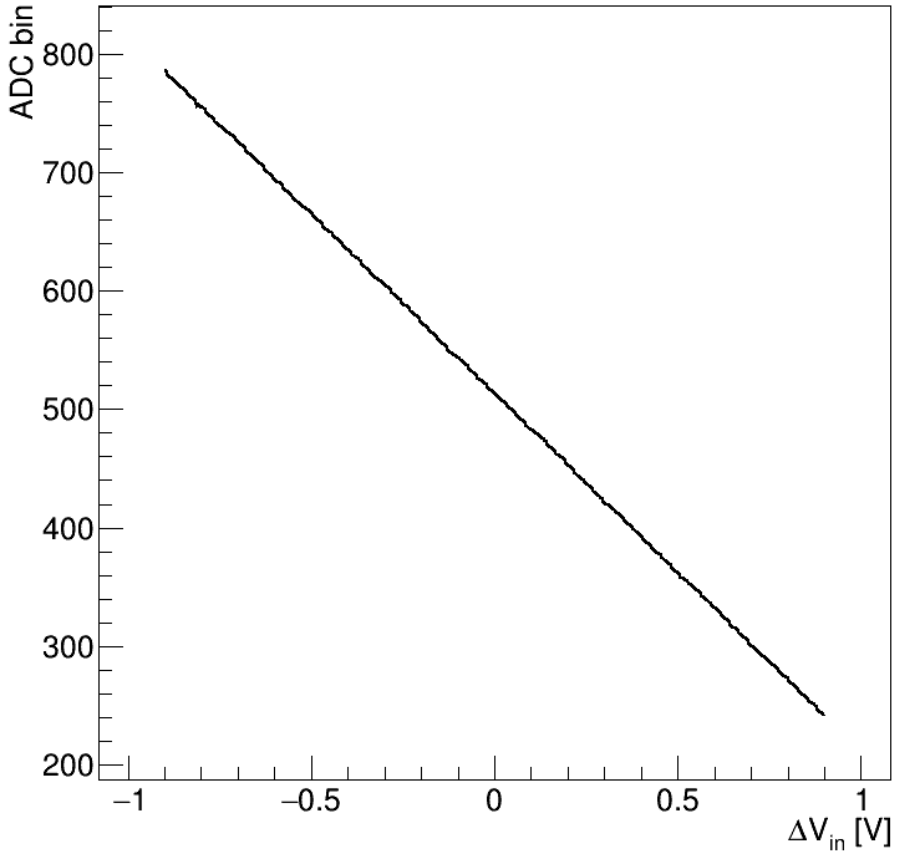
ADC ramp & sine scan for 10bit SAR ADC

sampling rate: 2 MHz, sine frequency: 10kHz

at the end : only the DC voltage is of importance in the system,

peak voltage of the signal processing unit in advance

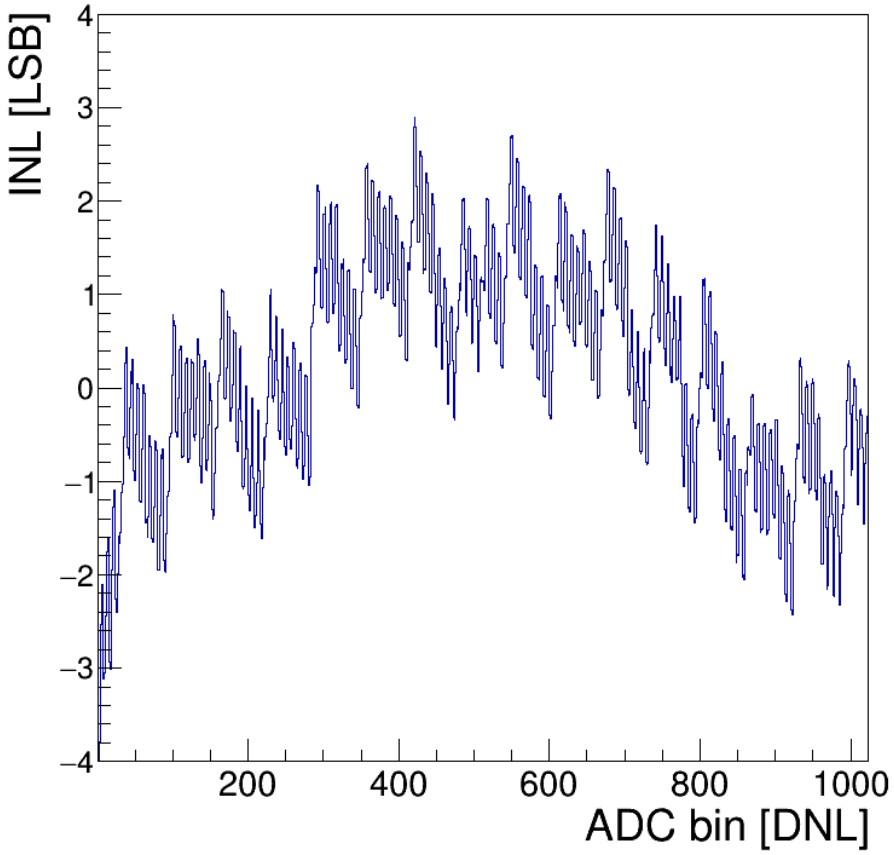


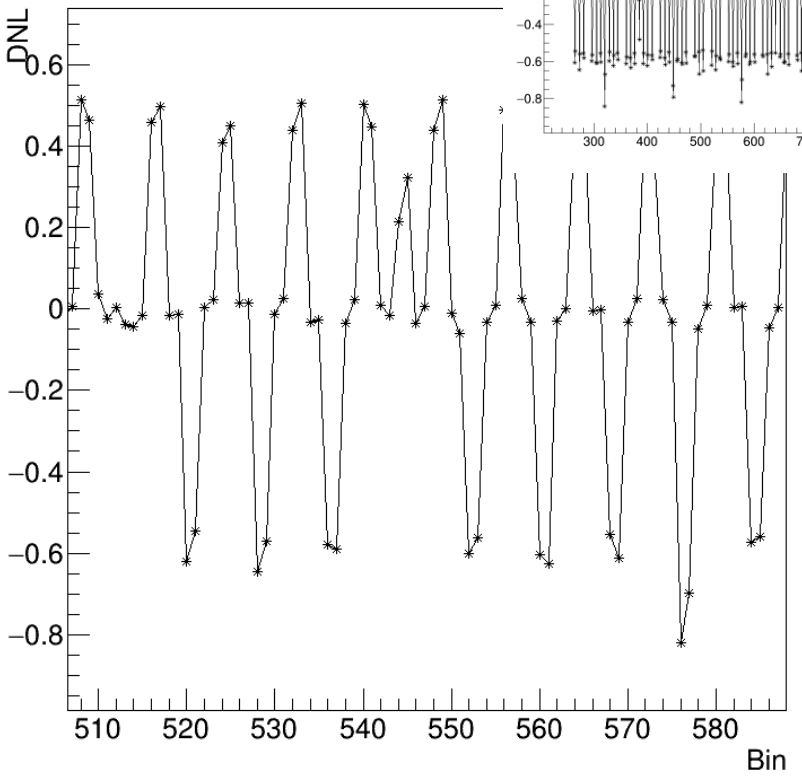


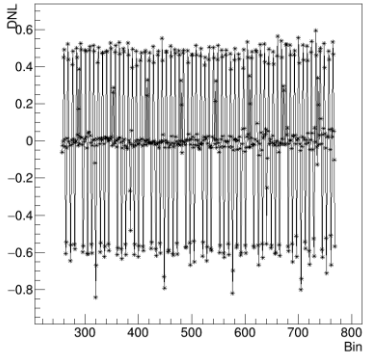
DNL and INL

- DNL and INL through code density test:

  regular +/- 0.5LSB DNL pattern

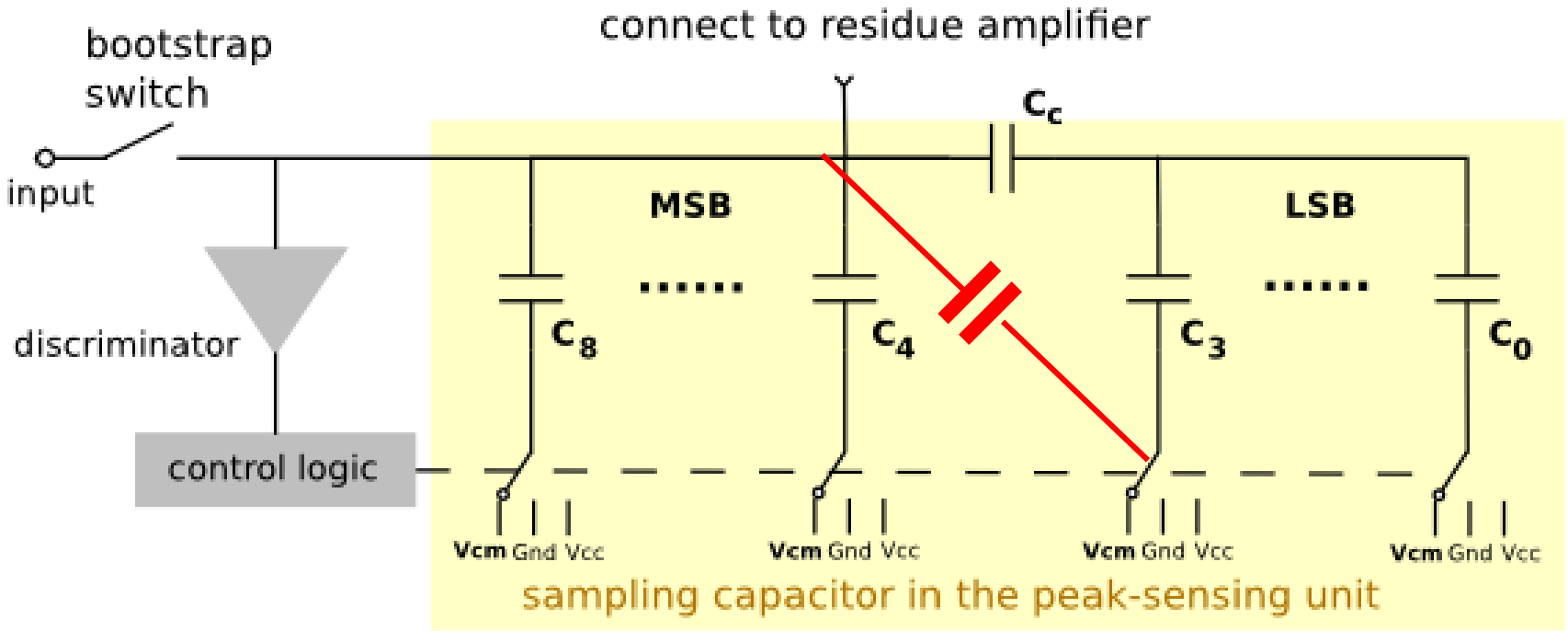






Layout problem

Array Parasitics revised



Parasitics *needed* to create this effect ~ 9fF (Unit size ~30fF) → Not found

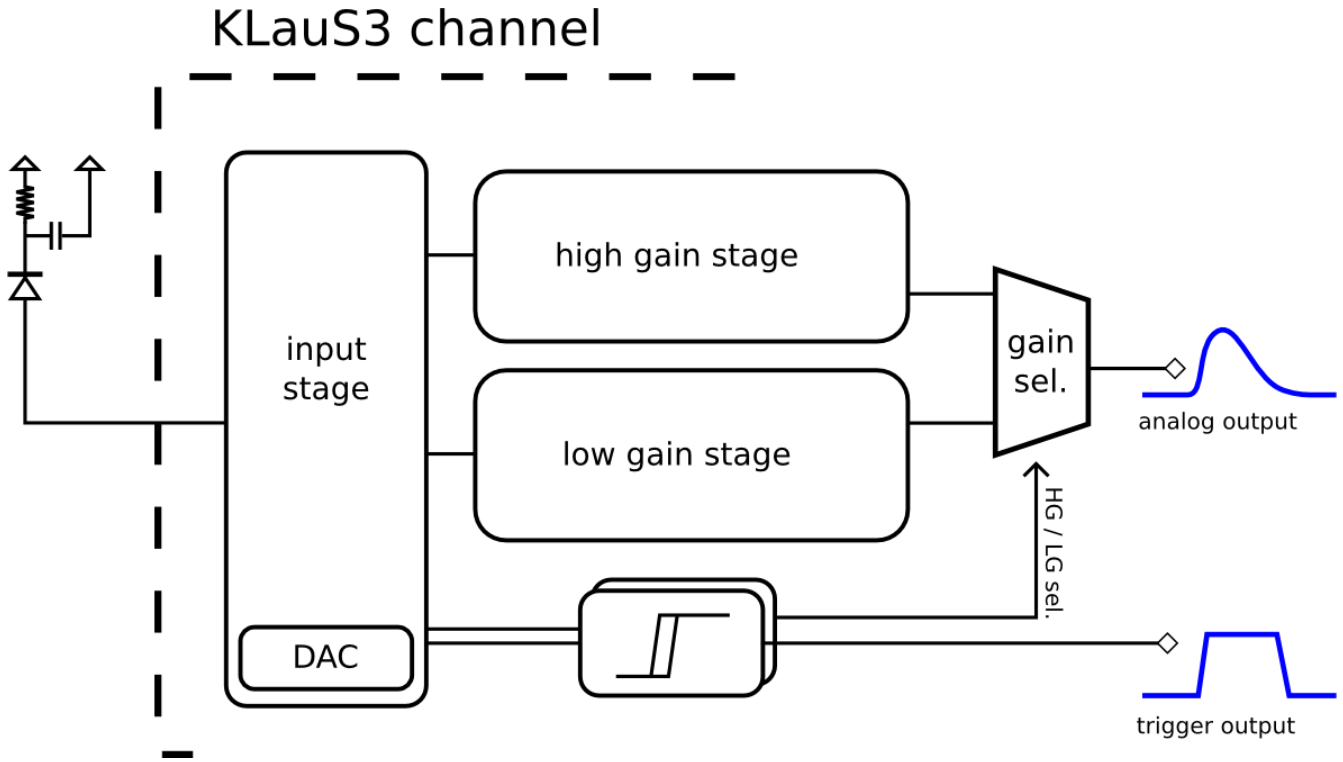
Parasitic *causing* the effect: 600aF between C1 switch line and MSB array

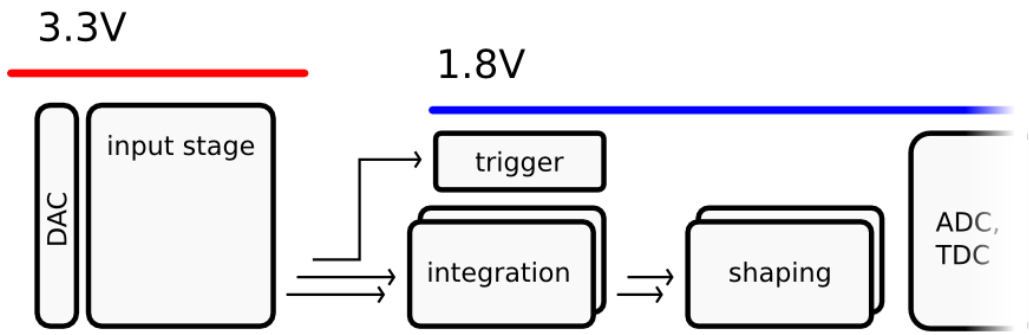
New layout version

more protection to reduce the parasitic capacitance

DNL0 *** LSB	1.819m
DNL1	-5.377m
DNL2	-9.986m
DNL3	-2.481m
DNL4	41.89m
DNL5	35.88m
DNL6	5.154m
DNL7	-26.8m
DNL8	16.65m

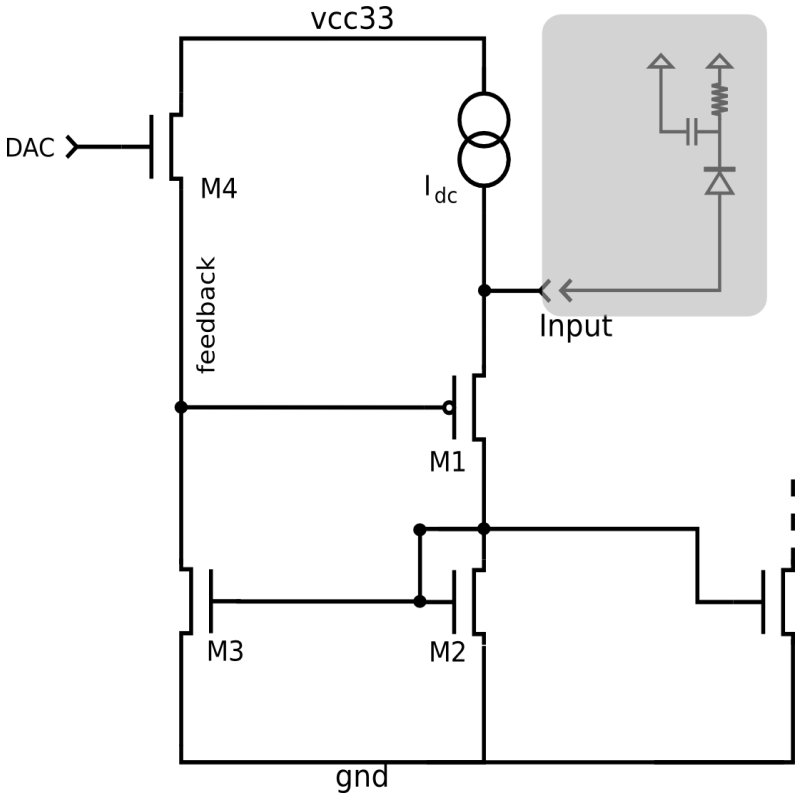
Reminder of the analog frontend

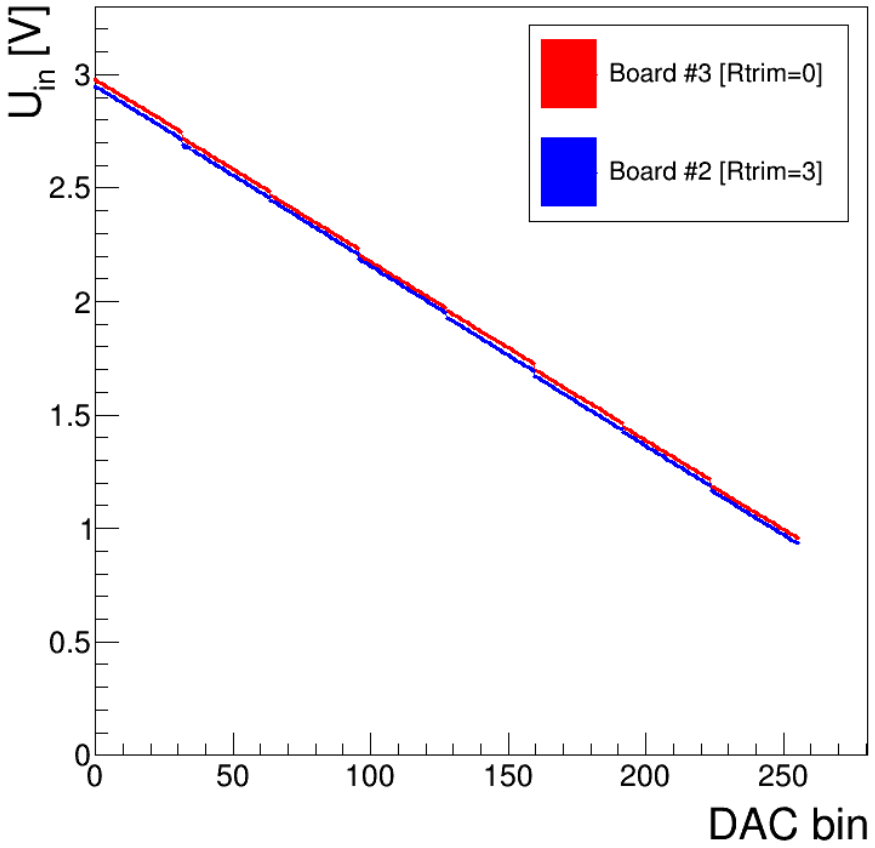




Preliminary frontend measurement

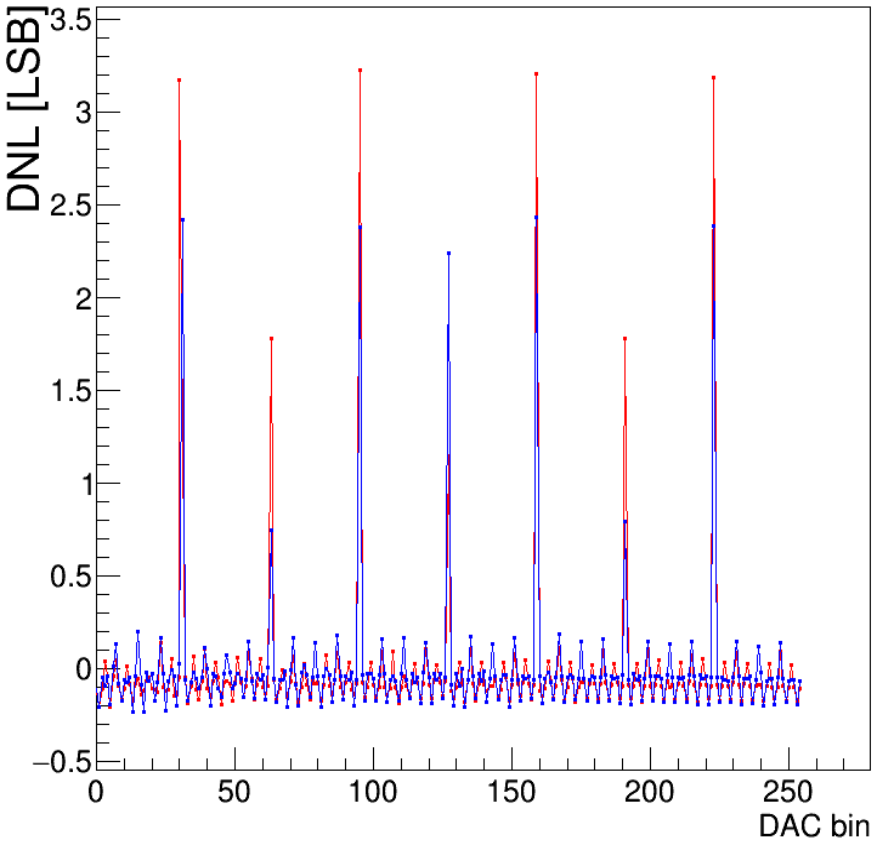
- DAC scan for the input bias, range of 2V at least

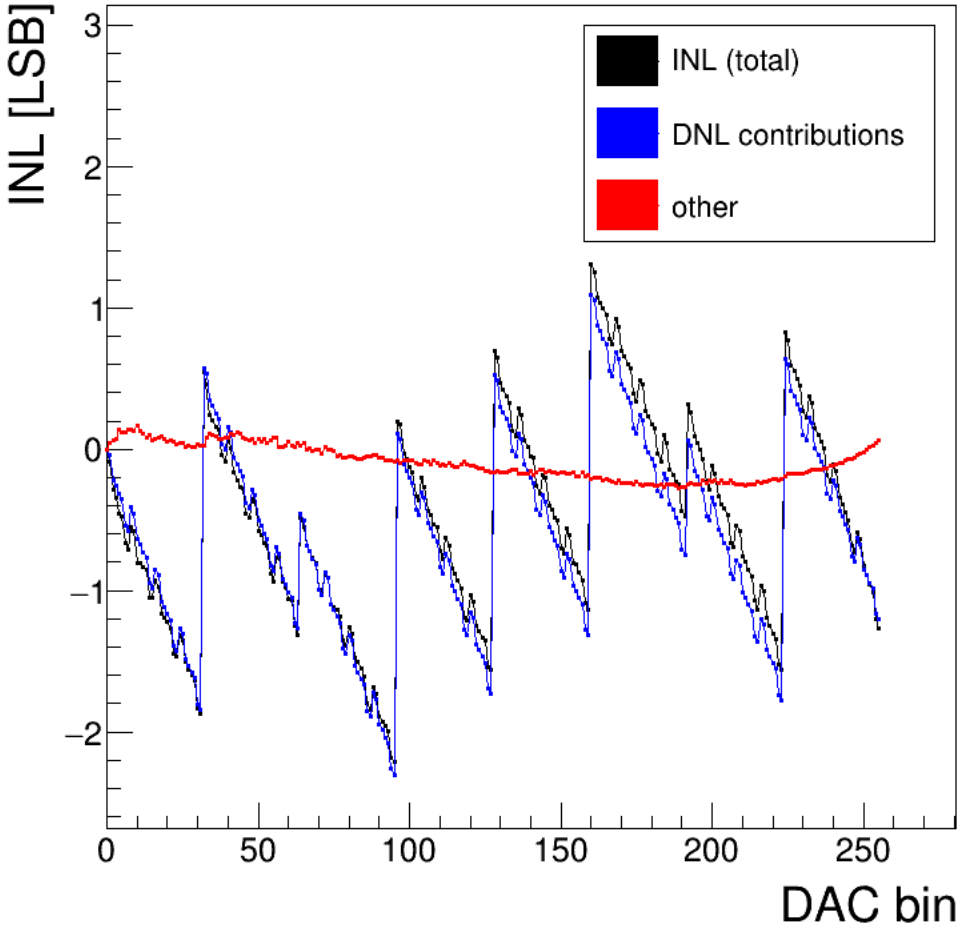




DNL , INL analysis for the input DAC

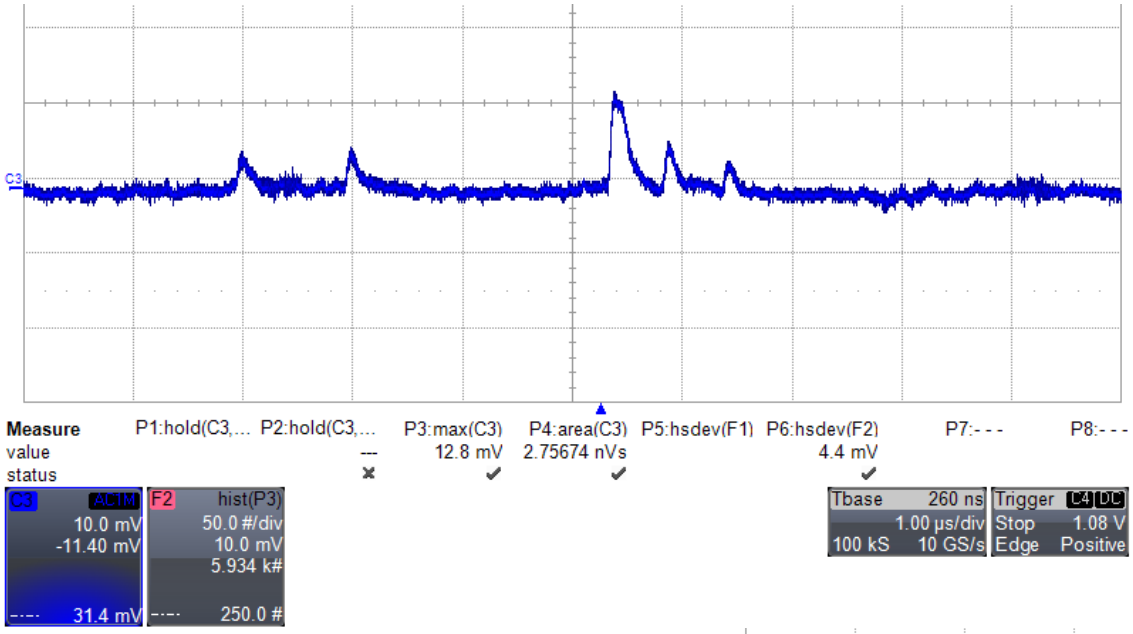
Different error sources are identified, layout mismatch is the largest

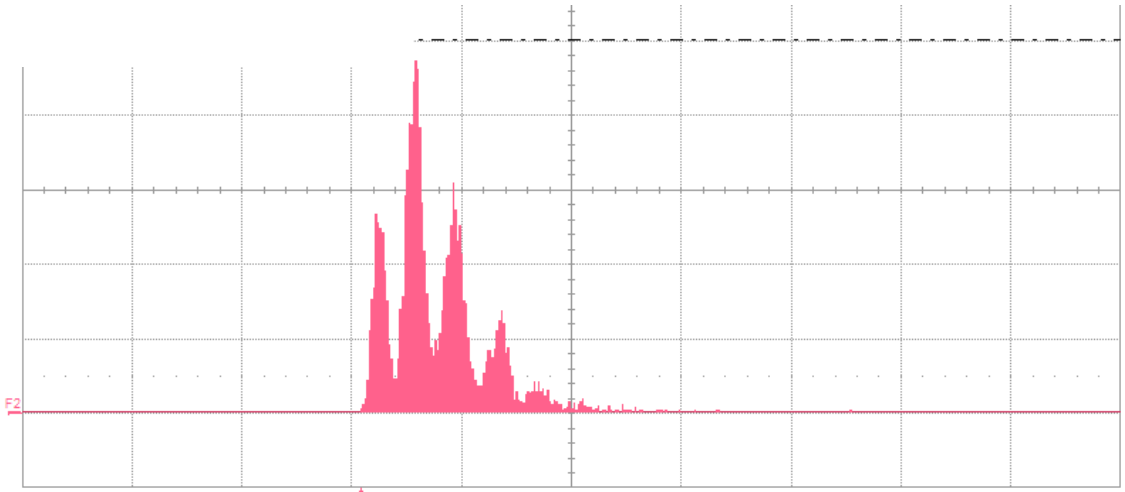




Mesurement with the 0.35u CMOS SiPM chip

nominal HV recommended from Hamamatsu
Gain = 1.35e5, shaping name = 25ns





Summary

- the miniASIC from March is working and under test
- preliminary results has been obtained since July
- ADC working, DNL & INL measured
- 0.5LSB error found due to layout issue, will be corrected in Nov 2015
- Analog frontend also functioning, input DAC scan performed DNL & INL analysed.
- frondend structure validated again for MPPC 10um pitch device