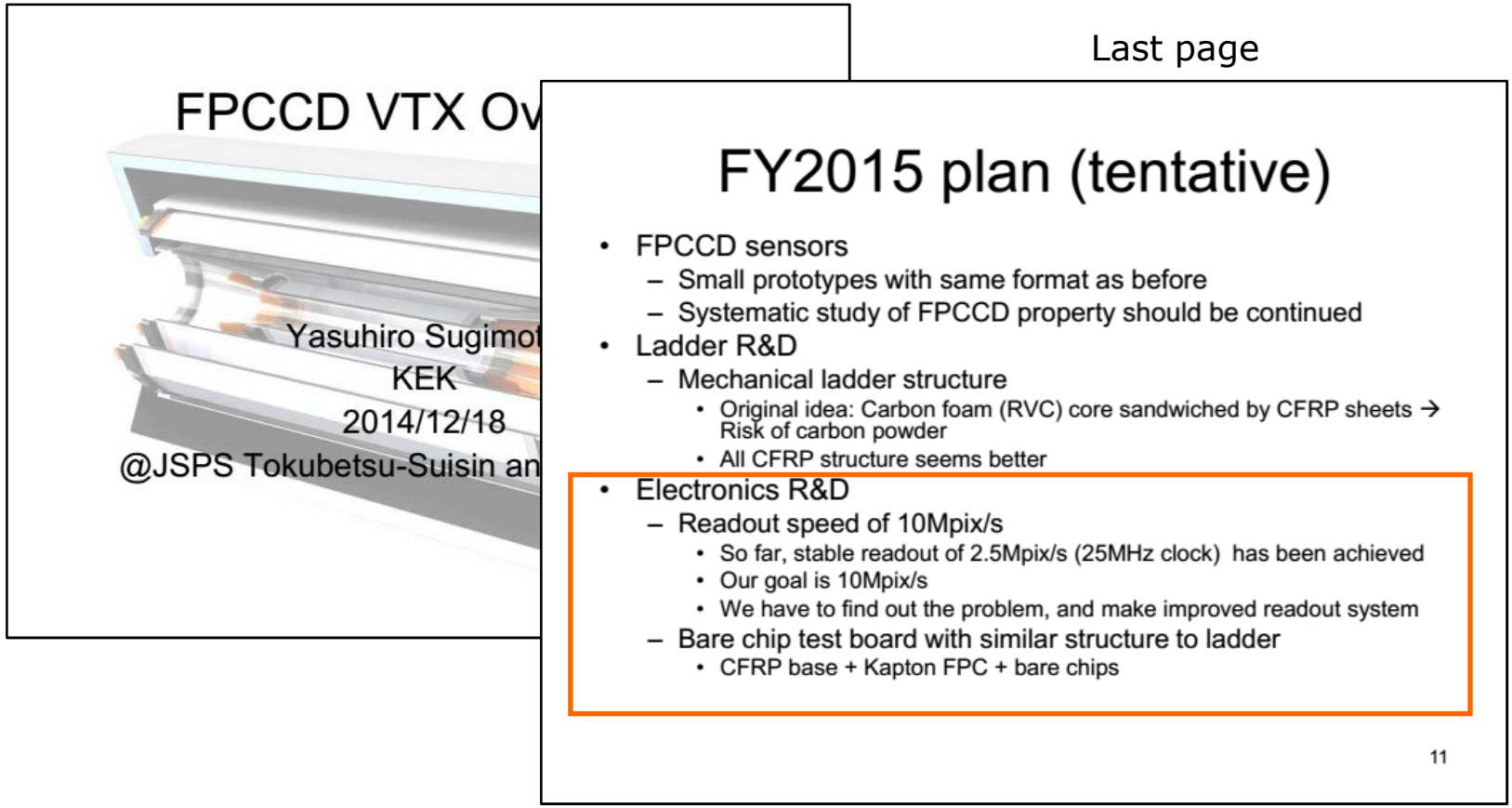
FPCCD READOUT ELECTRONICS progress in 2015

2015/12/8　Hisao SATO　(Shinshu-univ.)

@JSPS Tokubetsu-Suisin annual meeting

Preface

In the Tokubetsu-Suisin Annual Meeting 2014 Sugimoto san presented "FPCCD VTX Overview".



Contents

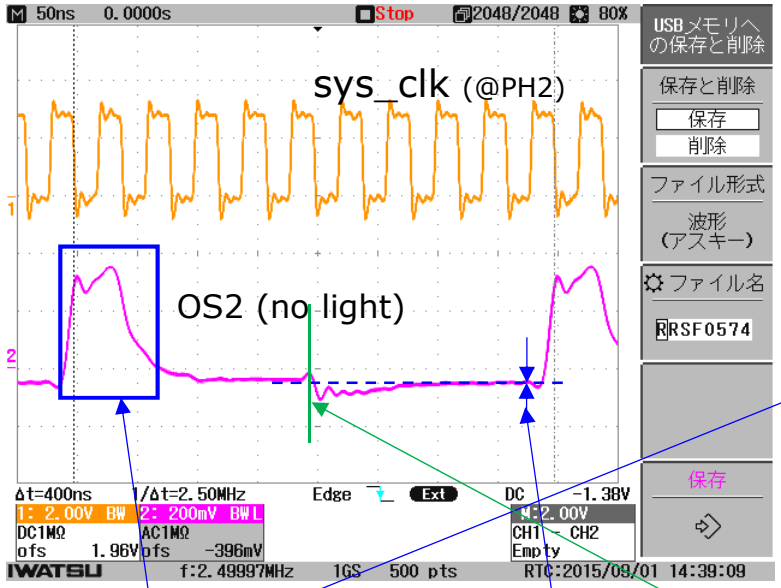
1. FPCCD readout speed of 10Mpix/s

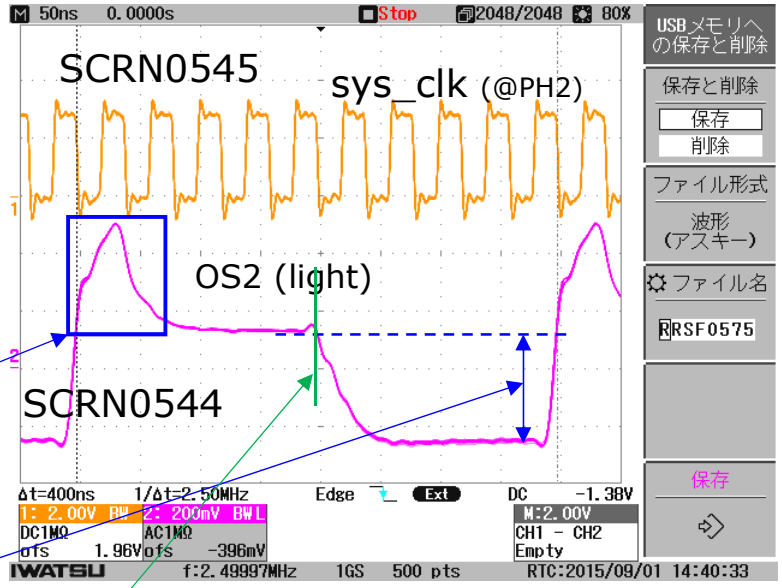
1.1 Requirements and current status

- In the FPCCD Vertex detector all pixel data have to be read in interval of train, 199msec. This corresponds to 100nsec/pixel, that is 10Mpix/s.
- In ASIC stand alone test, it was tested up to 12.5Mpix/s.
- In FPCCD test, that is FPCCD + ASIC test, speed was limited to 2.5Mpix/s. Then 0.6Mpix/s and 2.5Mpix/s have been conditions used so far.

1.2 CCD output waveform

Oscilloscope screenshots of FPCCD OS2 output at 2.5Mpix/sec with/without light





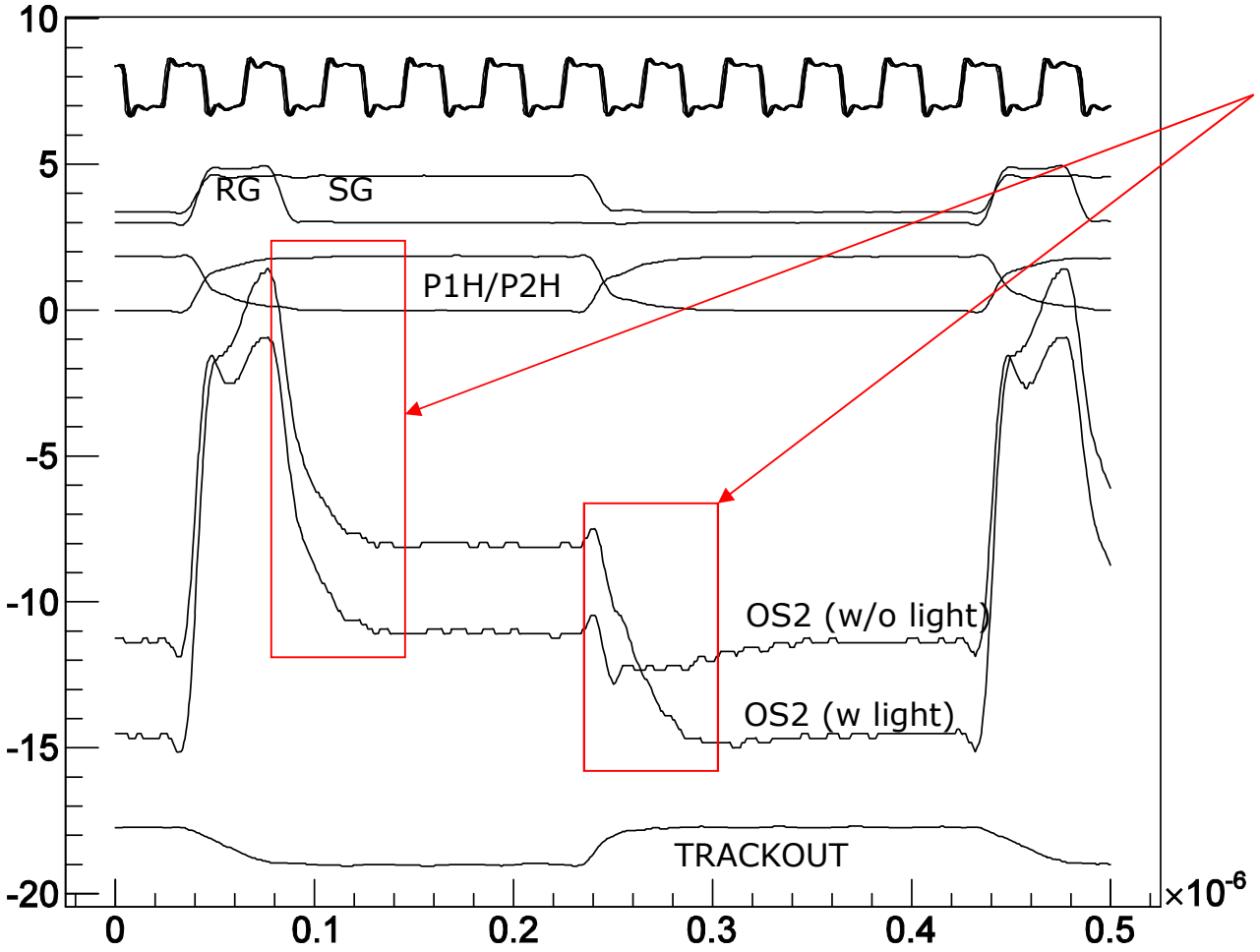
Reset feedthrough : Response to reset clock RG

signal

clock SG falling edge

1.2 CCD output waveform

2.5Mpix/s



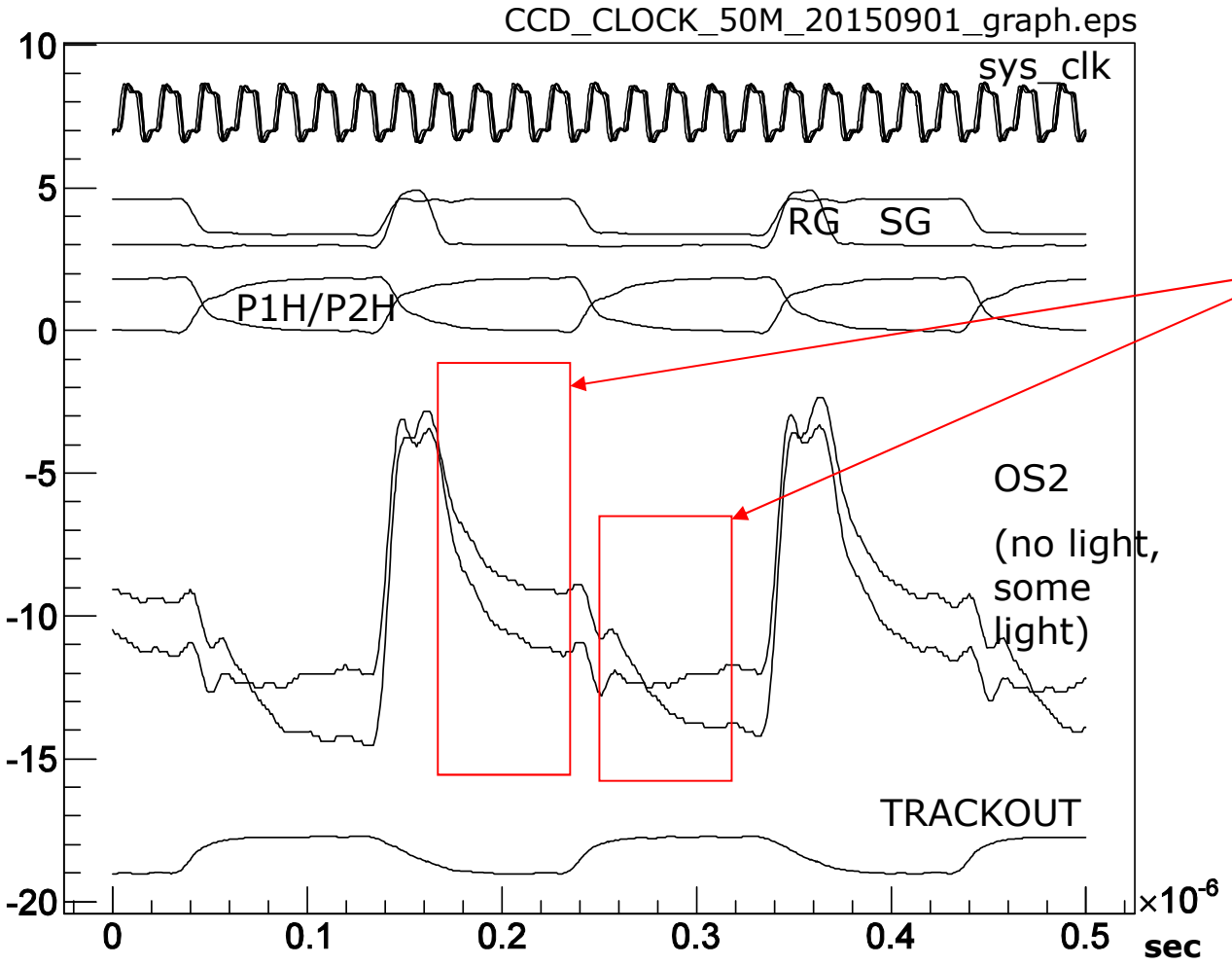
This decay time OK for 2.5M, but too long for 5M and 10Mpix/s.

Note) vertical axis is arbitrary

FPGA config.: uflD25MPLL50M_4CCDCLK_20150727.bit

1.2 CCD output waveform

5Mpix/s



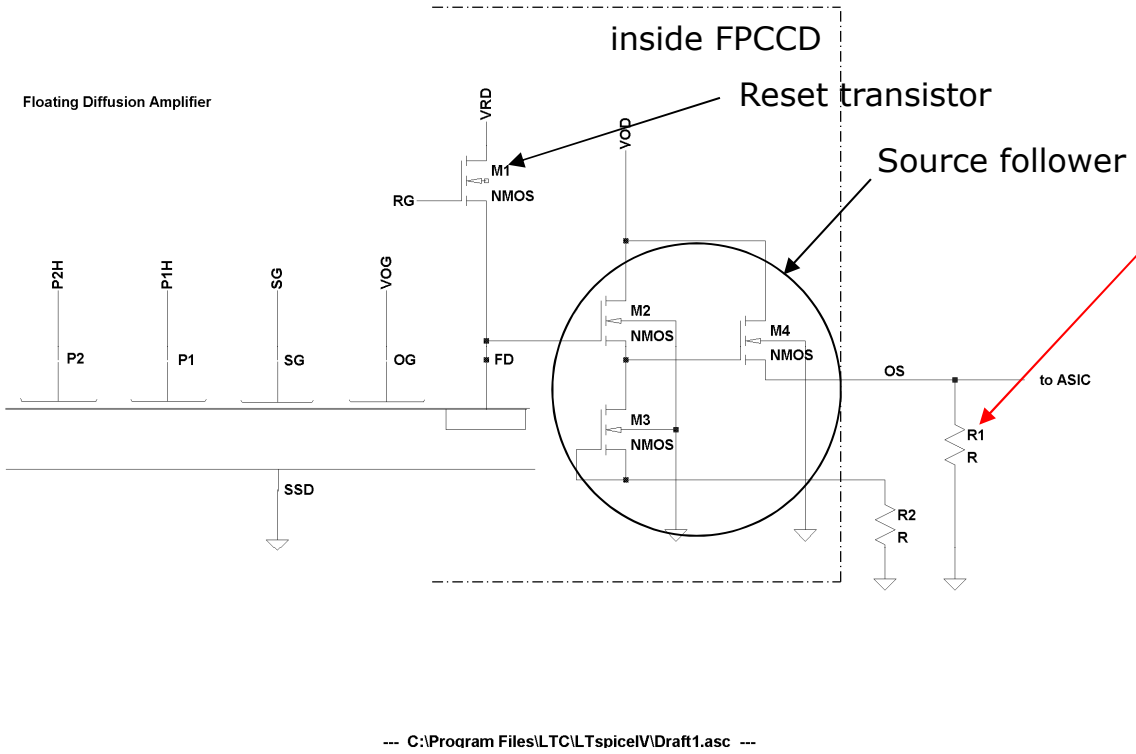
This decay time is too long for 5M and 10Mpix/s

Note) vertical axis is arbitrary

FPGA config.:uflD50MPLL50M_4CCDCLK_20150819.bit

1.2 CCD output waveform

OS circuits inside and outside of FPCCD

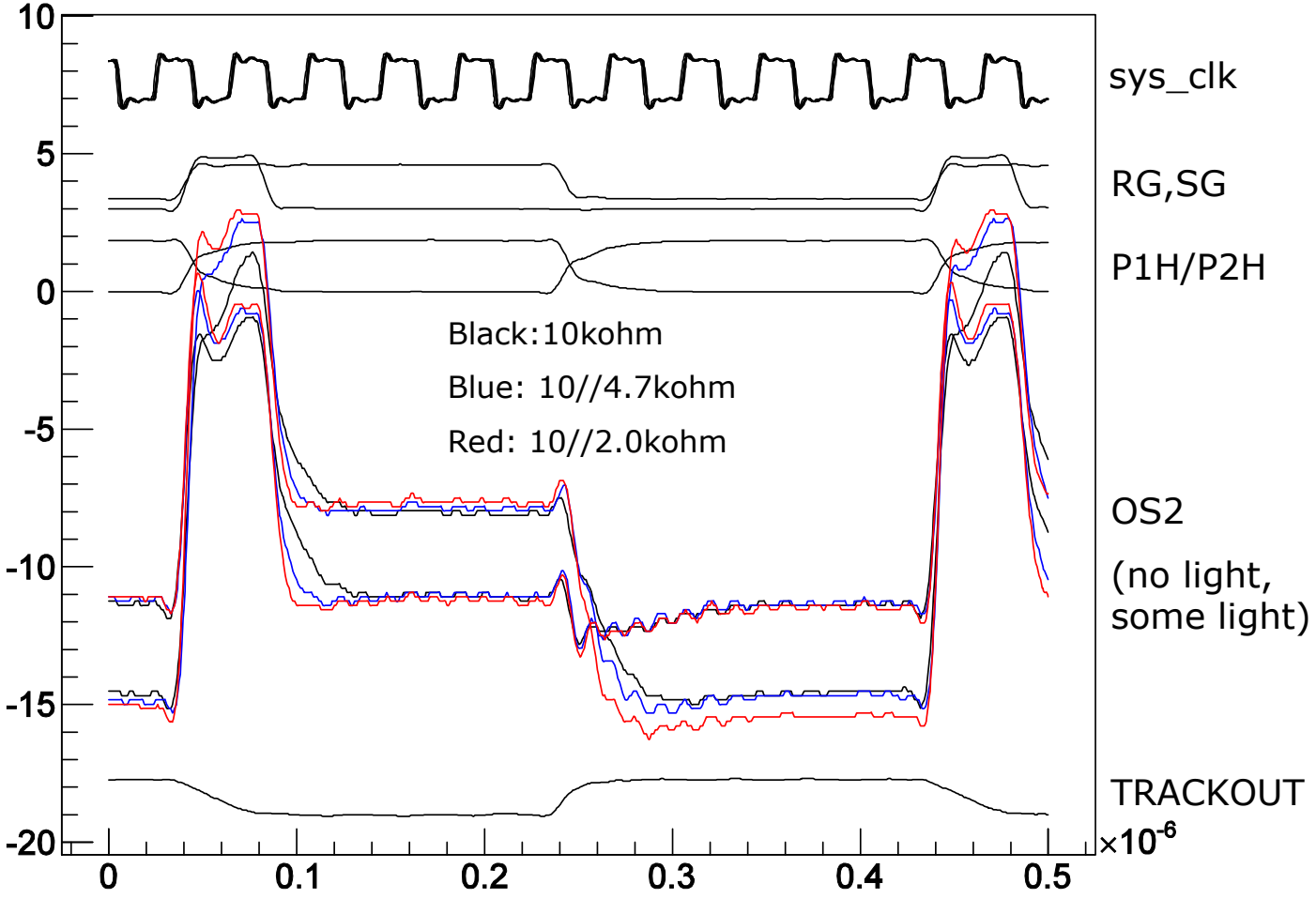


OS pull down resistors, 10kohm, determine bias current of M4.

Lower resistor increases the bias current and improves response speed of the source follower.

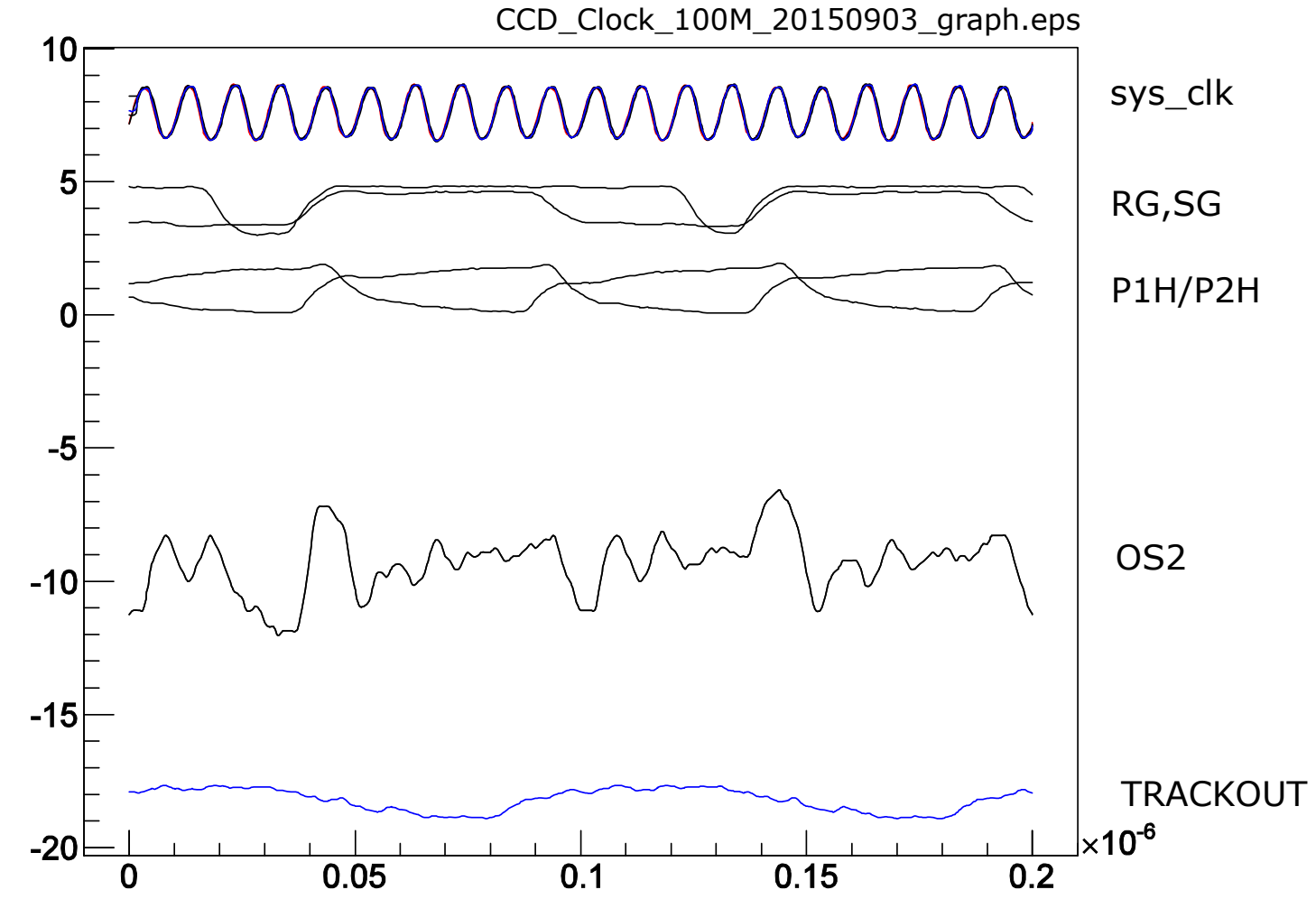
1.2 CCD output waveform

2.5Mpix/s, FPCCD output waveforms of 3 kinds of R1 resistor



1.2 CCD output waveform

10Mpix/s, ch7, FPCCD output waveforms of R1 resistor 10k//2kohm



FPGA config: uflD100MPLL100M_4CCDCLK_20150903.bit

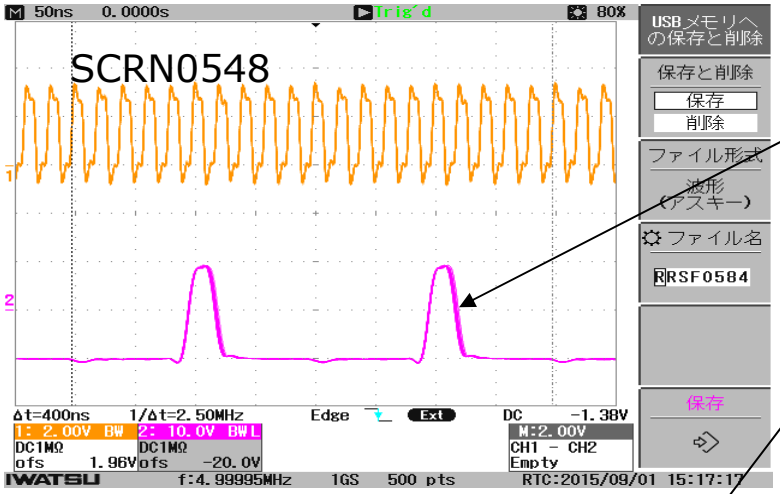
1.2 CCD output waveform

Section summery : 1st problem and measure

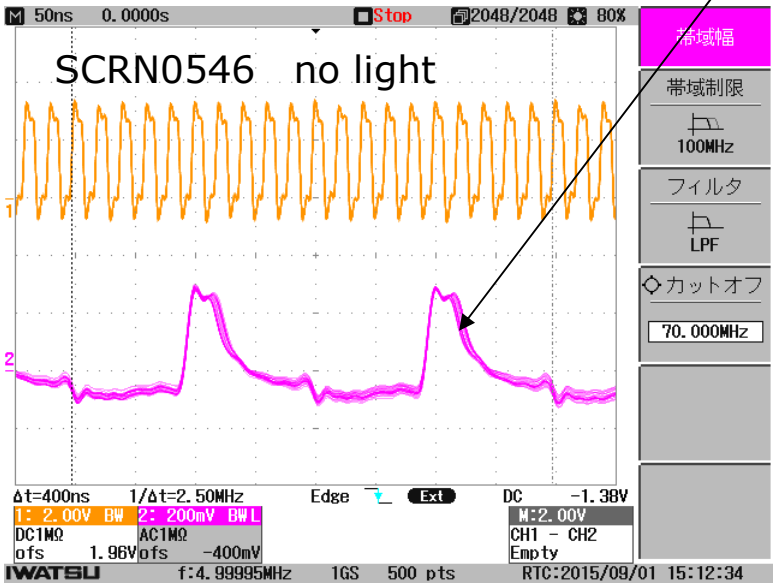
- 10kohm pull-down resistor makes output response slow, and works below 2.5Mpix/s.
- 2kohm or less pull-down resistor makes waveform good for 5M and 10Mpix/s.
- OS voltage = about 6V.
  10kohm → Pw = 3.6mW,
  2kohm → Pw = 18mW, exceeds Pw/ch budget (10mW)
- Temporally solution : 2kohm
- Require a permanent solution : Pw<3mW
- Even if R1 is 2kohm, scatter plot is not good, yet. There are other problems.

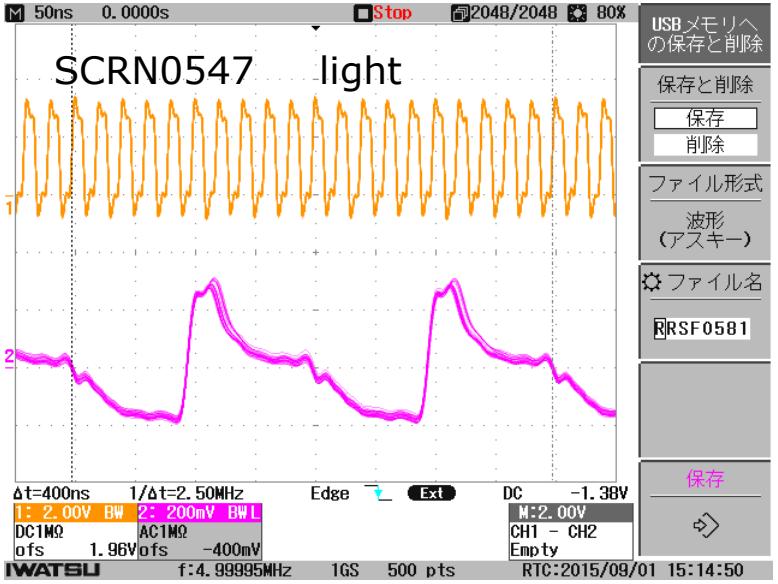
1.3 RG waveform

5Mpix/s, dispersion of RG and OS



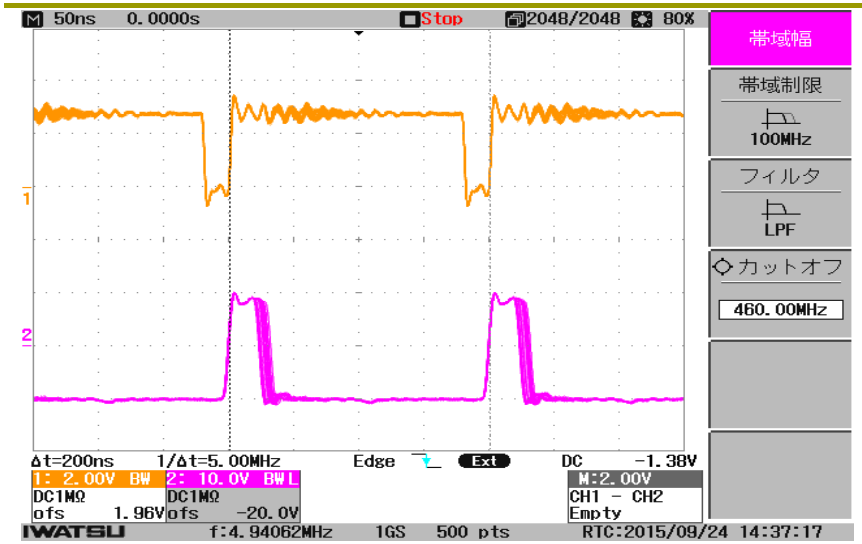
Dispersion of falling edge is observed. This probablly causes dispersion of OS signal. (bottom pictures)





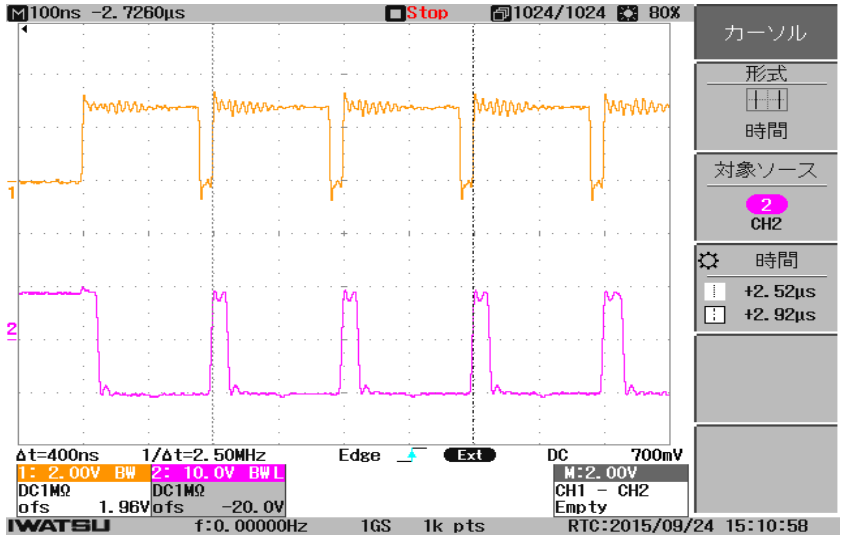
1.3 RG waveform

5Mpix/s, dispersion of RG falling edge



SCRN0566
ch1(orange): RG(@PH3) driver card input
ch2(violet):RG(@CCDpin)

RG pulse width is as short as driver card delay. RG falling edge is determined not only rising edge timing but some internal parameters.

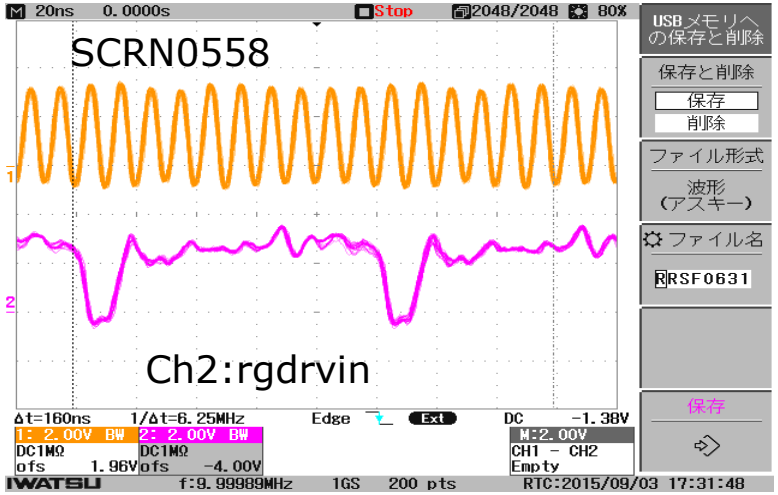


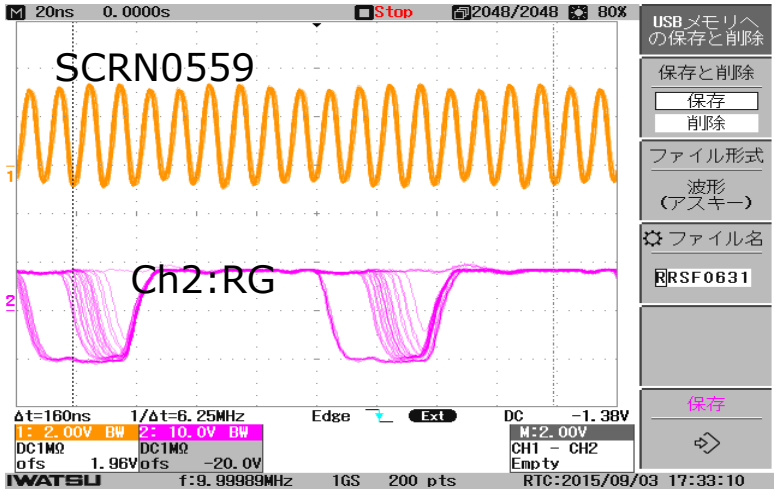
SCRN0567 at beginning of a frame
ch1(orange): RG(@PH3) driver card input
ch2(violet): RG(@CCDpin)

In this case RG falling edge is slow or fast randomly.

1.3 RG waveform

10Mpix/s, RG clock driver card input (rgdrvin) and output (RG)





Driver input (rgdrvin) is good, but driver output (RG) is totally wrong.

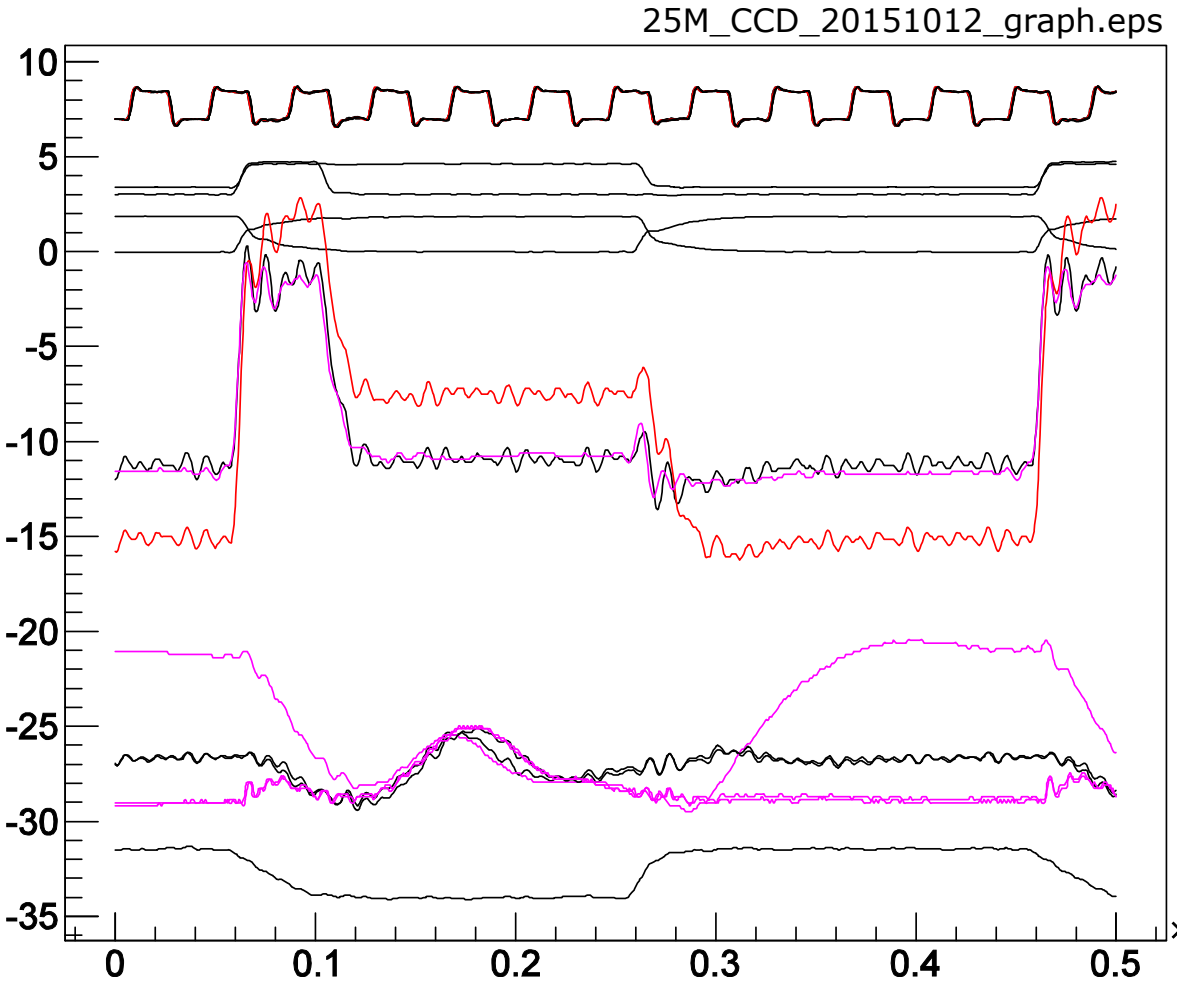
1.3 RG waveform

Section summery :2nd problem and measure

- Current CCD clock driver card generates 5Mpix/s RG clock which falling edge has dispersion. And it can not generate 10Mpix/s RG clock.
- Double width RG eliminates falling edge dispersion. This can be solution only for 5Mpix/s case.
- Origin of the problem is in EL7156, a driver IC used in the driver card.
- For 10Mpix/s operation a new clock driver is required.
- We are making an alternative RG driver using discrete parts which are easily available.

1.4 ASIC response to CCD reset feedthrough

Monitor AOUT/AHOLD in 2.5Mpix/s operation



sys_clk

SG, RG

P1H/P2H

OS2 (ch7)
black: no light
red light-in
violet light-in

AOUT (ch7)
black: no light
violet light-in

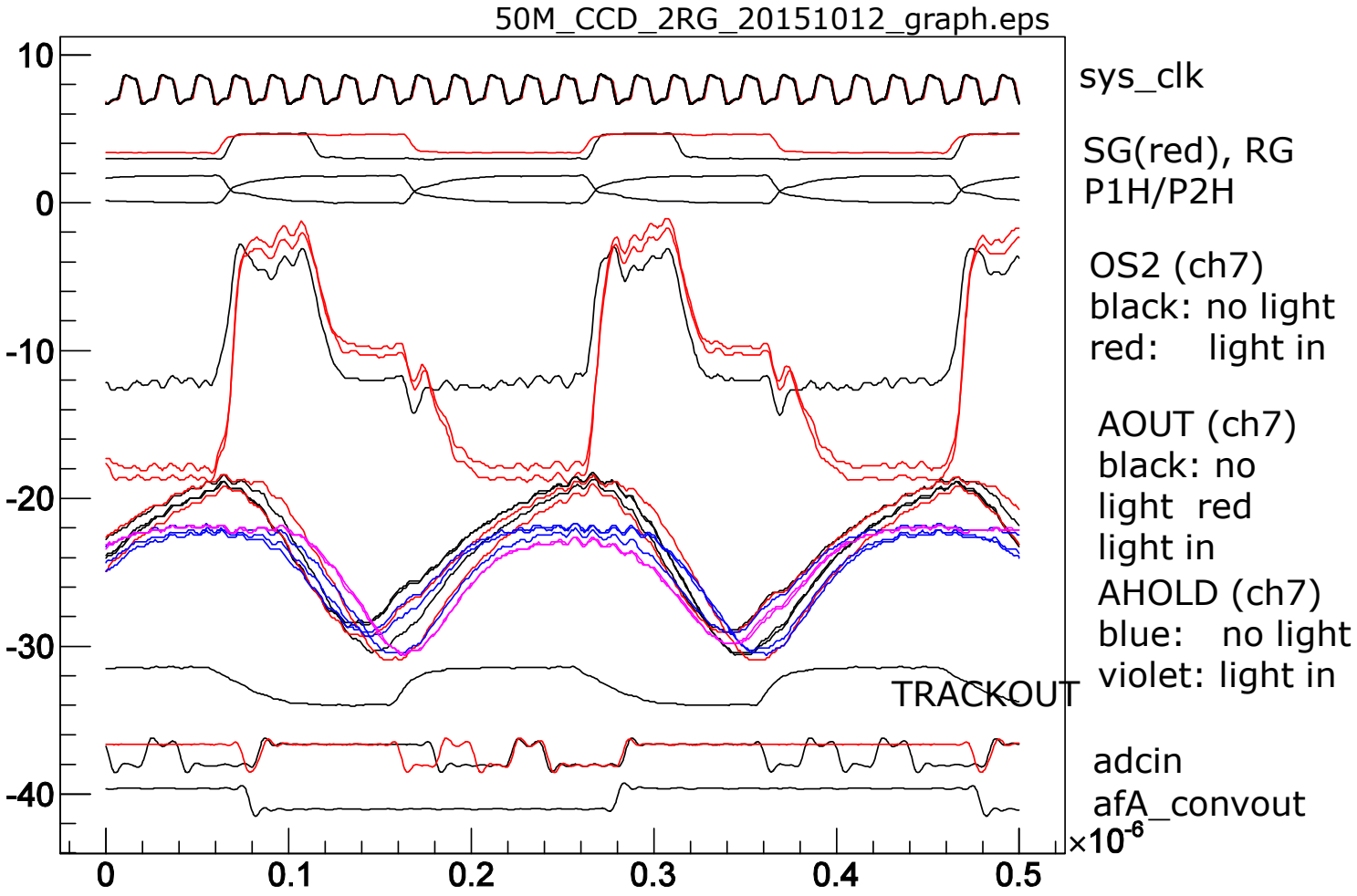
AHOLD (ch7)
black: no light
violet light-in

TRACKOUT

AOUT,AHOLD shows reasonable waveforms.

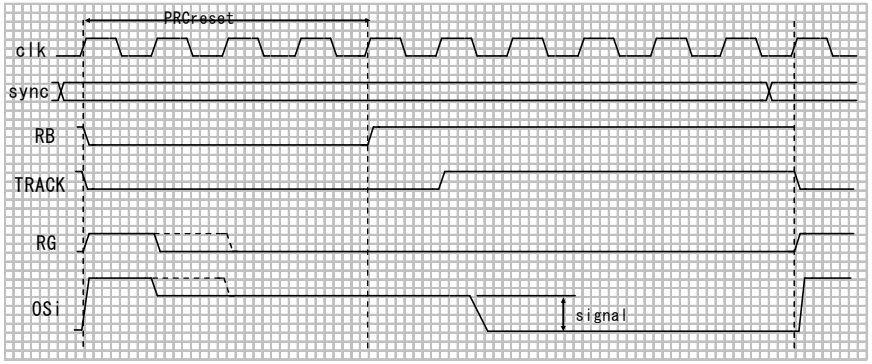
1.4 ASIC response to CCD reset feedthrough

Monitor AOUT/AHOLD in 5Mpix/s operation

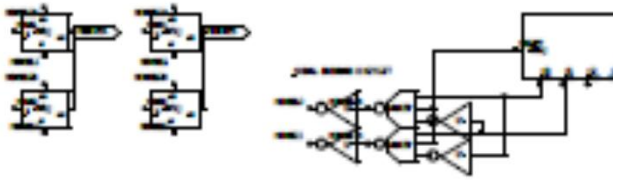


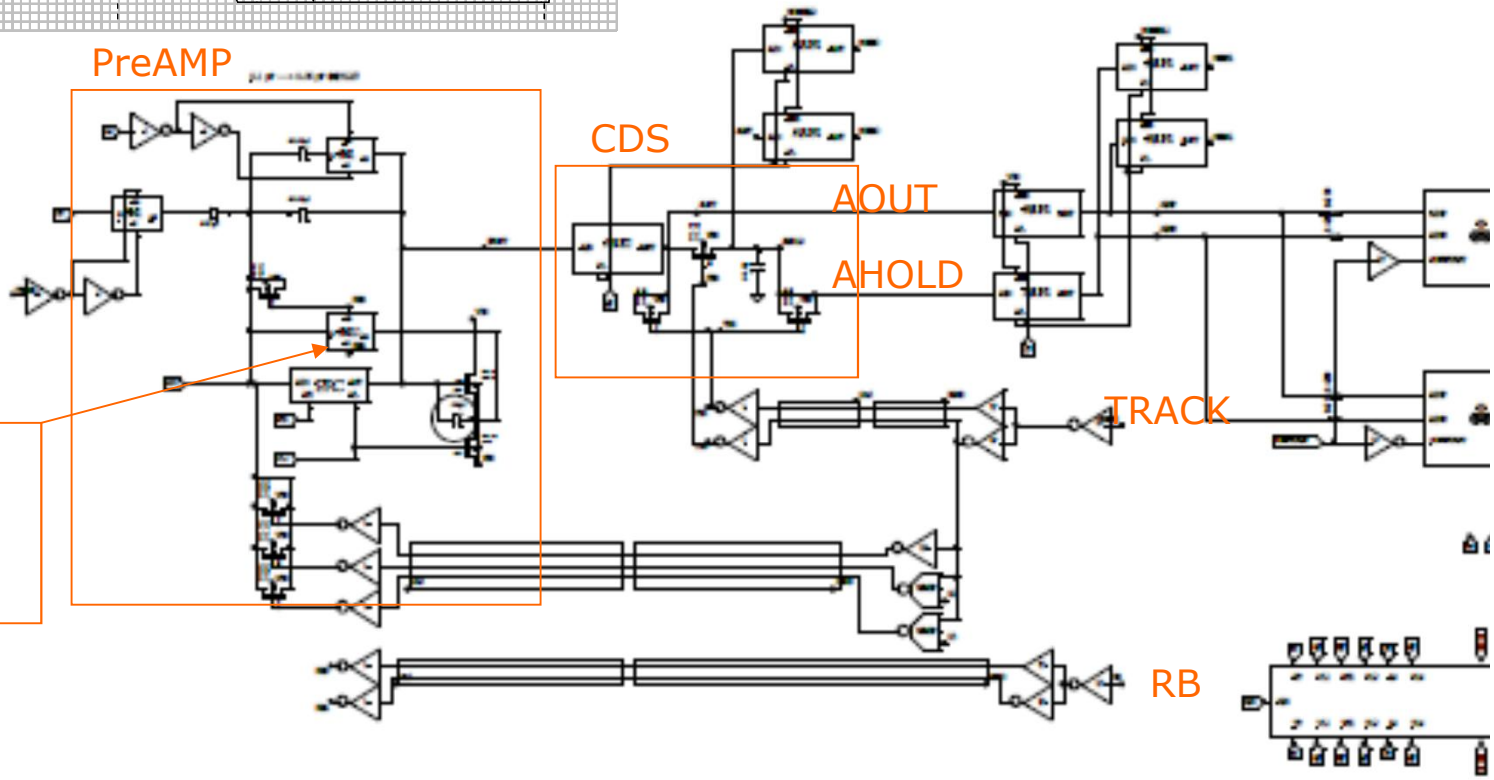
1.4 ASIC response to CCD reset feedthrough

PreAMP and CDS circuit structure and AOUT/AHOLD



Affroc CHAIN1B circuit schematic

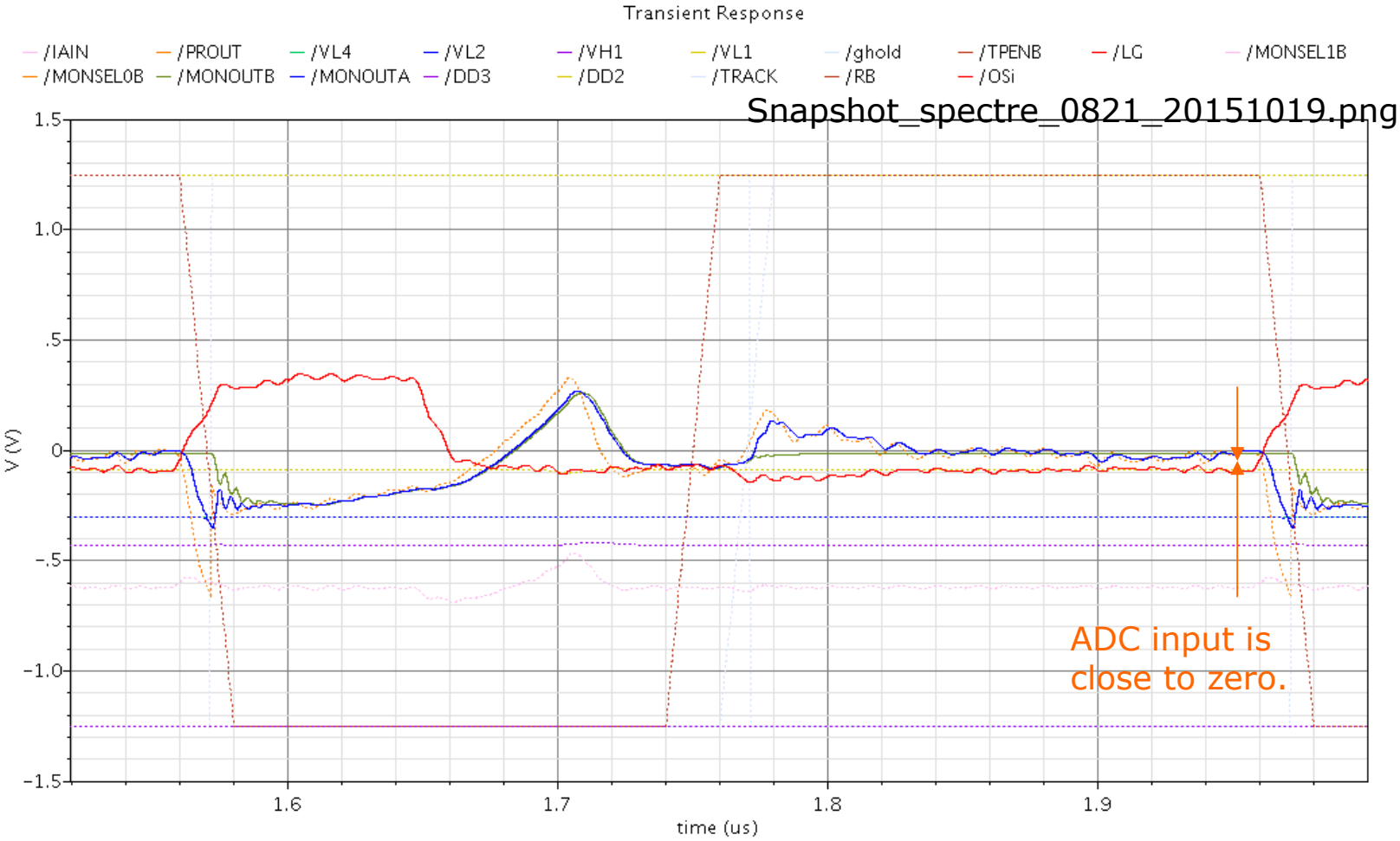




This SW is closed, when RB=0 (PRC in reset phase)

1.4 ASIC response to CCD reset feedthrough

Simulation : 2.5Mpix/sec ch7 no light

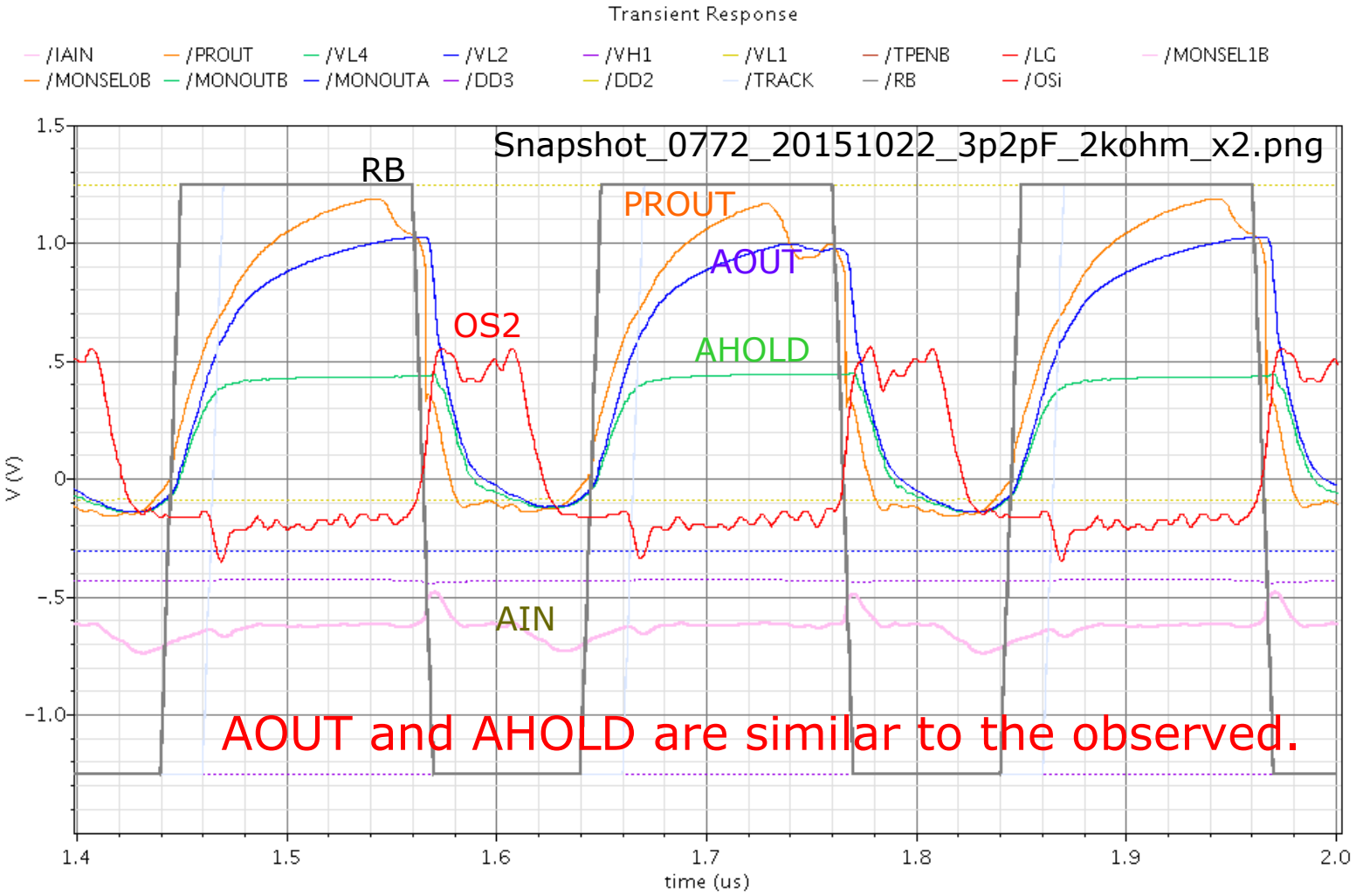


Snapshot_spectre_0821_20151019.png

ADC input is close to zero.

1.4 ASIC response to CCD reset feedthrough

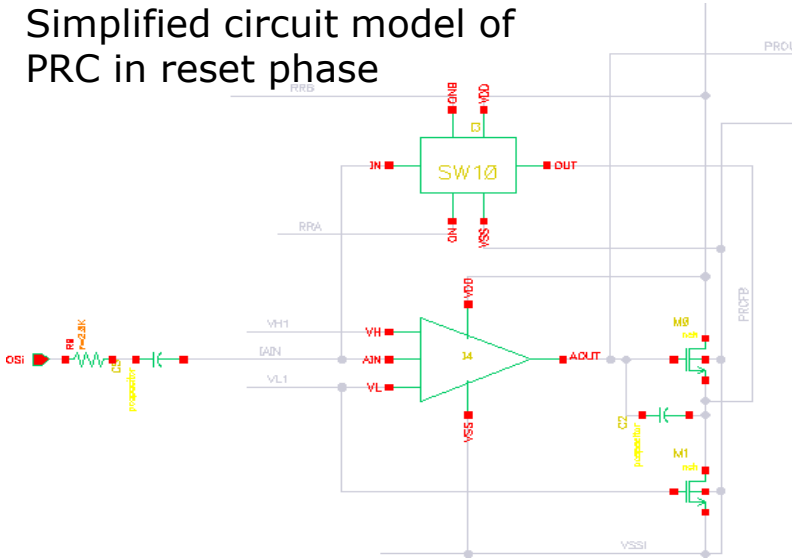
Simulation : 5Mpix/sec ch7 no light

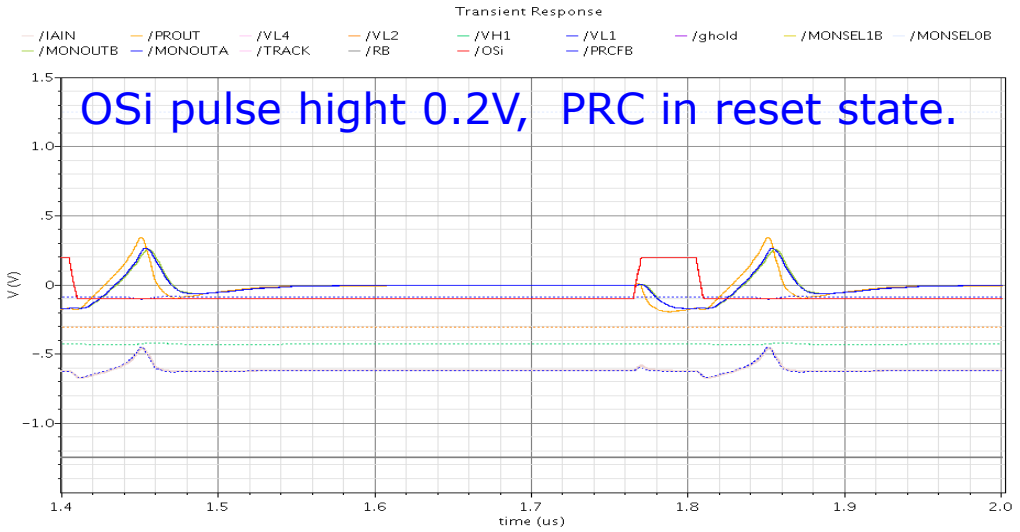


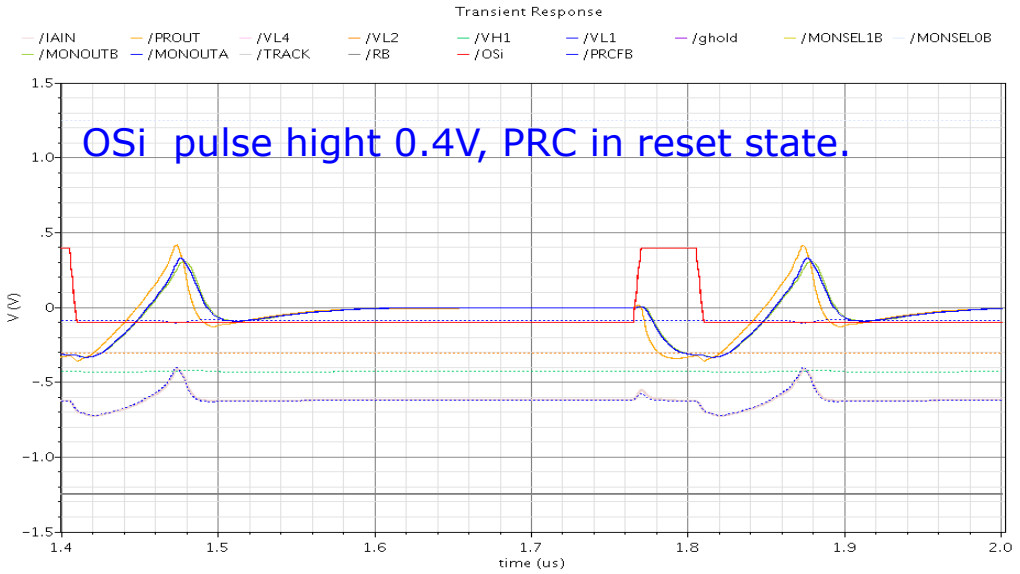
1.4 ASIC response to CCD reset feedthrough

Simulation of PRC in reset phase reproduces reset feedthrough response.

Simplified circuit model of PRC in reset phase







Simulation reproduces AOUT/AHOLD response to CCD reset feedthrough.

PRC is driven by a large reset feedthrough into a state, that does not work as amplifier, and takes time to return to normal bias point.

1.4 ASIC response to CCD reset feedthrough

Section summery, and comments on measure

1) CCD reset feed through pulse drives PRC, pre-Amplifier, in reset phase into some state. It takes time for PRC to return to normal bias point.
2) It works properly only below 2.5Mpix/sec.
3) “counter reset pulse” can be a temporally measure to fix the PreAMP behavior problem. Effectiveness of counter reset pulse was verified by simulation in 5Mpix/s cases. It is also verified in 10Mpix/s case with +/- 2nsec timing tolerance.

2. ASIC issues

1. Expand offset adjust range

2. Linearity of AD Converter

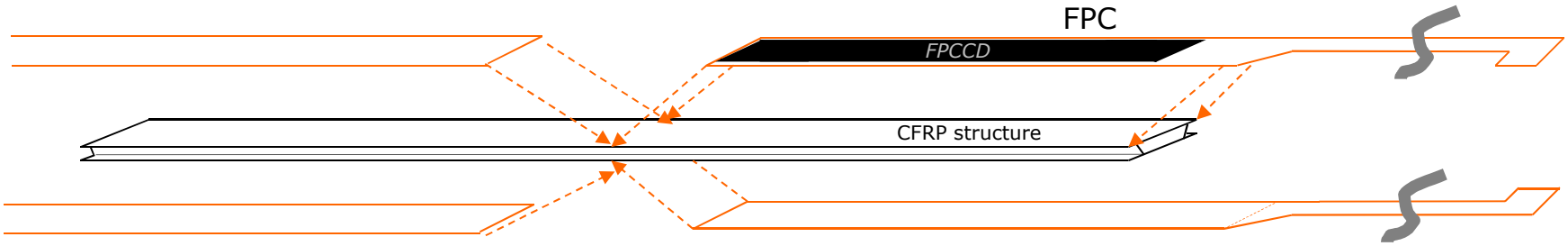
3. PRC reset phase response to CCD feedthrough

Following may or may not require ASIC change
4. Support CCD output source follower bias

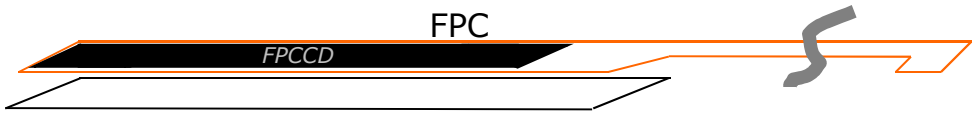
3. Ladder FPC development

Ladder structure and a prototype ladder

Ladder structure:
All ladder circuit components are formed on a flexible film. This is called FPC, Flexible Printed Circuit.
Ladder FPCs are attached to a CFRP structure.



Prototype ladder consists of one FPC attached to a CFRP plate.



3.1 Purpose of ladder design and goal of this year

1. Investigate and optimize electrical characteristics determined by layout pattern.
2. ASIC output LVDS signals : micro-strip-line of which ground plane shared with power lines.
3. CCD clock lines : 30ohm or lower impedance
4. Ladder1b is to be fabricated in this fiscal year, and we start electrical testing.
5. Study issues on mechanical dimension and assembly.
6. Size issues: bonding area of FPCCD that determines dead area
7. Manufacturability
8. In order to do #5~7, all materials will be ready by the end of this fiscal year. 50um thick big dummy chip is also provided.

3.2 Design environment and status

- FPC layout design is key part of work, because layout pattern determines signal integrity of CCD clocks and of fast LVDS signals. We expect inevitable iteration in layout design.
- We use PCB CAD tool “Allegro” for FPC layout design.
- Allegro is licensed by VDEC, VLSI Design and Education Center, which is located in the University of Tokyo, providing CAD software and licenses.
- FPC venders are selected, and we discuss technical details with them in order to finalize the design in this month.

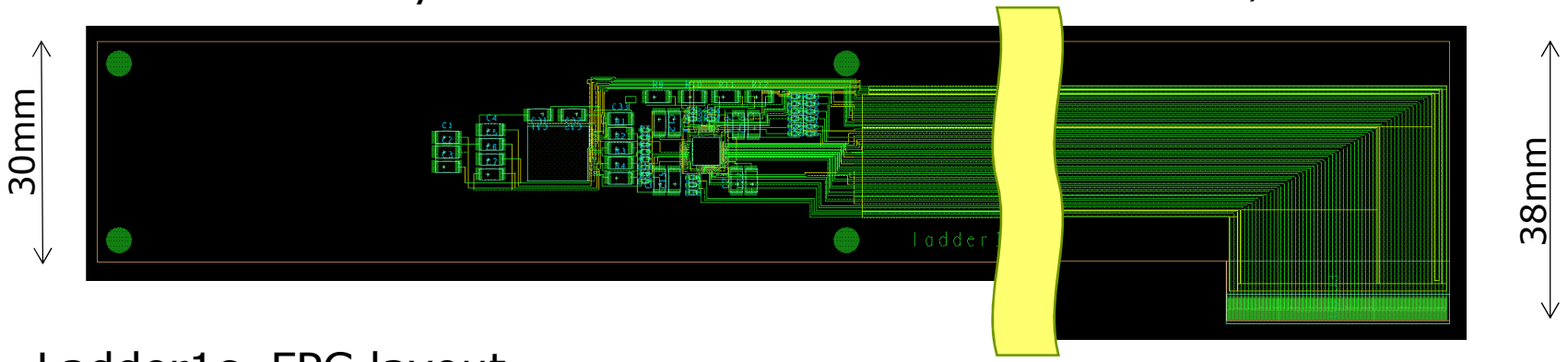
  venders: INGS SHINANO Co., Ltd. (assembly,cordination),

  Yamashita Materials Corporation (FPC)

3.2 Design environment and status

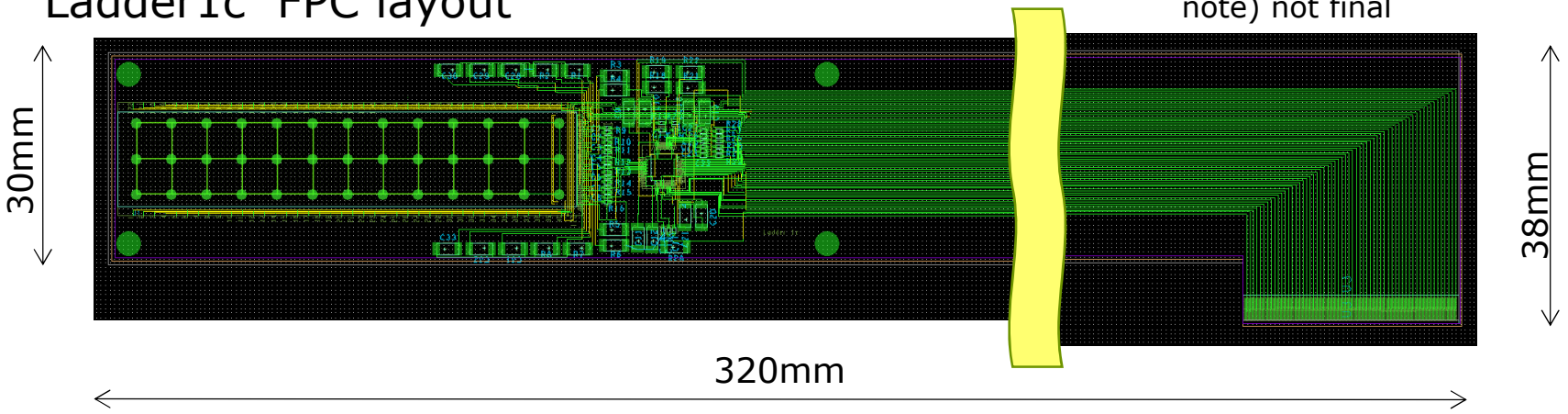
Ladder1b FPC layout

note) not final



Ladder1c FPC layout

note) not final



FPC design is finalizing in this month.

4. Summery

- Three problems preclude FPCCD 10Mpix/s readout.
- FPCCD source follower bias is optimized. Low power dissipation method is required in future.
- RG clock driver problem and measure is reported.
- Third problem is reported. Cause of the problem is becoming clear. ASIC needs to be revised. Temporally measure action is taking.
- 1st Ladder prototype design goal and current status is reported.

Acknowledgement

1. This work is supported by VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

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