

Development Status of Electronics and Cooling for ILC TPC

Takahiro Fusayasu (Saga U.)

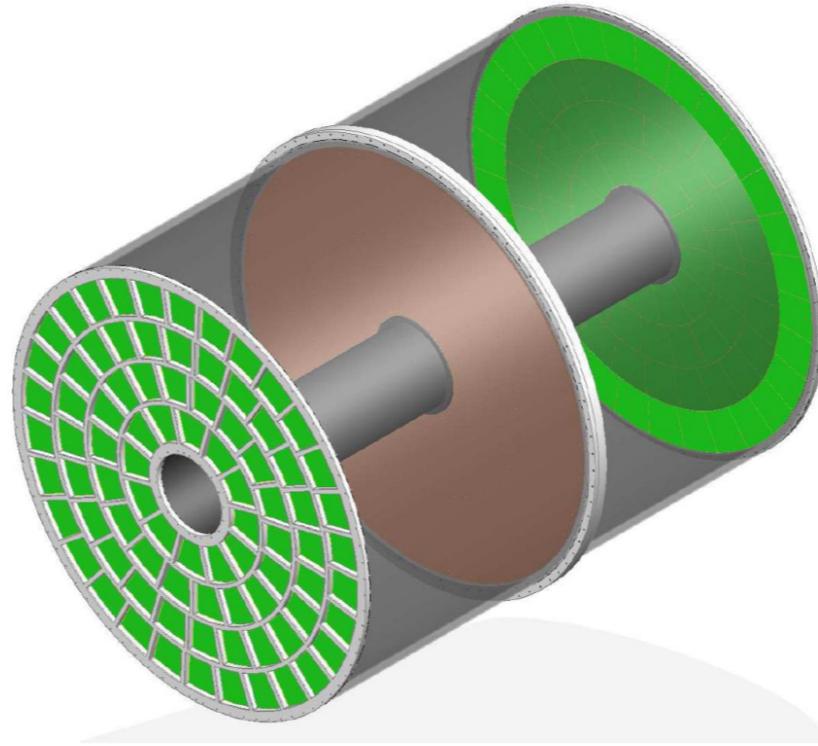
2015.12.9 ILC Tokusui Workshop @ KEK

Outline

1. Introduction
2. Electronics for next pad-readout module
3. Evaluation of TPG (heat-conductive plate)
4. Towards final electronics
5. Summary

1. Introduction

TPC Endplate Requirement

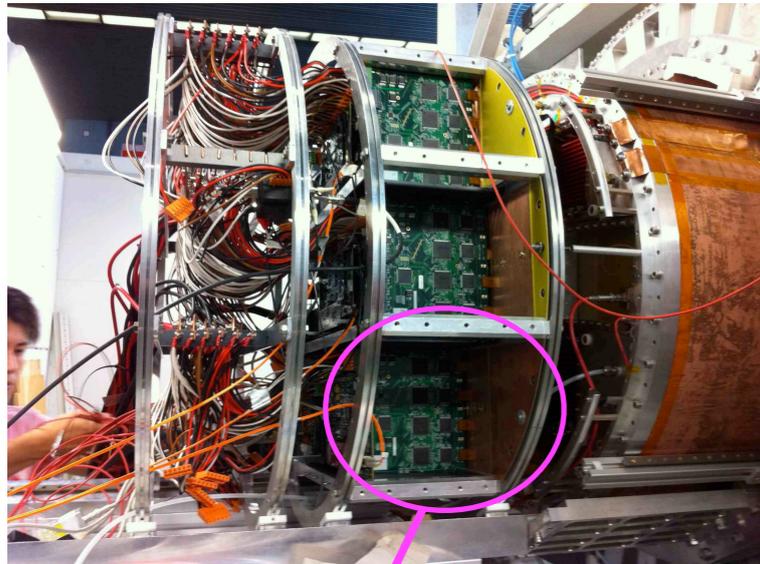


- TPC readout endplate $< 25\% X_0$ in z for PFA
→ Thin electronics are required.

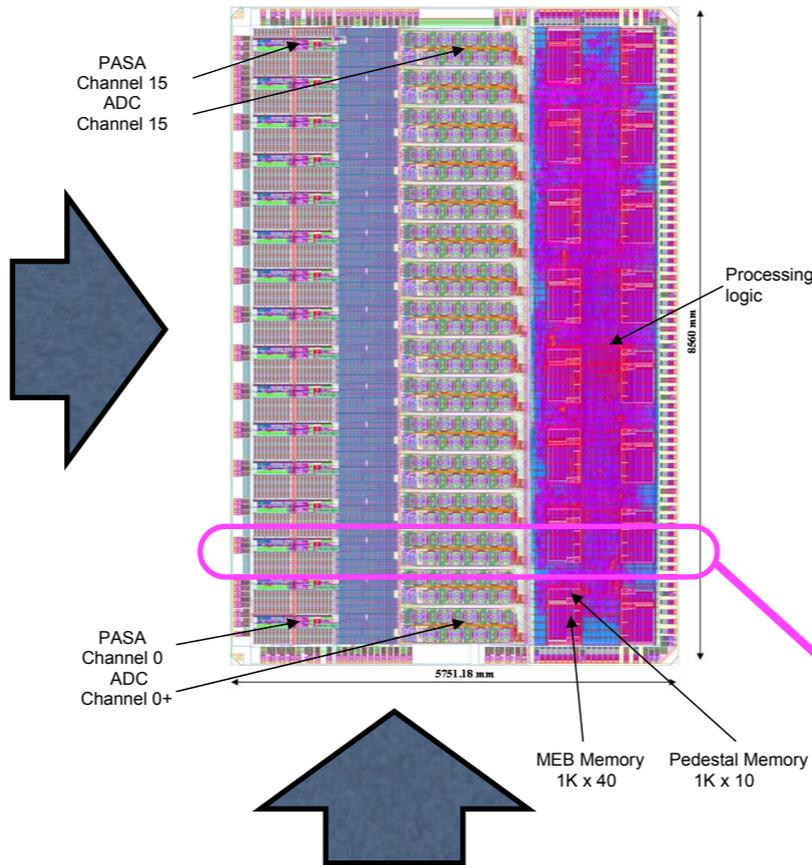
Introduction:

LCTPC Electronics Development for Pad Readout

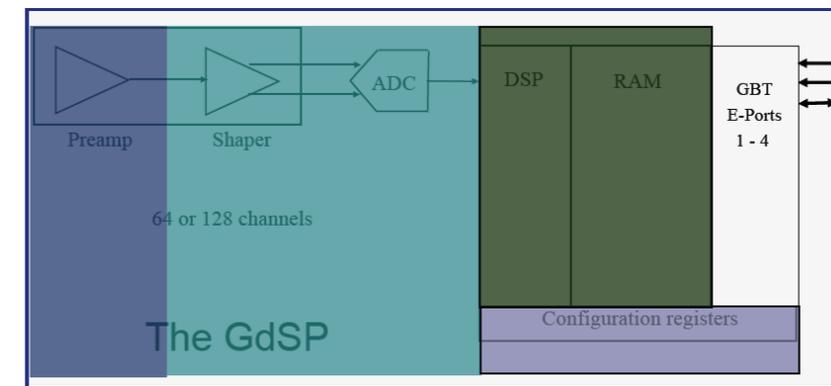
Large Prototype test so far



Next step S-ALTRO16 (fabricated)



Future GdSP



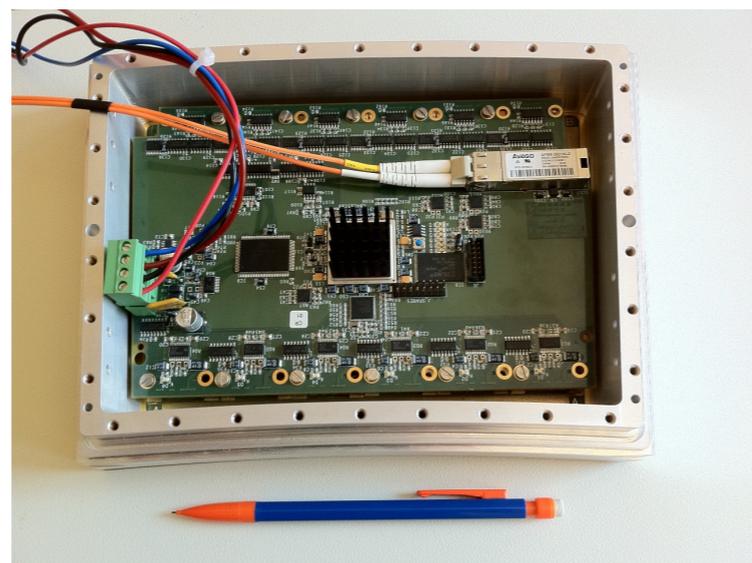
- 64 or 128 channels in a chip.
- Low power consumption (7-8mW/ch).

Front End Card

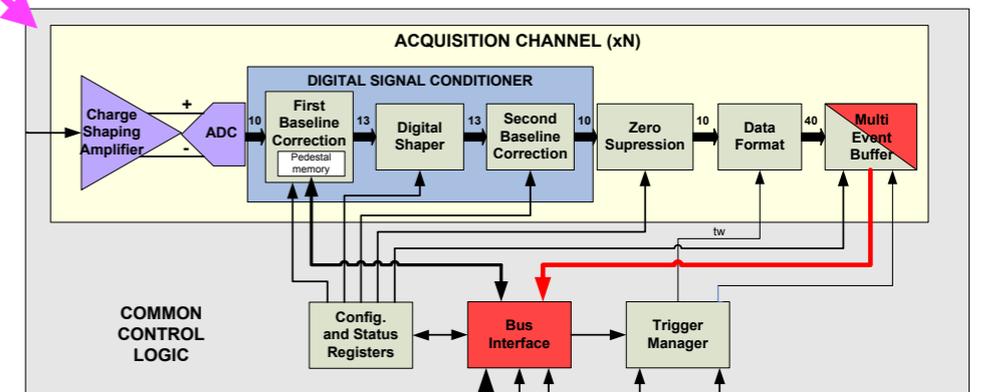


PCA16 (programmable)

ALTRO



MicroMegas module with AFTER-based electronics



- Runs with Sampling Clock
- Runs with Readout Clock

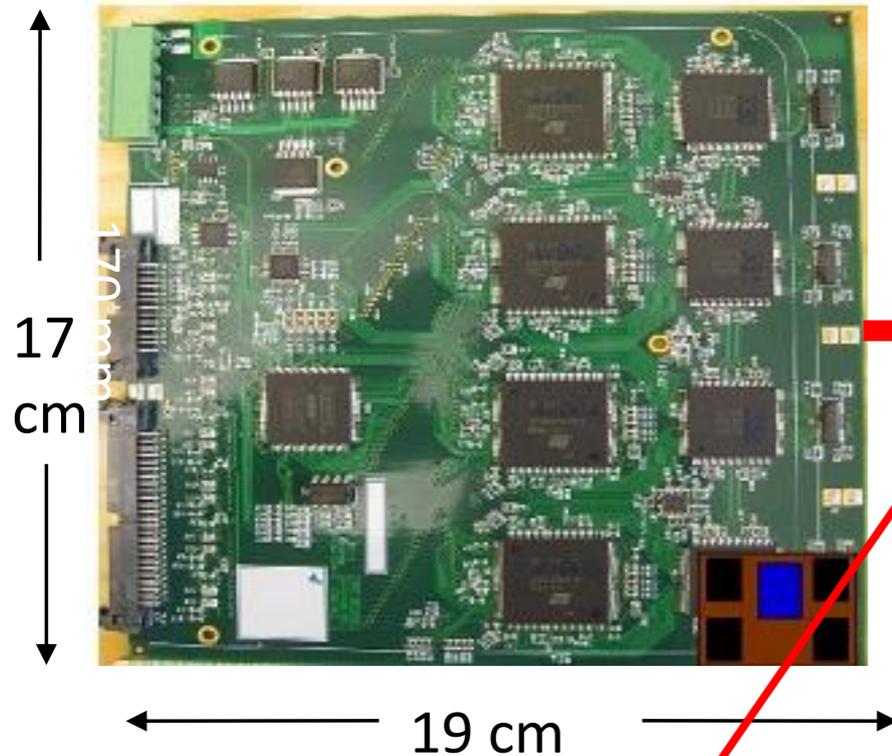
- 16 channels in a chip.
- 59(42)mW per channel @ 40(20)MSPs.

2. Electronics for next pad-readout module

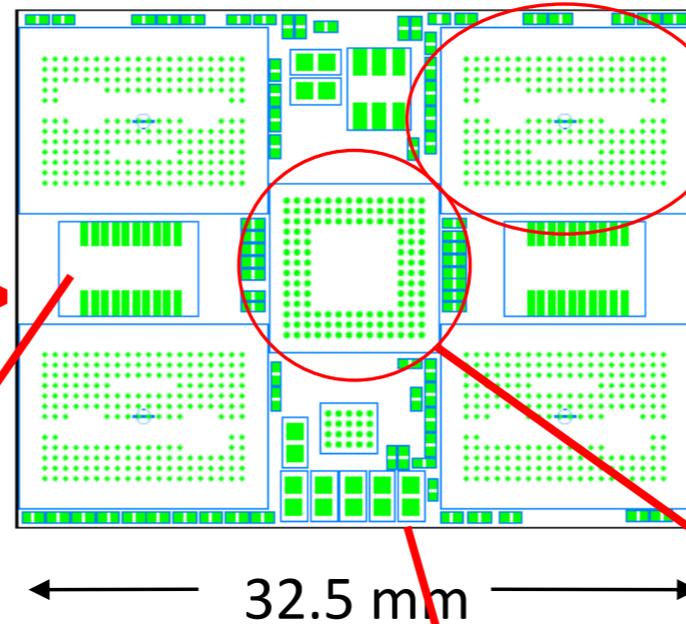
From ALTRO to SALTRO16

A decrease in size by a factor 40 of the front end electronics

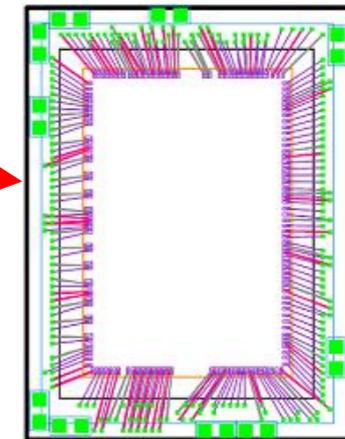
FEC with 8 ALTRO



MCM with 8 SALTRO on carrier boards



Carrier Board

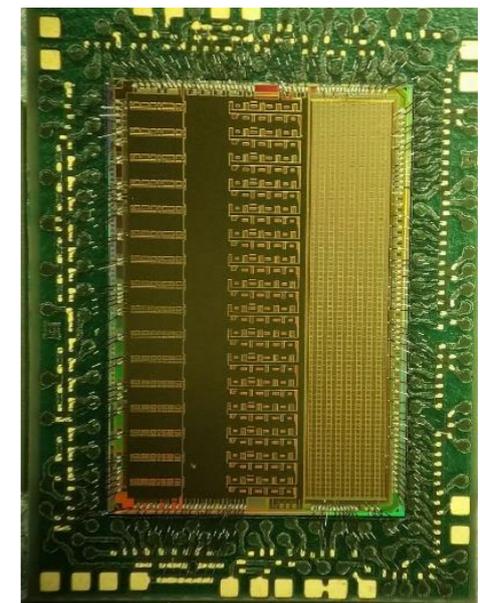


12 mm

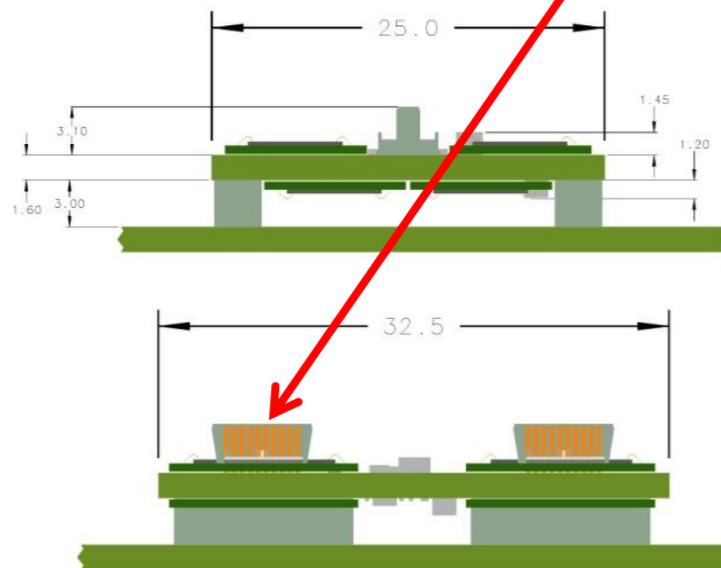
8.9 mm

CPLD

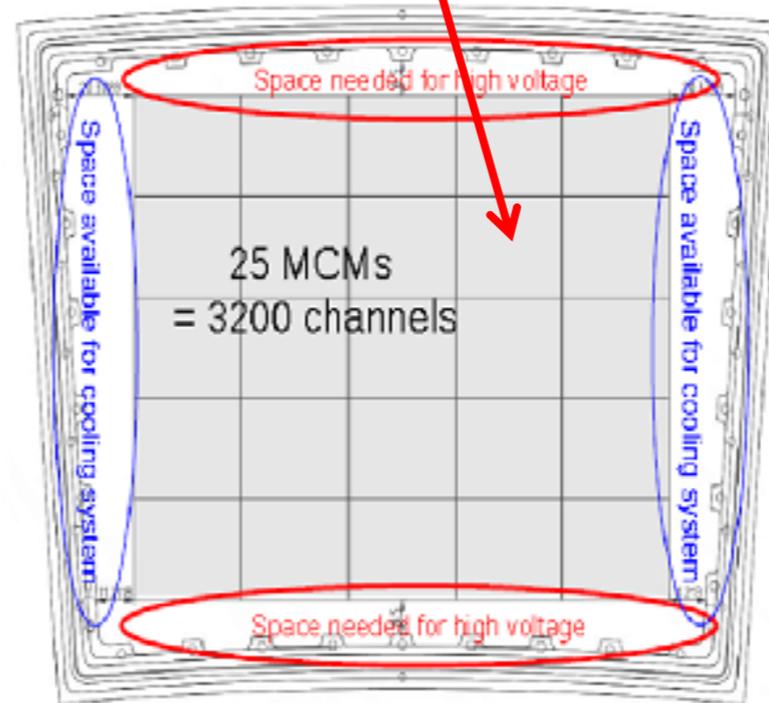
Carrier Board with SALTRO



Side views of an MCM

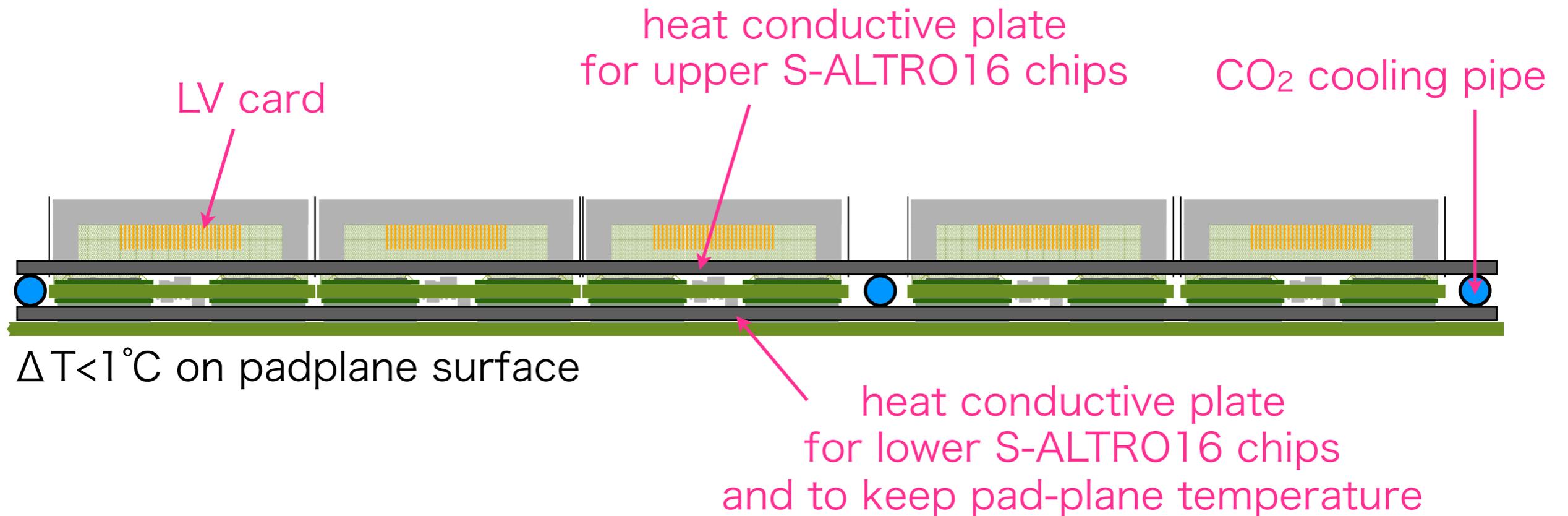
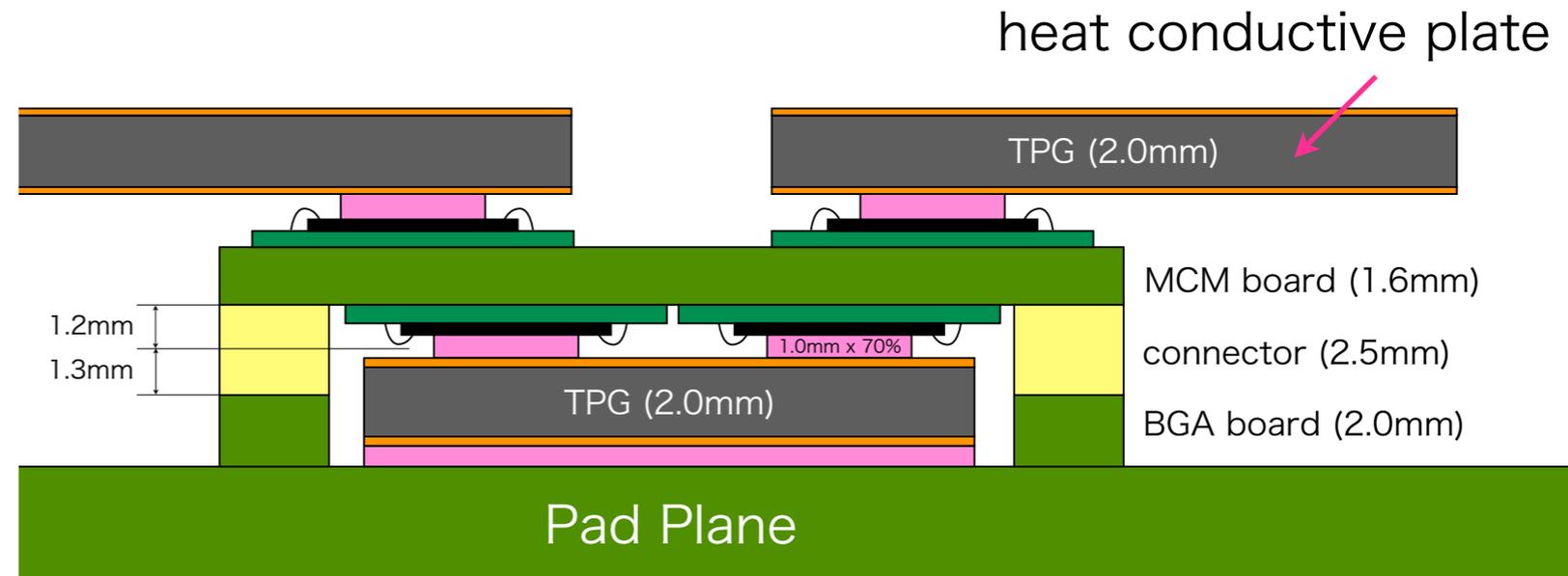
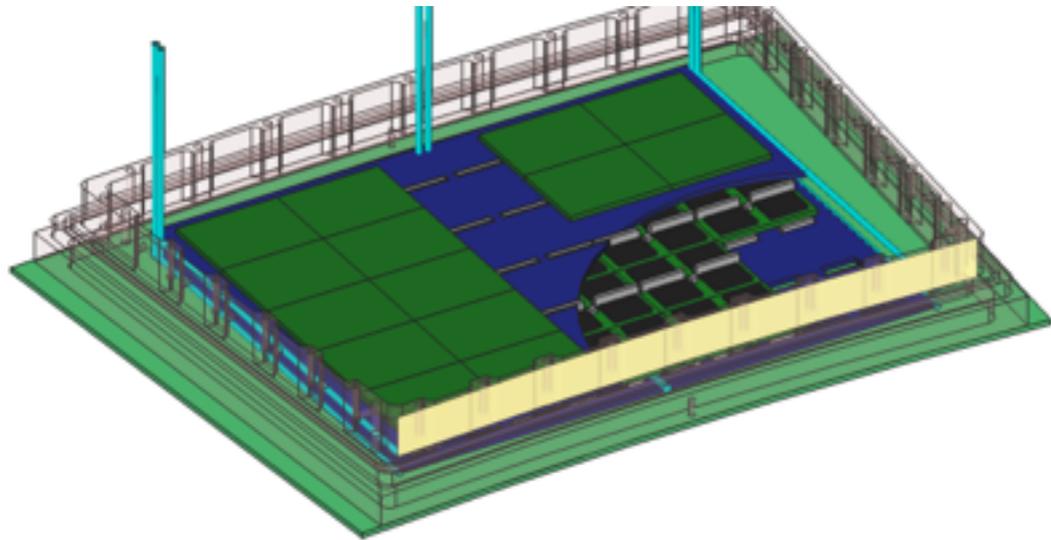


Pad Module



Proposed Cooling for our next module

CO₂ cooling pipe

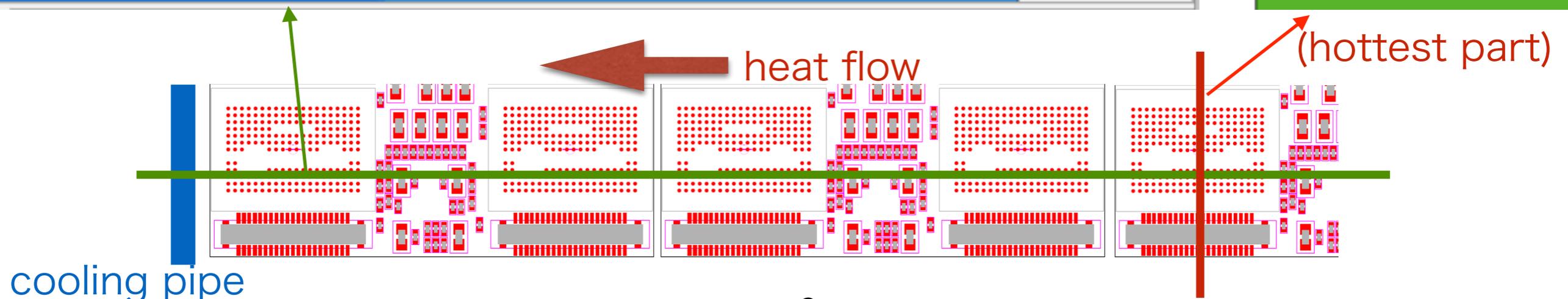
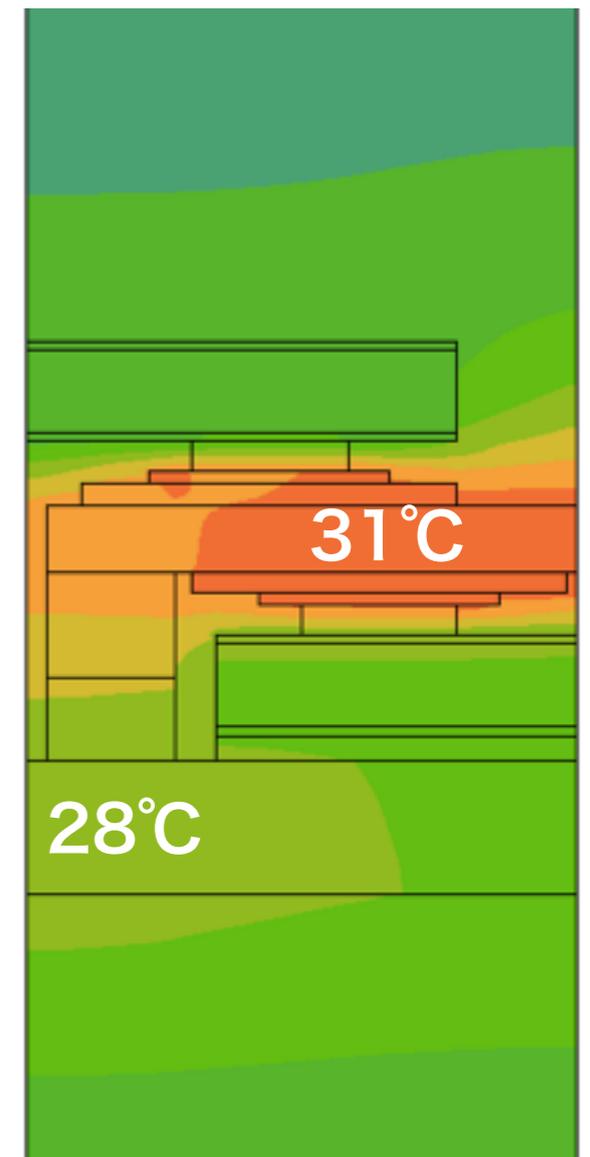
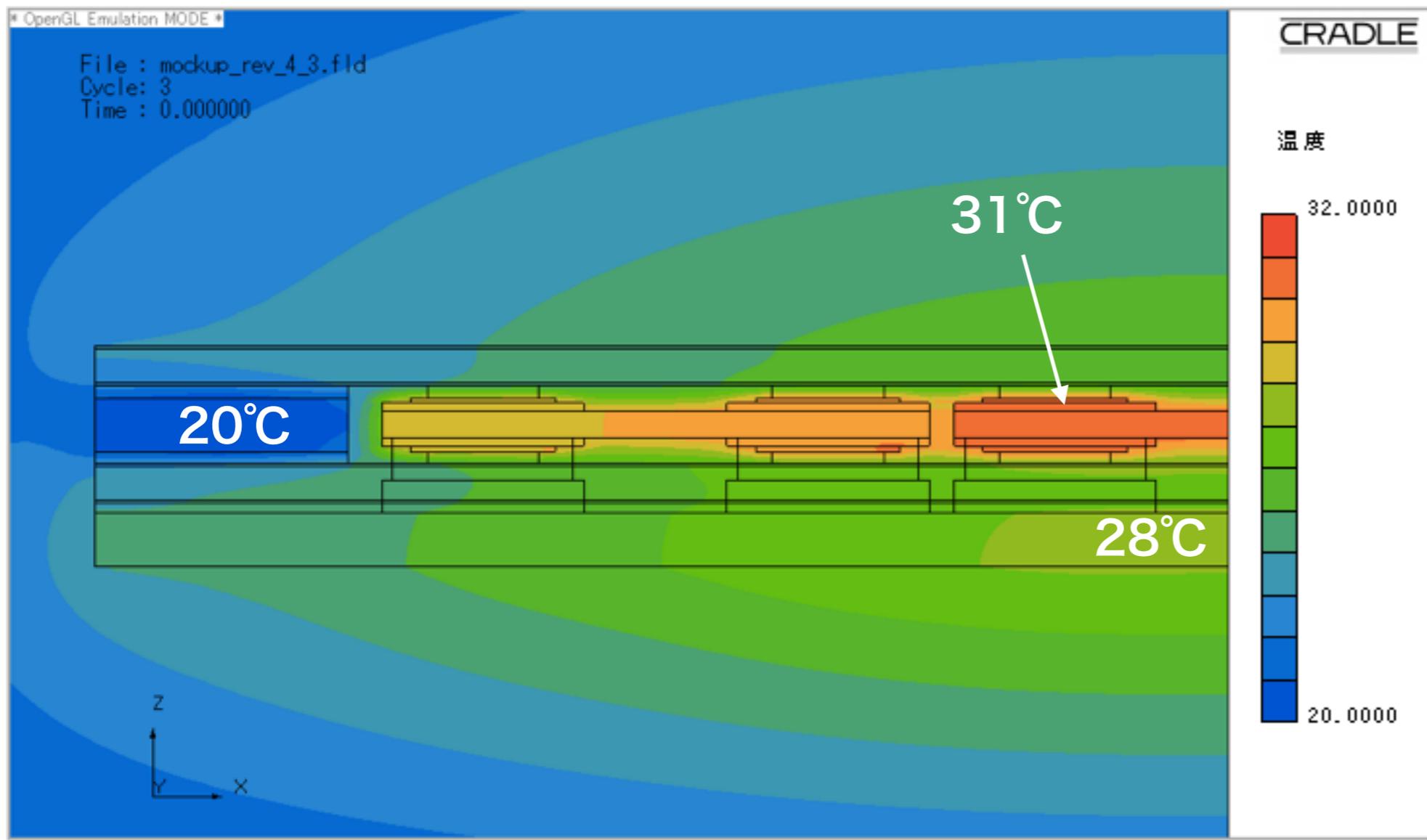


Heat Simulation of the Next Module

Last year's Tokusui mtg

$T(S\text{-ALTRO}) \sim 31^{\circ}\text{C} \rightarrow$ acceptable for the chip operation

$T_{\text{max}}(\text{Pad Plane}) \sim 28^{\circ}\text{C} = T(\text{pipe}) + 8^{\circ}\text{C}$ w/o power pulsing.

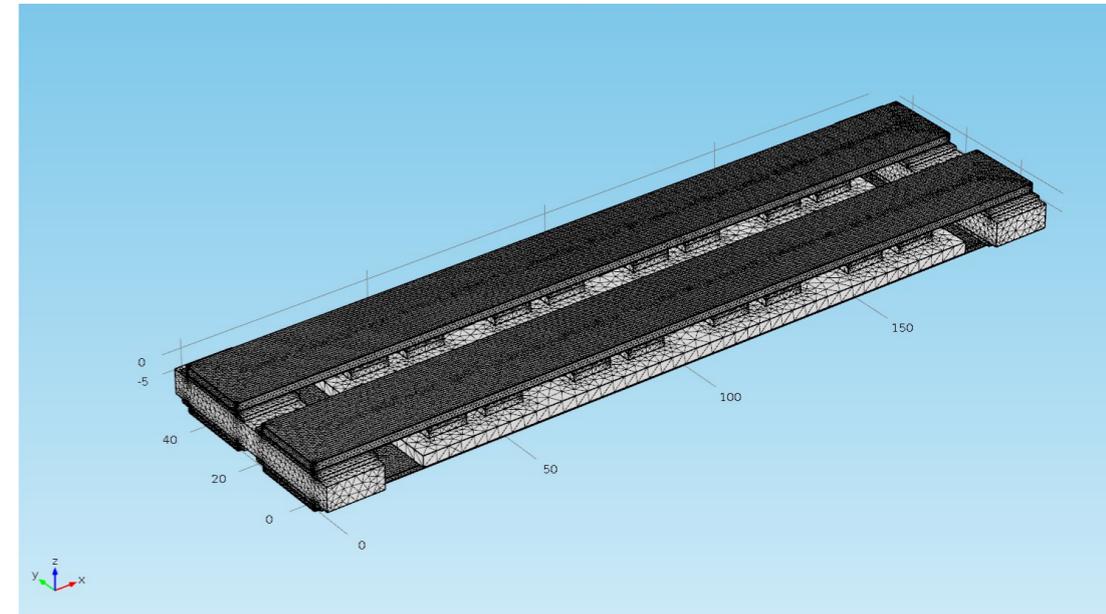


Cross check by different simulator

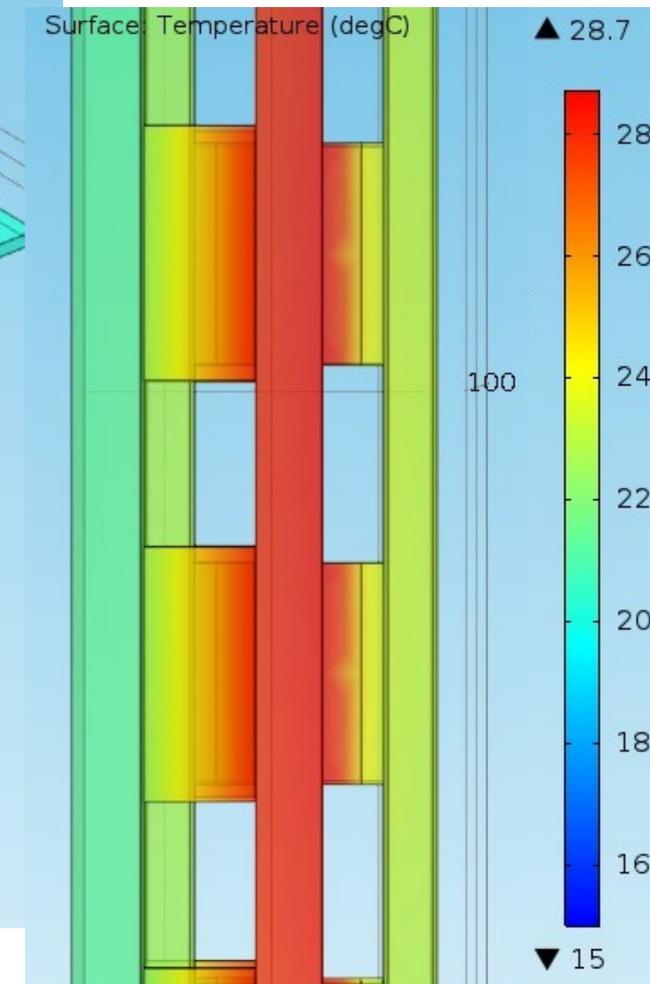
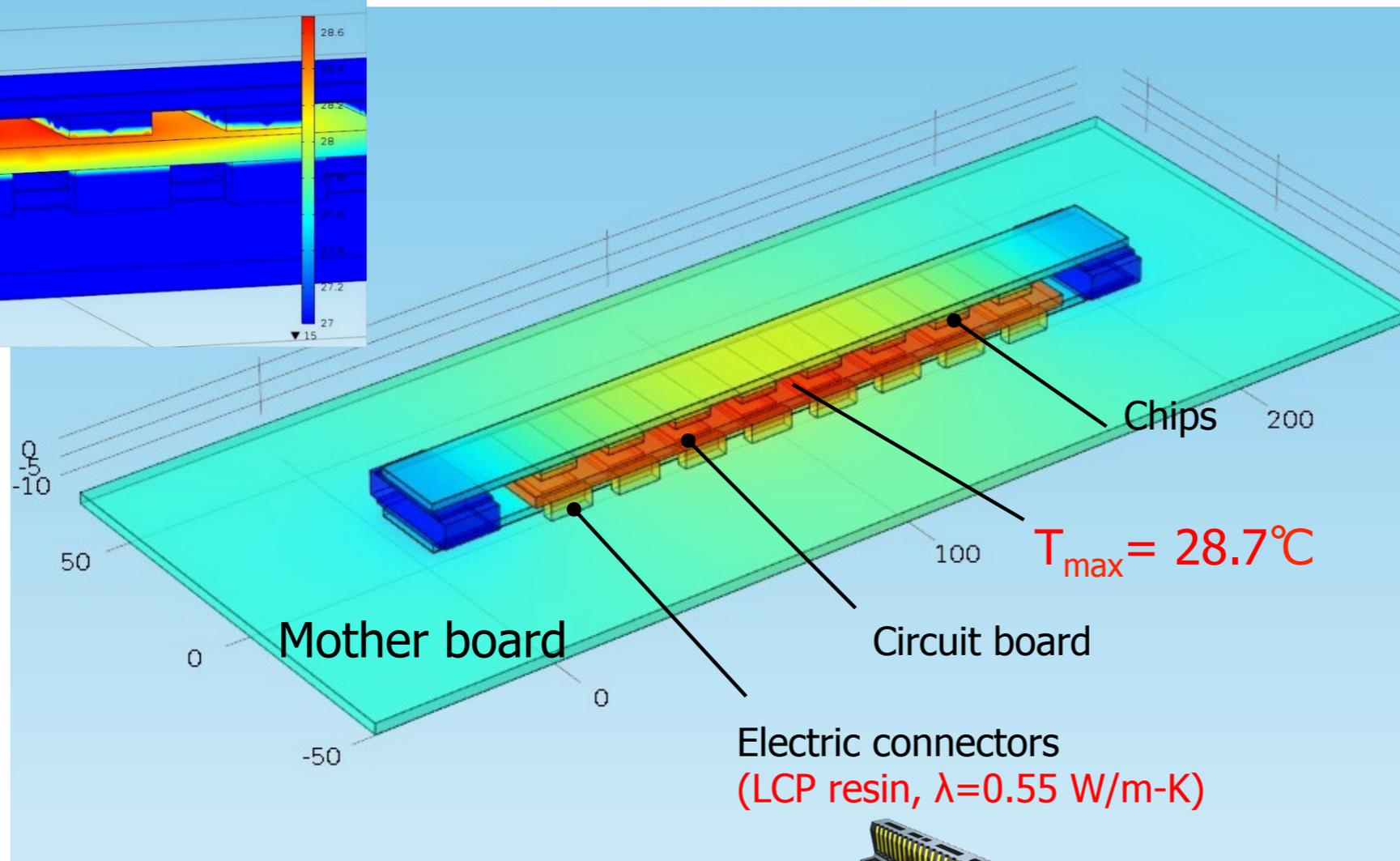
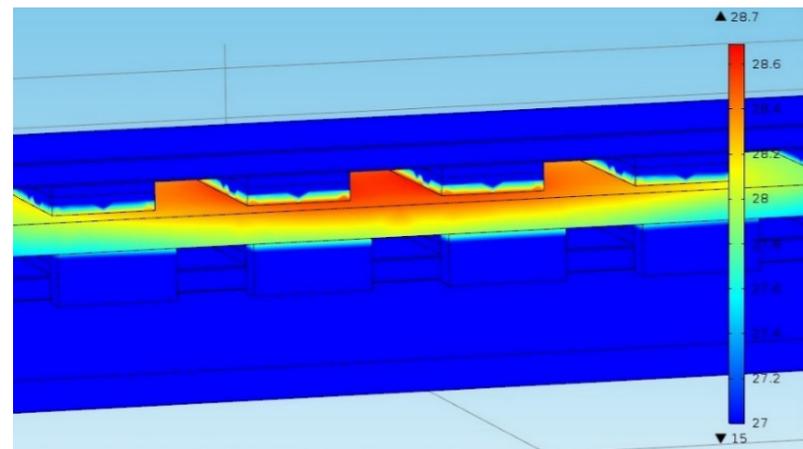
Note: conditions are different:

- 3 → 4 MCMs btw. pipes
- 0.94W → 1.4W per chip
- $T_{\text{pipe}} = 15^{\circ}\text{C}$

$$\rightarrow T_{\text{chip}} = T_{\text{pipe}} + 13.7^{\circ}\text{C}$$

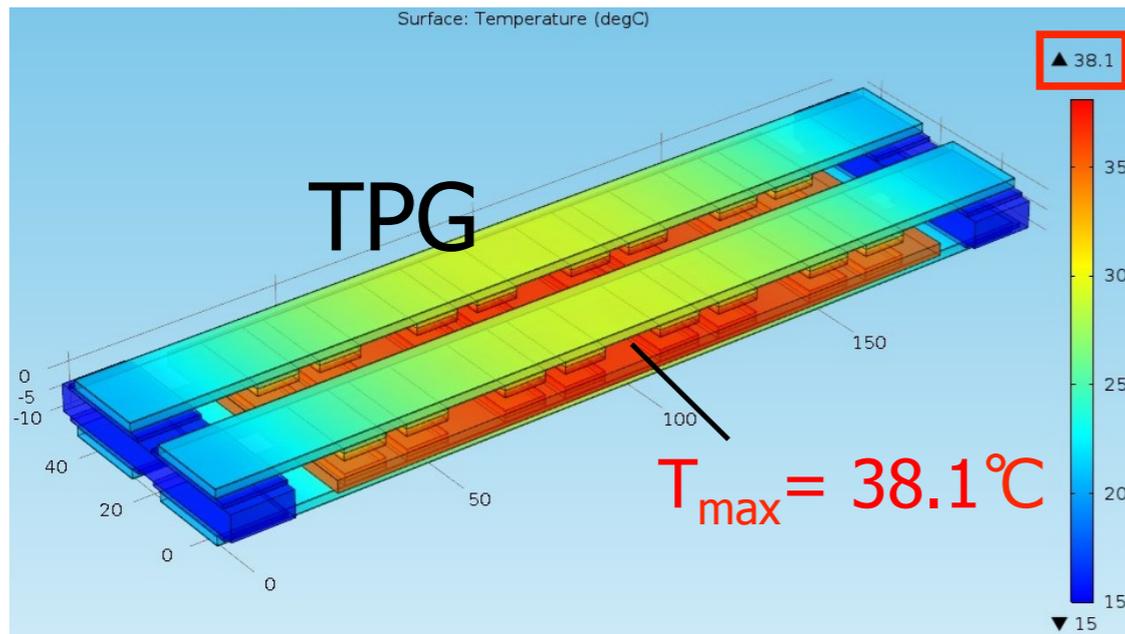


Chip : 16 pcs, 23.04 W

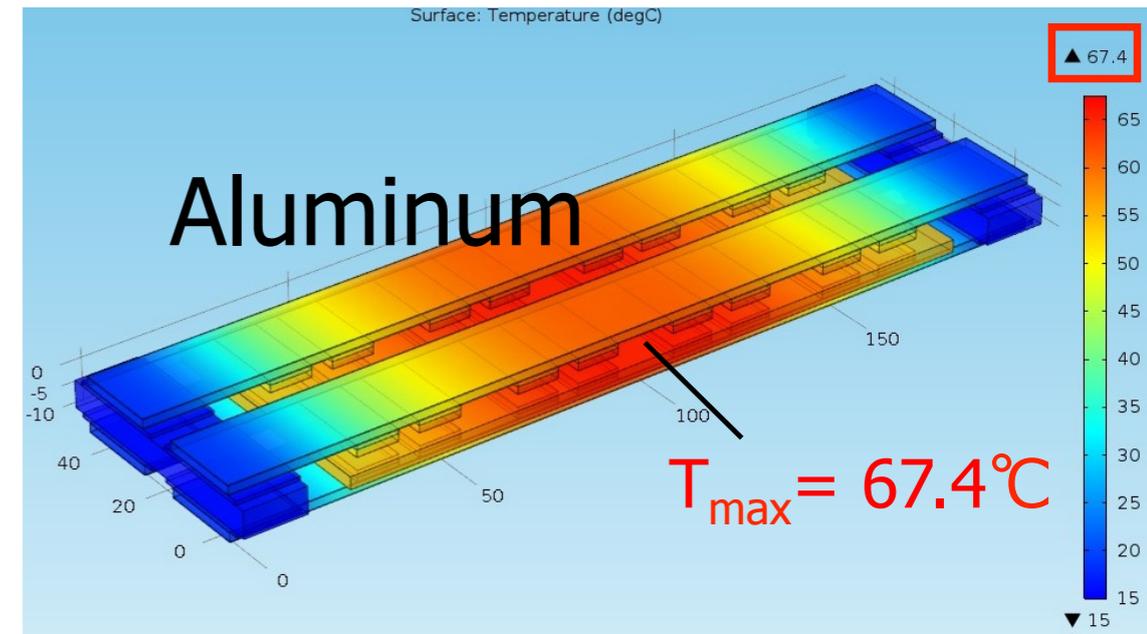


Different Heat Conductor

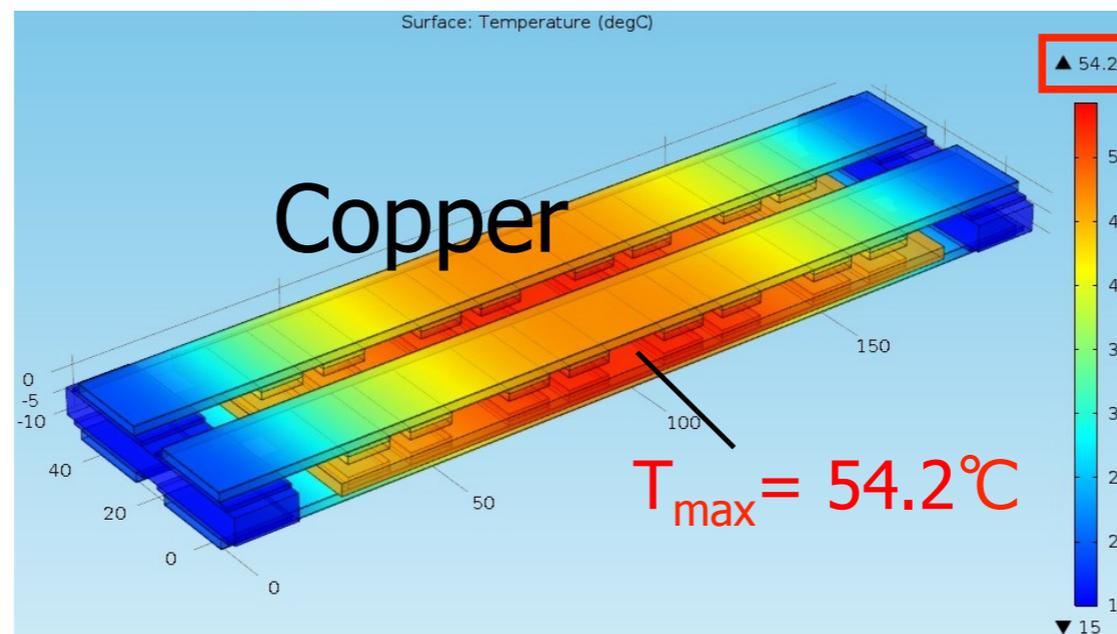
(Again, conditions are different, but just compare different conductors)



TPG $\lambda = \{1500[\text{W}/(\text{m}\cdot\text{K})], 1500[\text{W}/(\text{m}\cdot\text{K})], 20[\text{W}/(\text{m}\cdot\text{K})]\}$

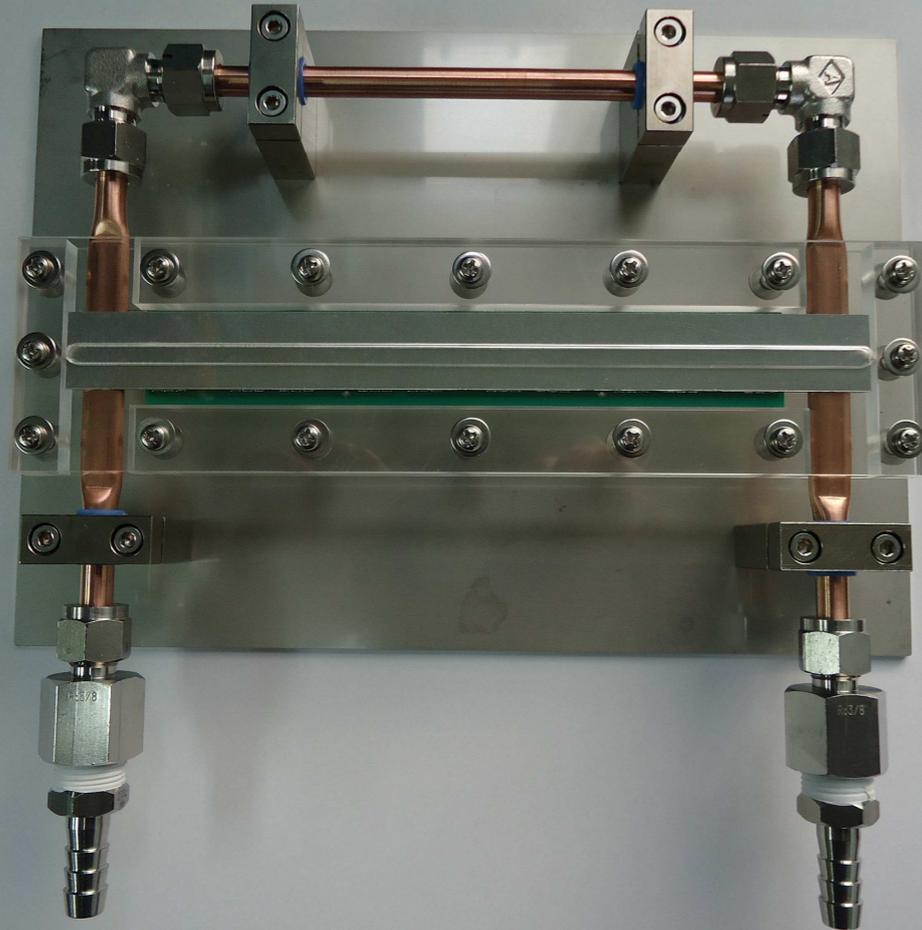


Aluminum $\lambda = 236 [\text{W}/(\text{m}\cdot\text{K})]$



Copper $\lambda = 400 [\text{W}/(\text{m}\cdot\text{K})]$

Mock up test



Mockup test setup for simple water cooling was prepared.
→ Presentation by Daisuke Toda.

By the end of FY15:

- Prepare simple mockup for CO₂ cooling
- Test with KEK CO₂ cooling bench

Next year (and later):

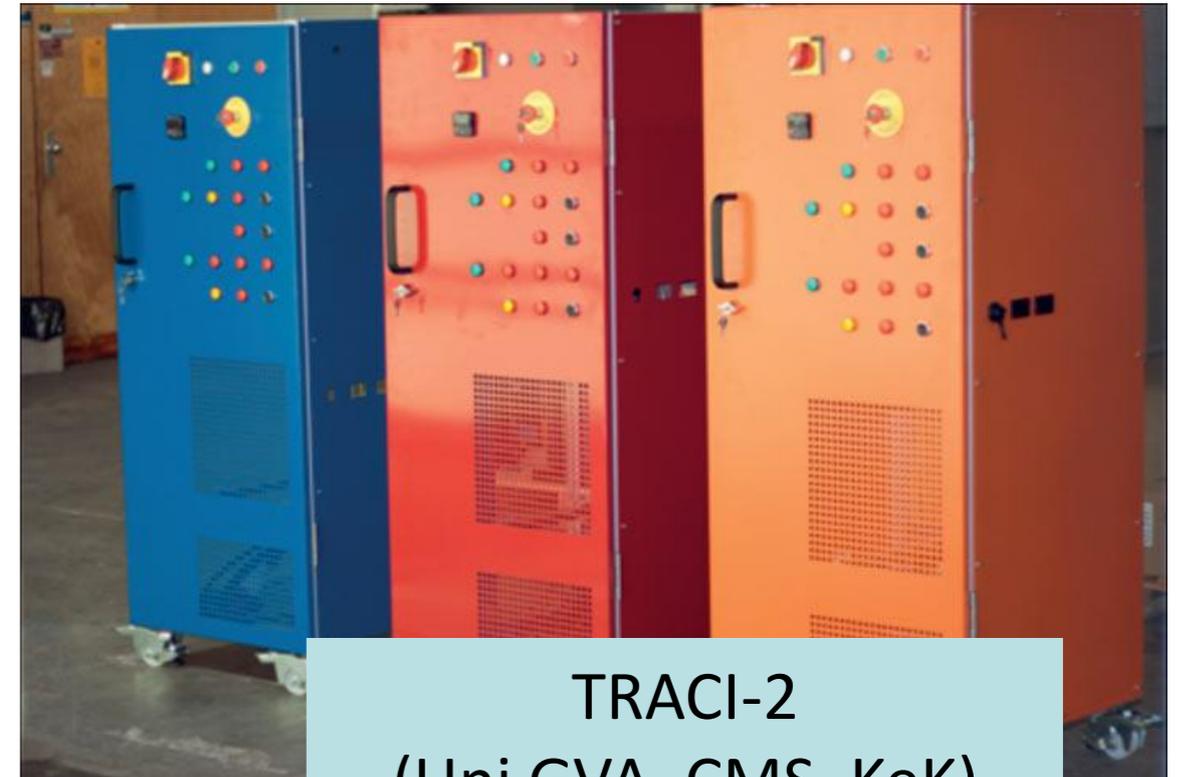
More precise heat mockup with real module size (but probably only limited number of heat sources) with also realistic mechanical support devices.

2-Phase CO₂ Cooling systems

KEK CO₂ group for
Belle II VTX, ILC VTX, ILC TPC



KEK-TRACI2 for LCTPC
by Bart Verlaat @ NIKHEF



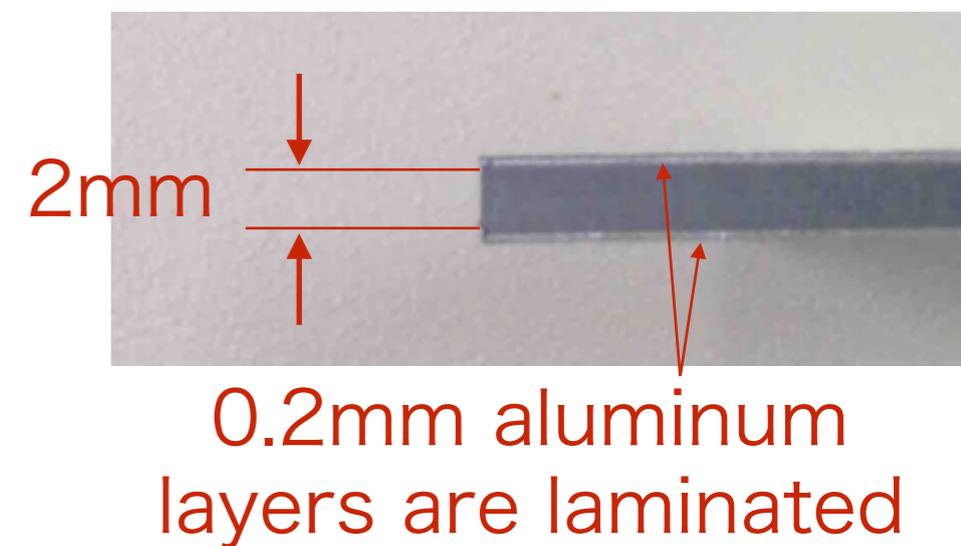
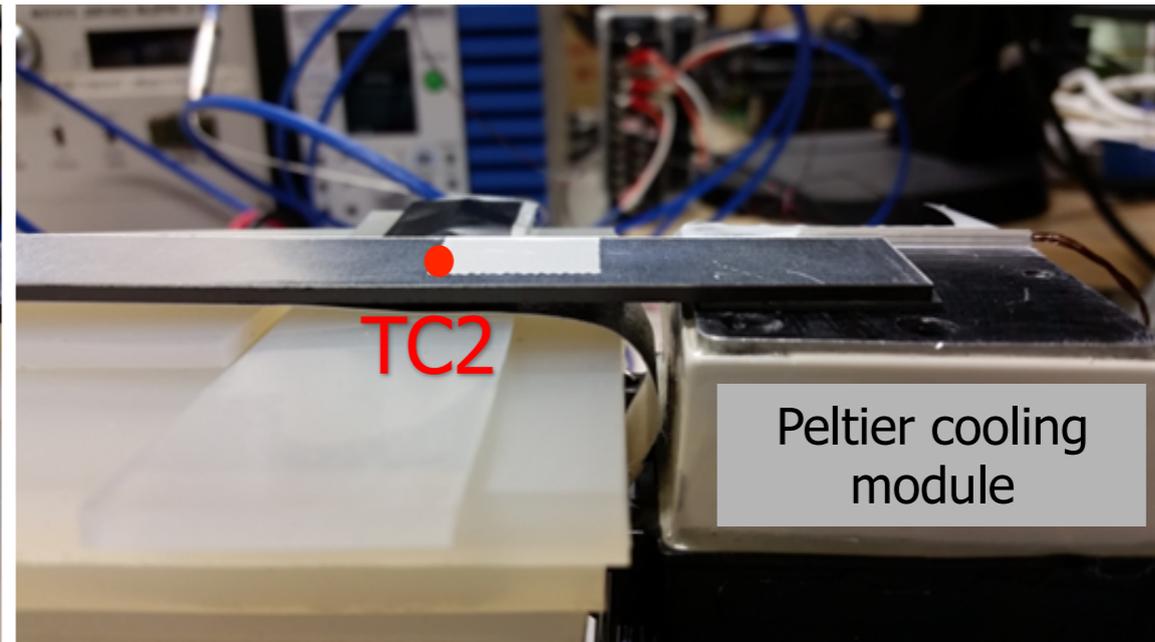
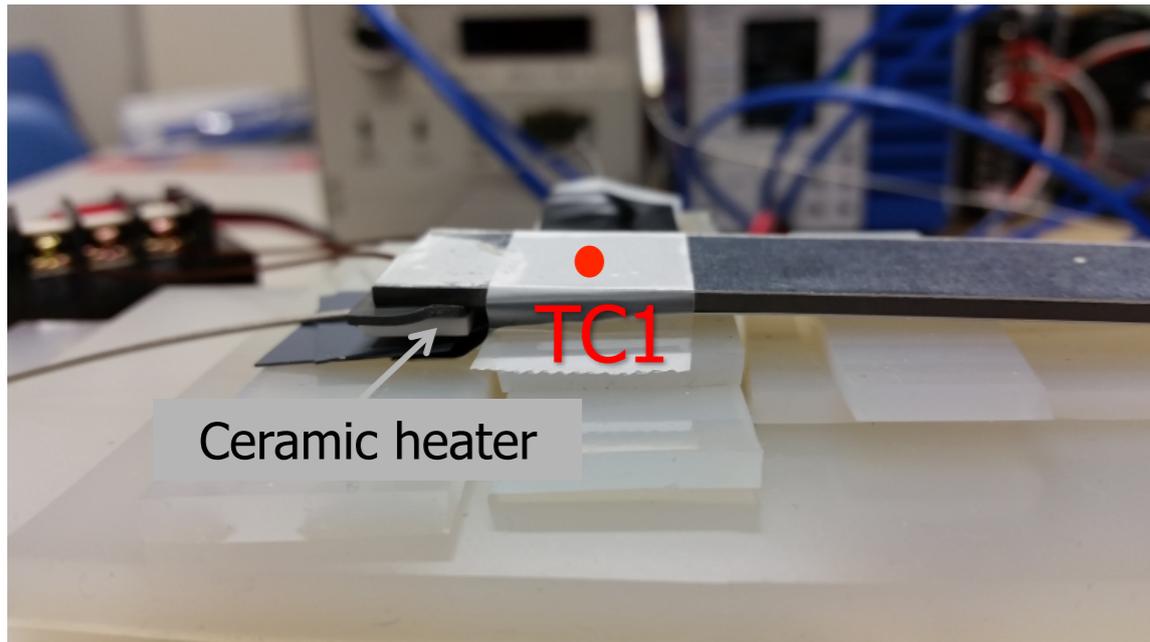
TRACI-2
(Uni GVA, CMS, KeK)

- **Portable** laboratory cooling unit
- Cooling power <100W – 250 W>
- Temperature range <-40°C;+20°C>
- **Turn key**
- Very simple to operate "**fridge like**"

KEK-TRACI2 is now working at DESY.
MM group uses for their beamtest.

3. Evaluation of TPG

Evaluation of Heat Conductive Plate, TPG

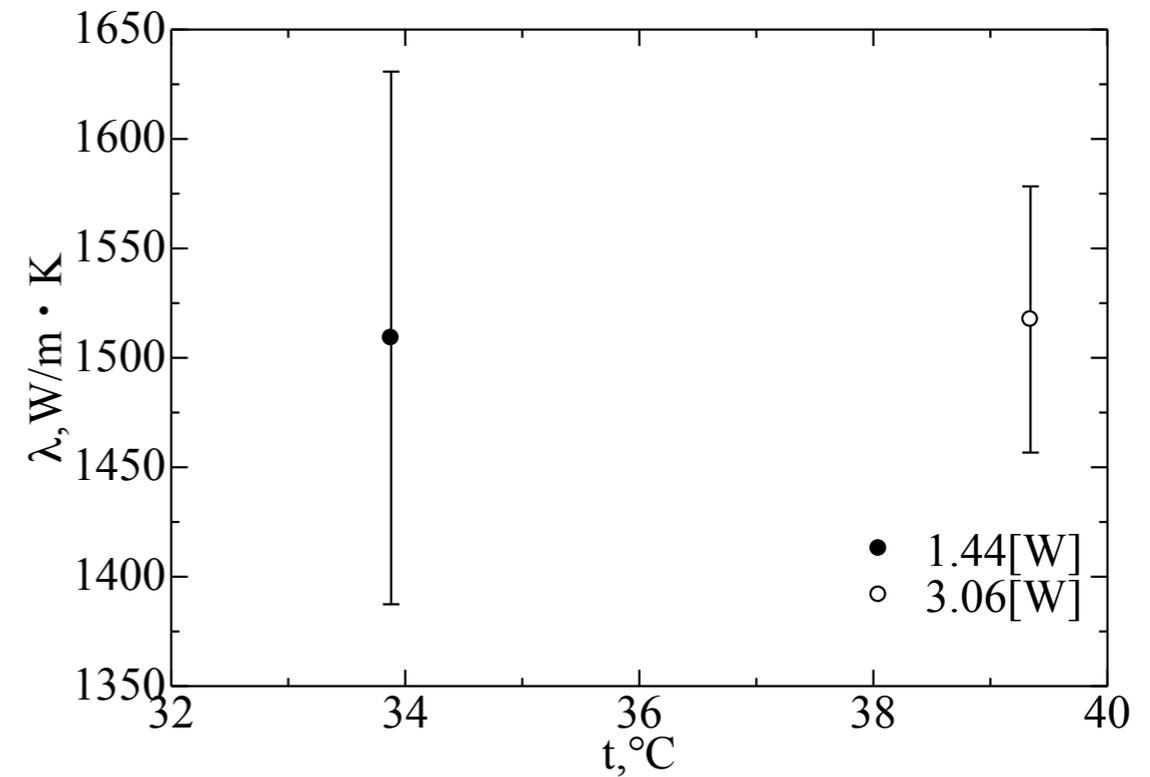


Evaluation of Heat Conductive Plate, TPG

steady state method



y-axis: Temperature, °C **x-axis: time, s**



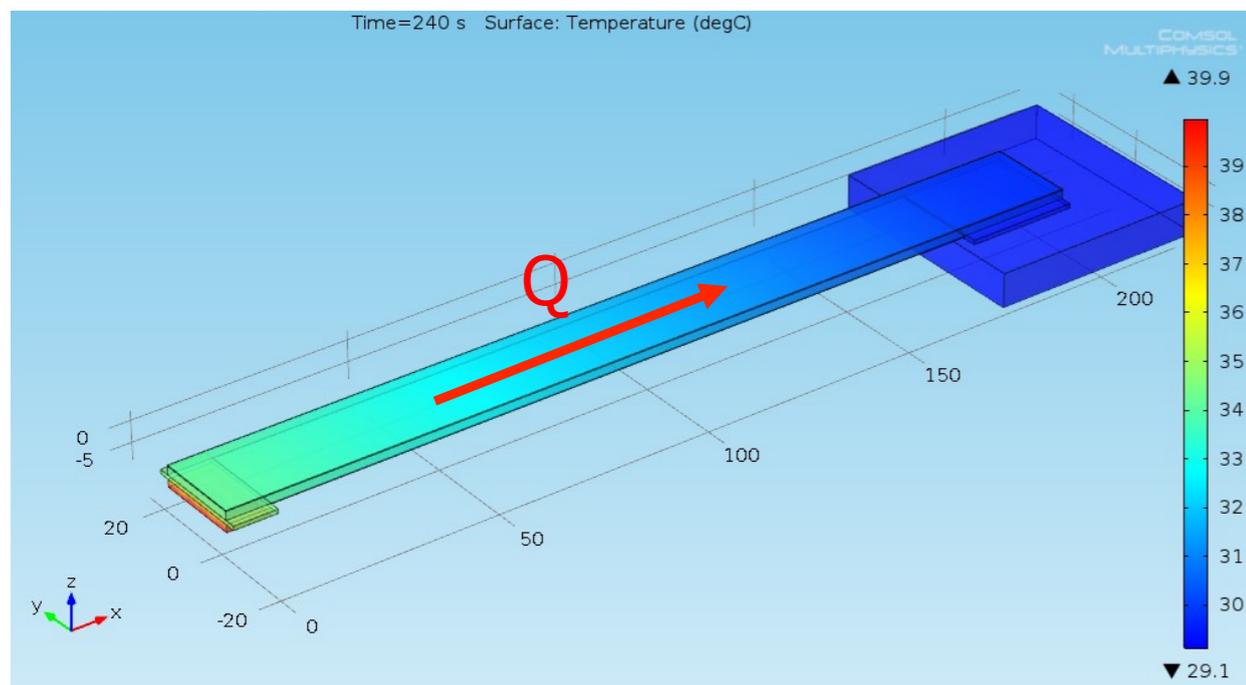
Results of thermal conductivity measurements

1.44[W]
 $\lambda = 1509 \pm 121.7 \text{ W/(m-K)}$
3.06[W]
 $\lambda = 1518 \pm 60.8 \text{ W/(m-K)}$

Evaluation of Heat Conductive Plate, TPG

Results

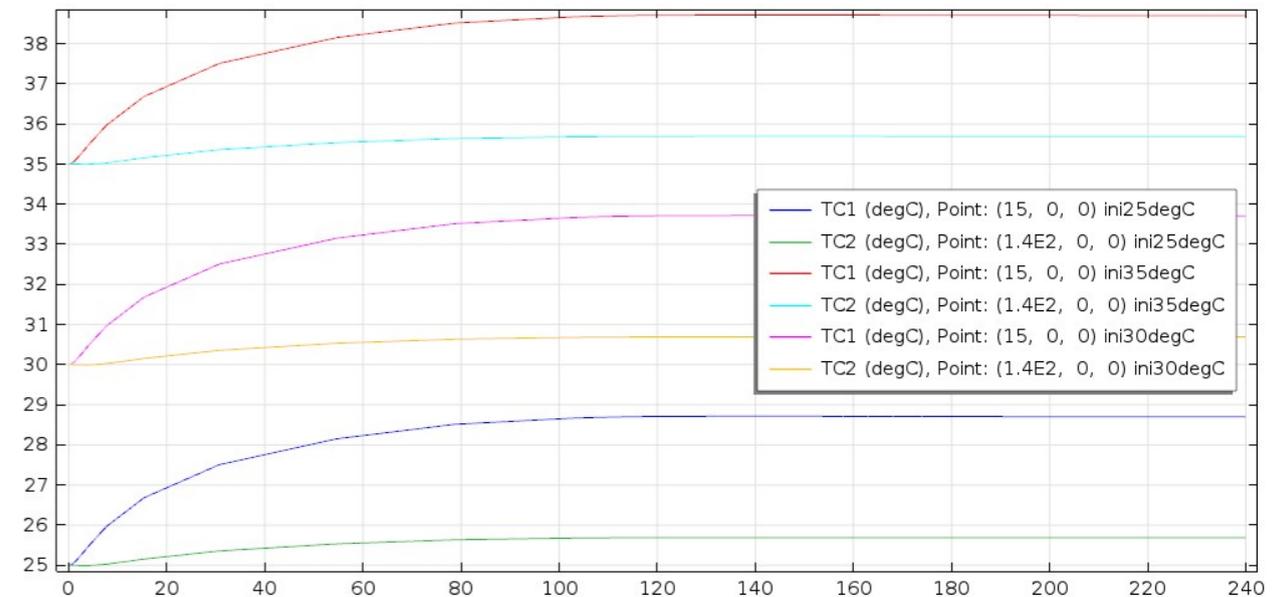
Analysis Results



※Analysis software: COMSOL Multiphysics v5.0

TPG: $\lambda = \{1500[\text{W}/(\text{m} \cdot \text{K})], 1500[\text{W}/(\text{m} \cdot \text{K})], 20[\text{W}/(\text{m} \cdot \text{K})]\}$

TPG { 1500,1500,20 }, Cp 710, rho 2260, Ttrl 0.02mm, 10 W/(m K), (0, 0.1, 240), finer mesh, (P)-1.4448W



Time (s)	Temperature	Temperature	Temperature	Temperature	Temperature	Temperature
239.4	28.70138	25.68816	38.70138	35.68816	33.70138	30.68816
239.5	28.70138	25.68816	38.70138	35.68816	33.70138	30.68816
239.6	28.70138	25.68816	38.70138	35.68816	33.70138	30.68816
239.7	28.70137	25.68816	38.70137	35.68816	33.70137	30.68816
239.8	28.70137	25.68816	38.70137	35.68816	33.70137	30.68816
239.9	28.70137	25.68816	38.70137	35.68816	33.70137	30.68816
240	28.70136	25.68816	38.70136	35.68816	33.70136	30.68816

Experimental result

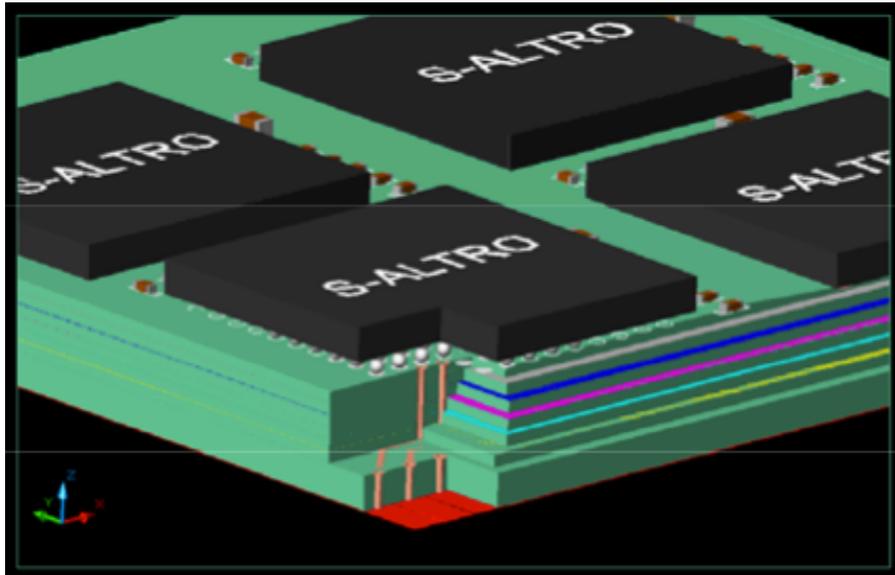
$$\Delta T = 2.98 \text{ } ^\circ\text{C}$$

Analysis result

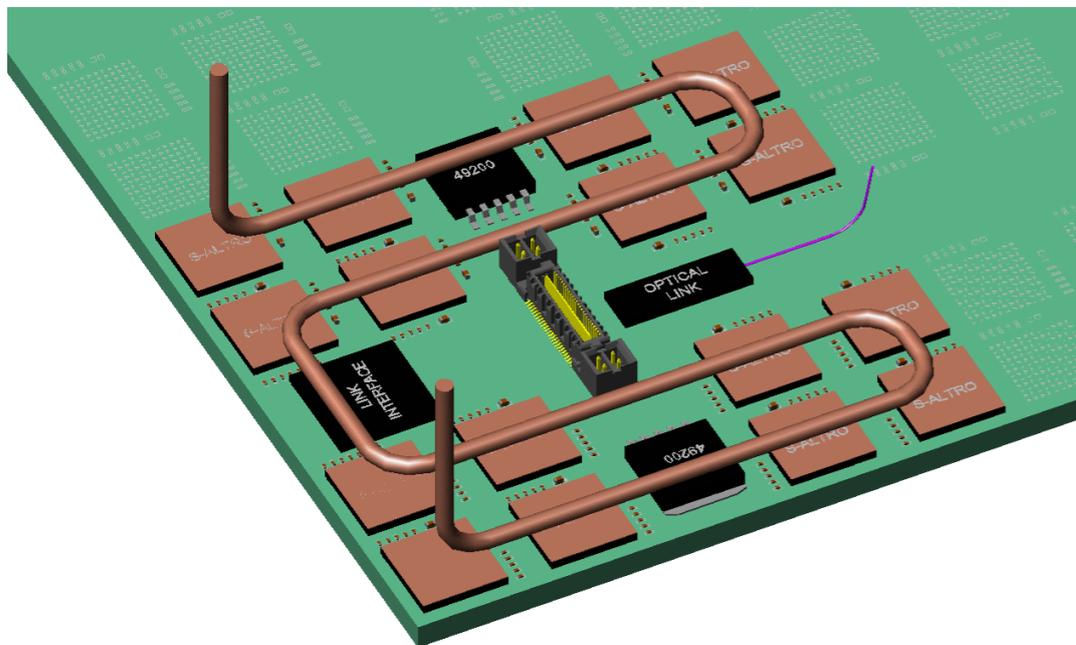
$$\Delta T = 3.01 \text{ } ^\circ\text{C}$$

4. Towards the final electronics

Advanced Endplate Concept



- high channel-density chips are mounted on the backside of the endplate.
- ASIC specifications were discussed (next page) but not final ones.
- Study of in-board cooling channels is necessary.



Parameters of final ILD TPC

1.) List: Parameters driven by physics

Preamplifier: input capacitance (5-20 pF)

shaping peaking time (60-200 ns) Martin Ljunggren MSc

sensitivity (1-10 mV/fC)

polarity (negative)

dynamic range (SALTRO: 150 fC, AFTER: 120, 240, ?, 600fC) dE/dx

linearity error <1% for full dynamic range dE/dx

noise (<600 electrons)

Shaper: restoring to baseline in units of counts

at least 1 μ s for Micromegas (not to lose the signal on side pads)

ADC: number bits (8-10) Wenxin's thesis (Saclay), Liangliang's thesis (Lund) for spatial resolution

sampling frequency (20 - 40 MHz)

Time of continuous readout: \sim 800 μ s (full bunch train)

2.) List system driven by other considerations

Input leakage current compensation (if too high -> noise, but may be necessary, e.g. for protection diodes)

pad density (1/4 of smallest pad size per channel)

Power consumption: 4 mW/channel (without power pulsing) -> 20 W per Module (5000 channels) -> 1 kW per endcap with power pulsing (+ at least a factor of 5 in power reduction by power pulsing)

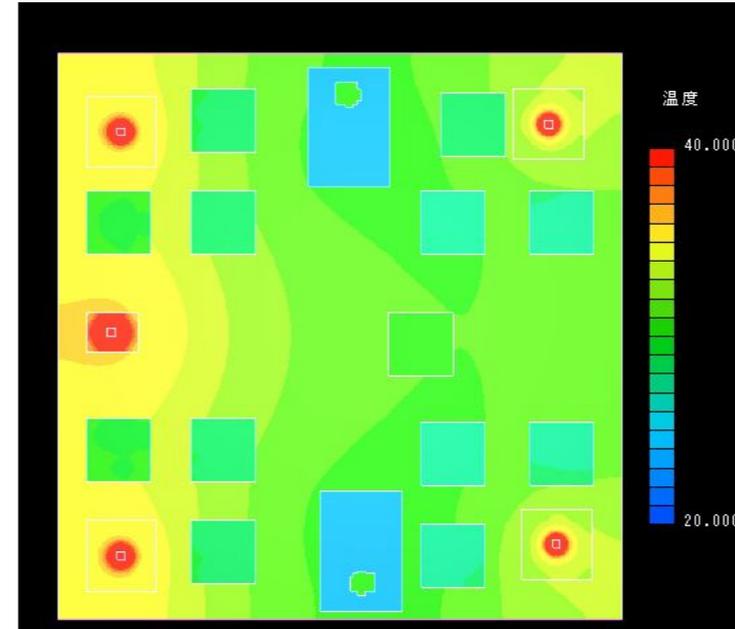
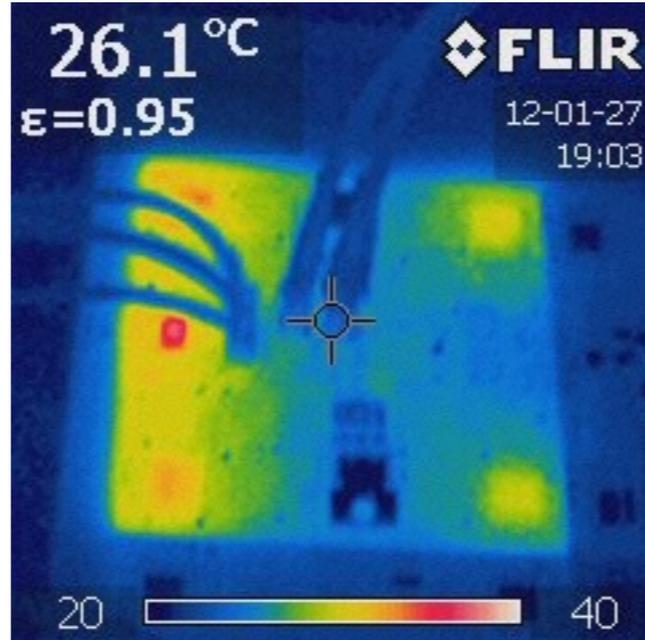
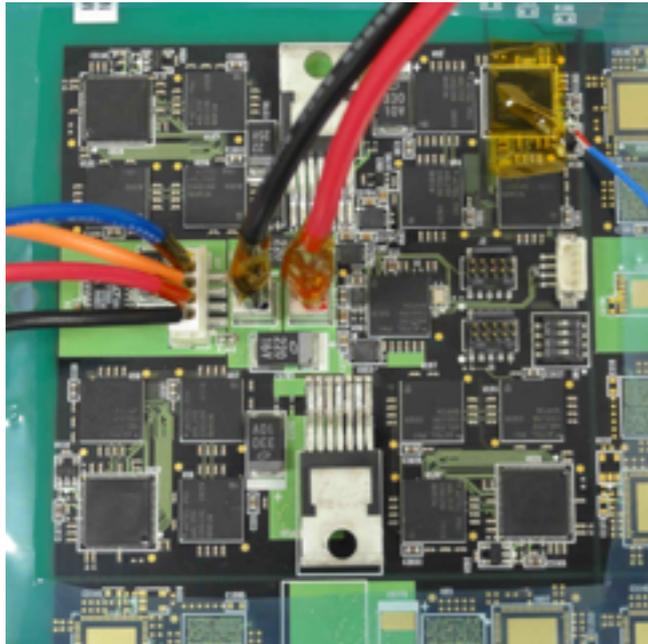
from <https://agenda.linearcollider.org/event/6507/>

AEP heat mockup test

Observation

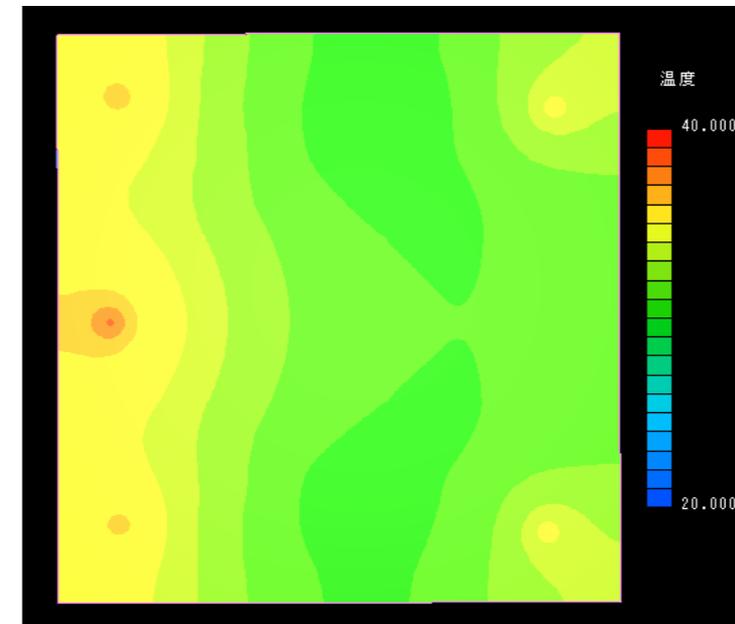
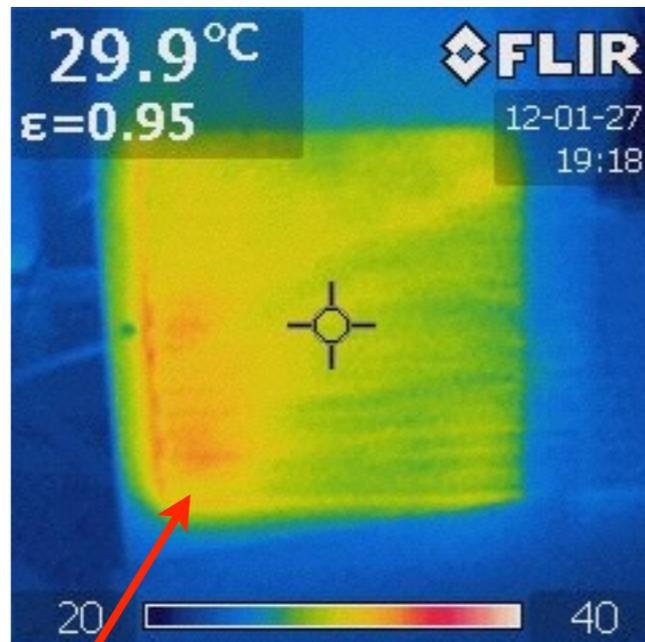
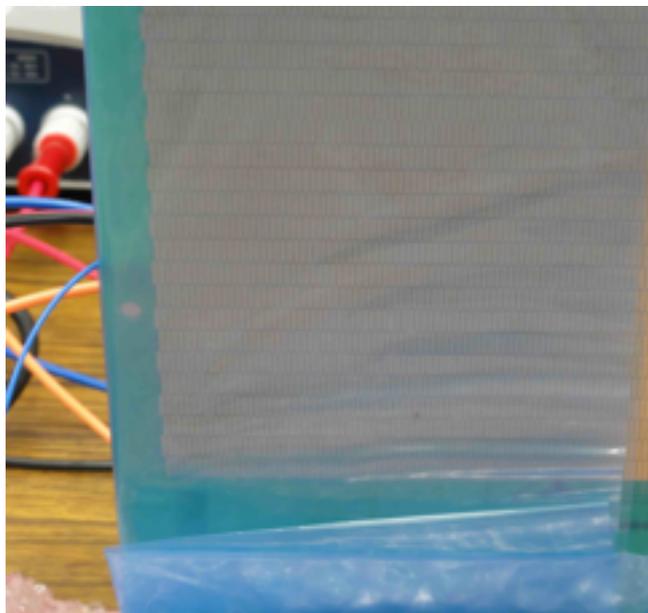
Simulation

Part side



$$P_{\text{tot}} = 1.44\text{W}$$

Pad side

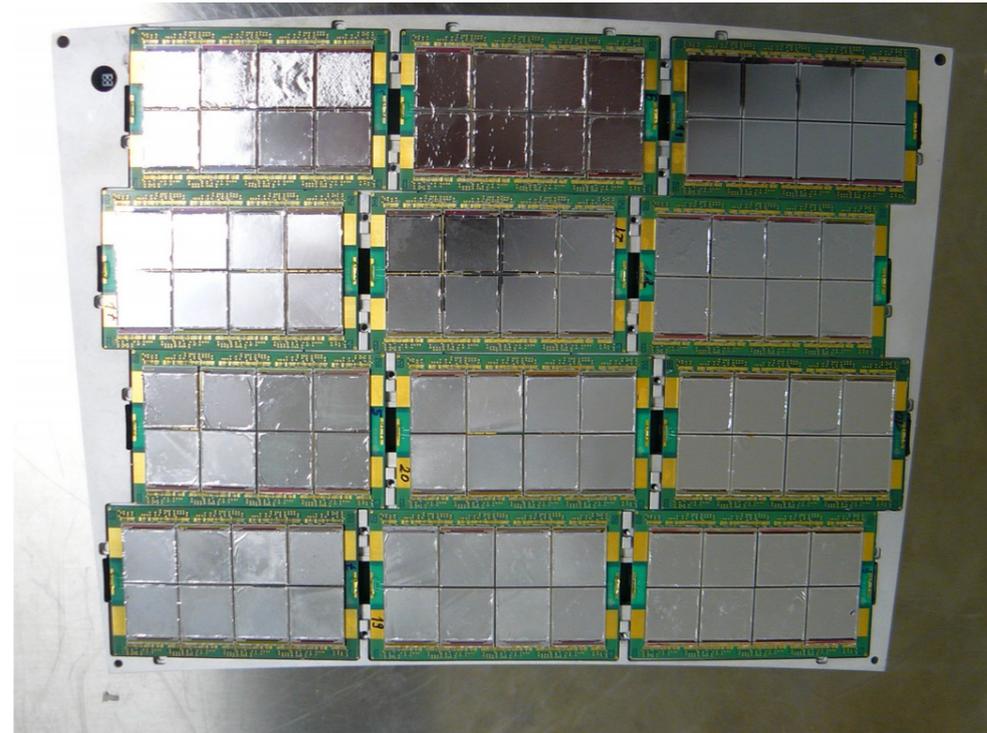
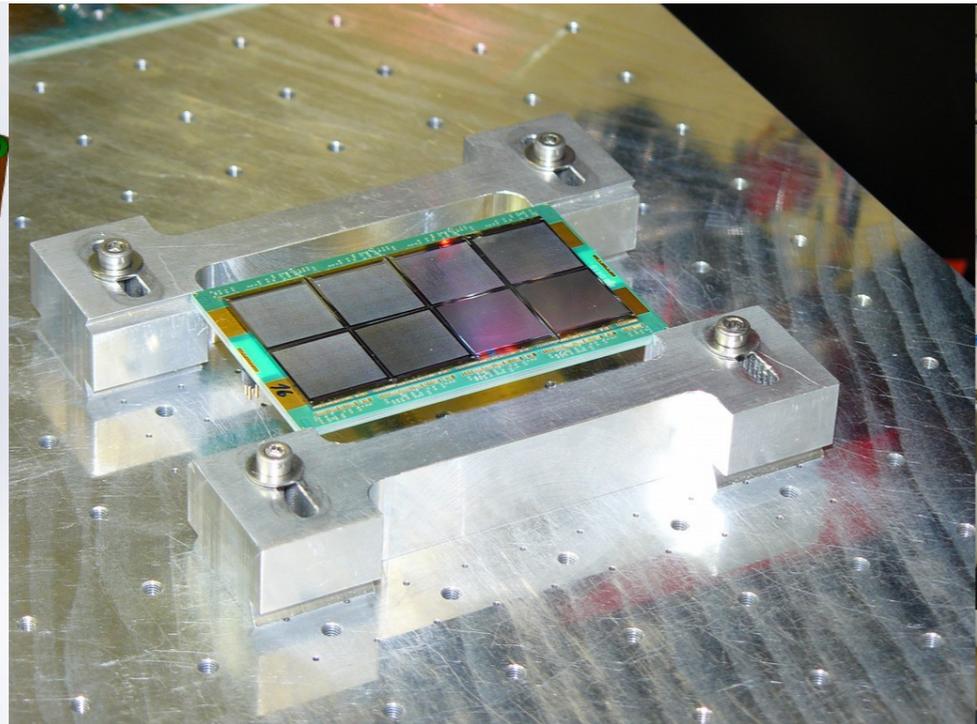


$$\Delta T \text{ will be } > 10 \text{ [K]} \times \frac{57 \text{ [W]} (16 \text{ SALTRO's})}{1.44 \text{ [W]} (\text{this experiment})} \times 1.5 \% (\text{PP}) = 5.9 \text{ [K]}$$

(w/o cooling, w/ PP, w/ real SALTRO)

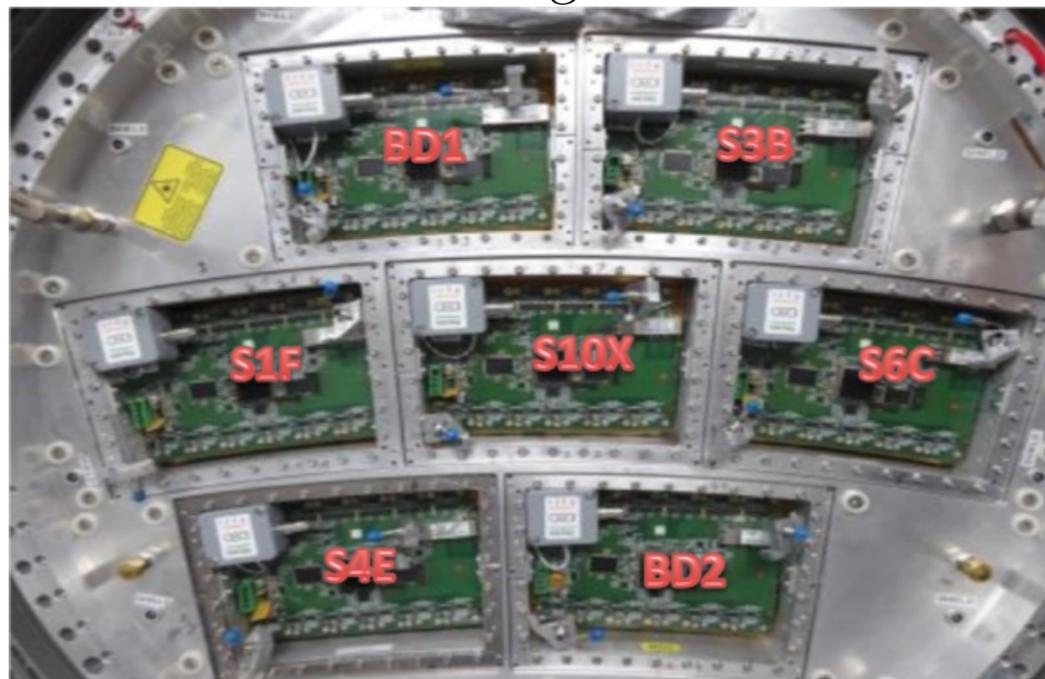
TimePix module / MM module

TimePix Ingrid

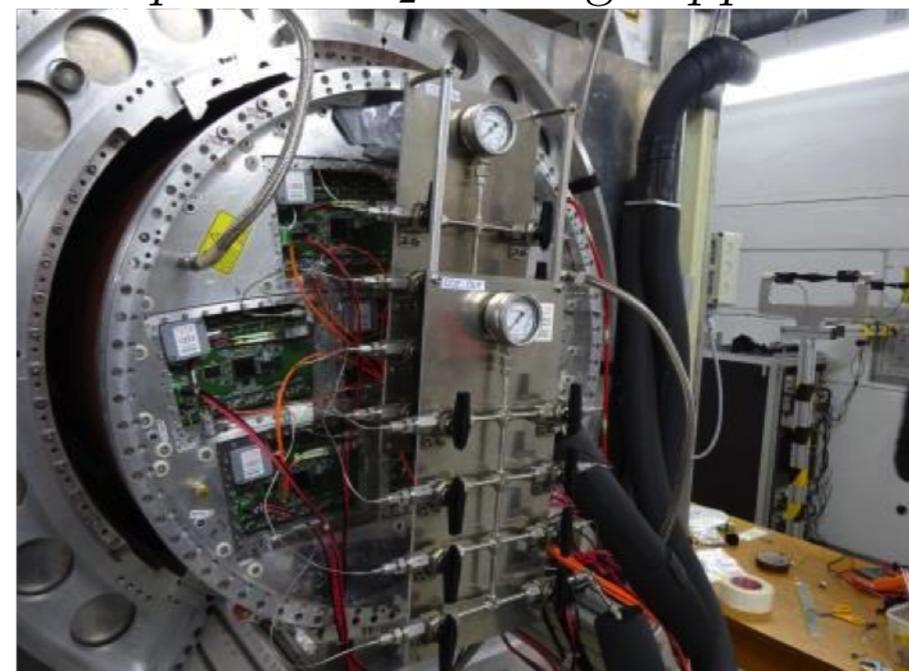


MicroMegas

Baseline module configuration for TB2015



2-phase CO₂ cooling support



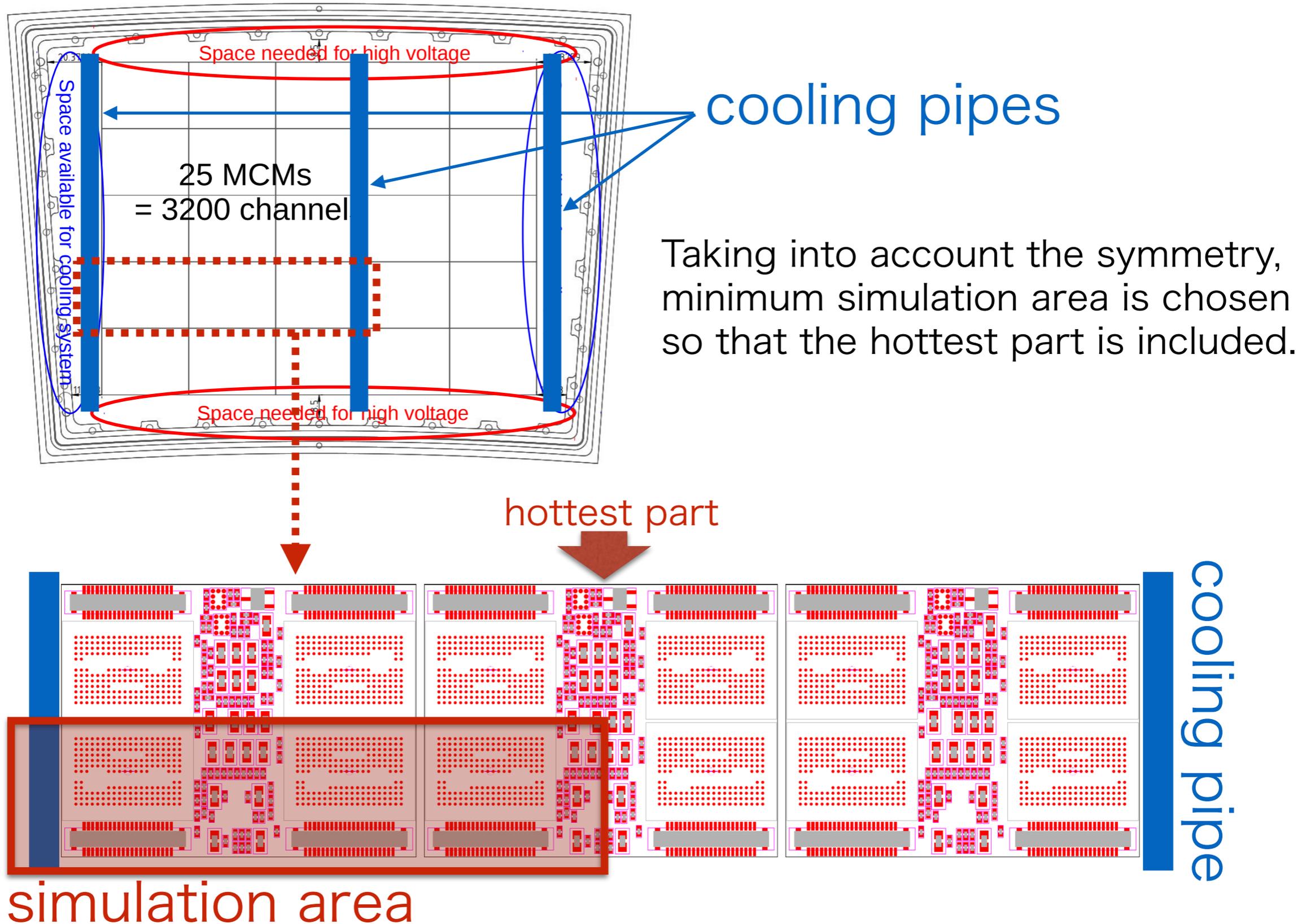
Summary

- For the next module development,
 - Readout electronics are being developed by Lund group.
 - Module design, which includes cooling channels, mechanical objects, are the next step.
 - For this, we started heat mockup tests.
- For the final electronics (advanced endplate),
 - Just a quick test with heat mockup was done.
 - Chip specifications are to be defined.
 - Cooling channel studies are necessary.

Backup Slides

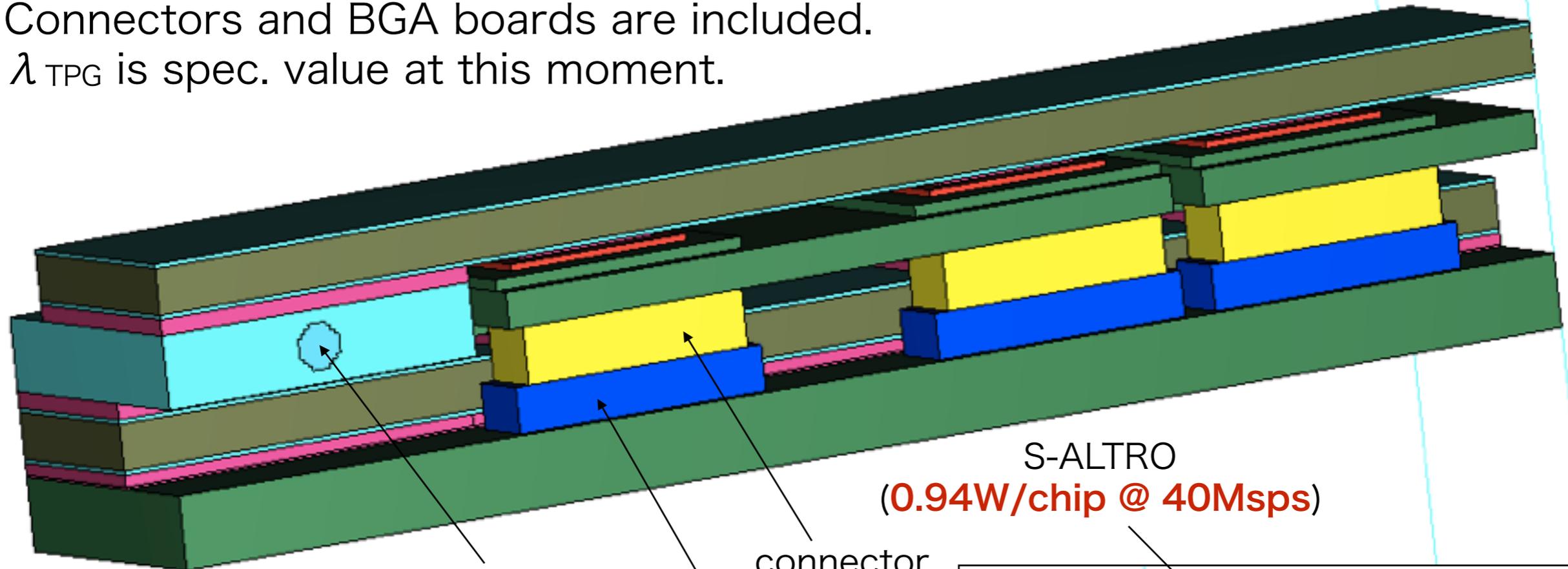
3D Thermal Modeling of the Readout Module

Two cooling pipes at the module sides and one near the middle.



3D Thermal Modeling of the Readout Module

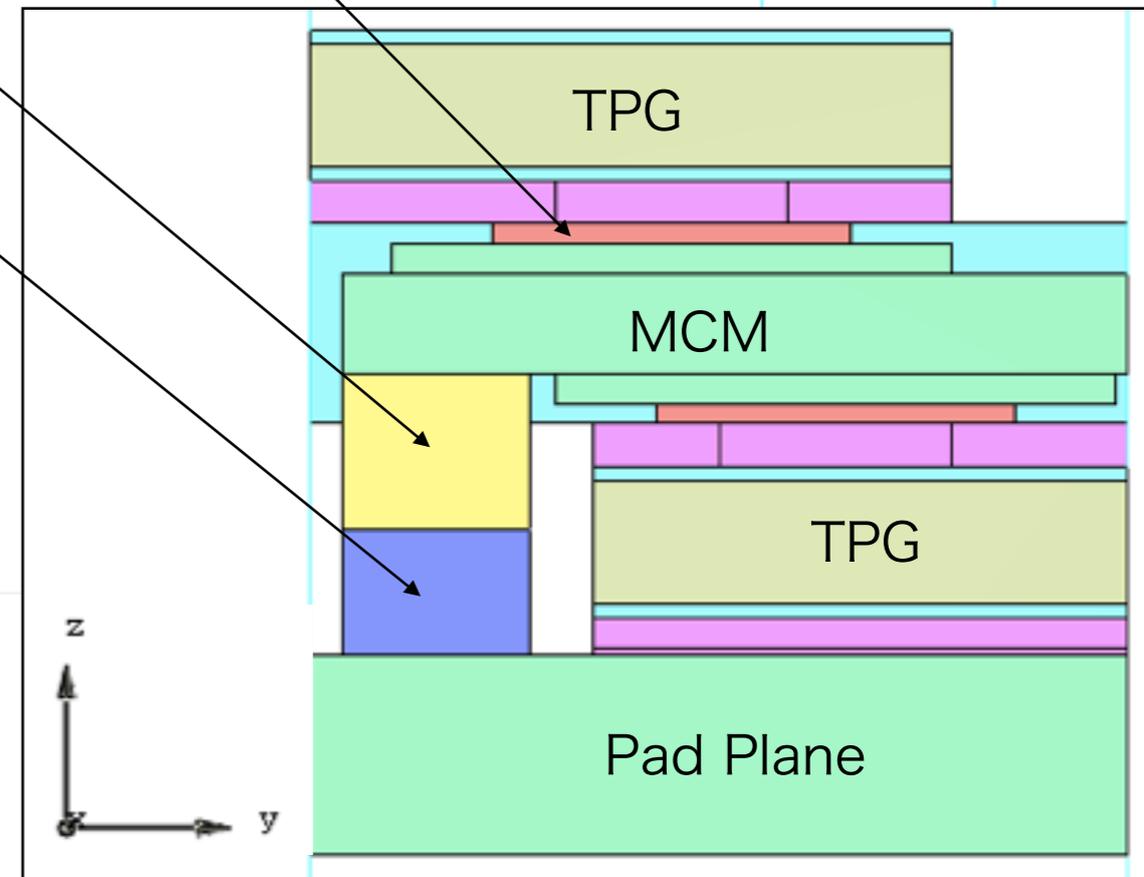
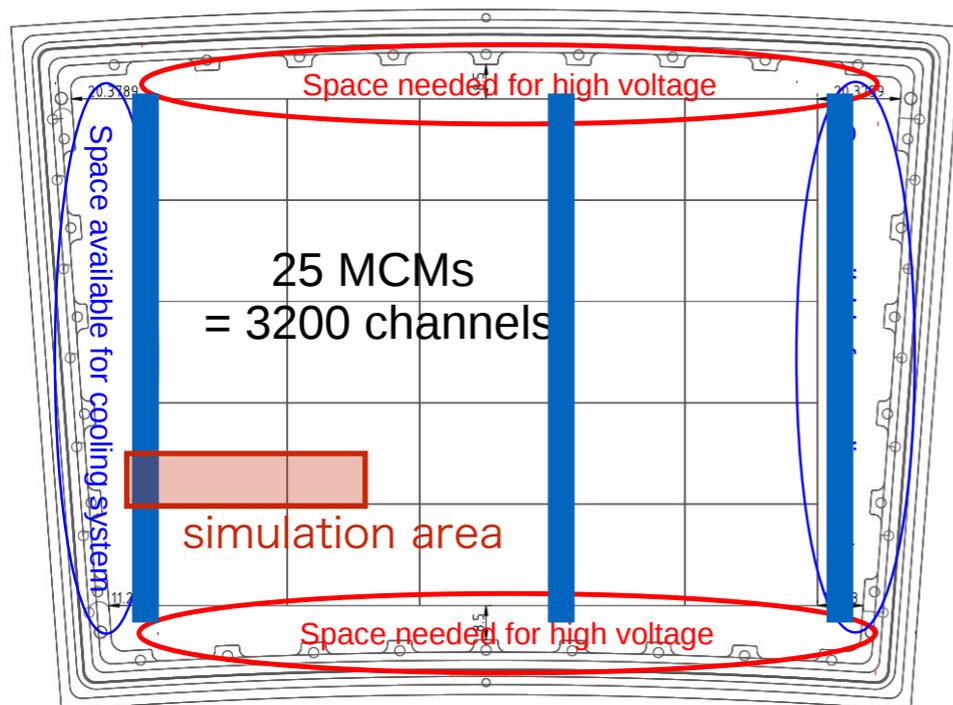
More precise modeling than before.
Connectors and BGA boards are included.
 λ_{TPG} is spec. value at this moment.



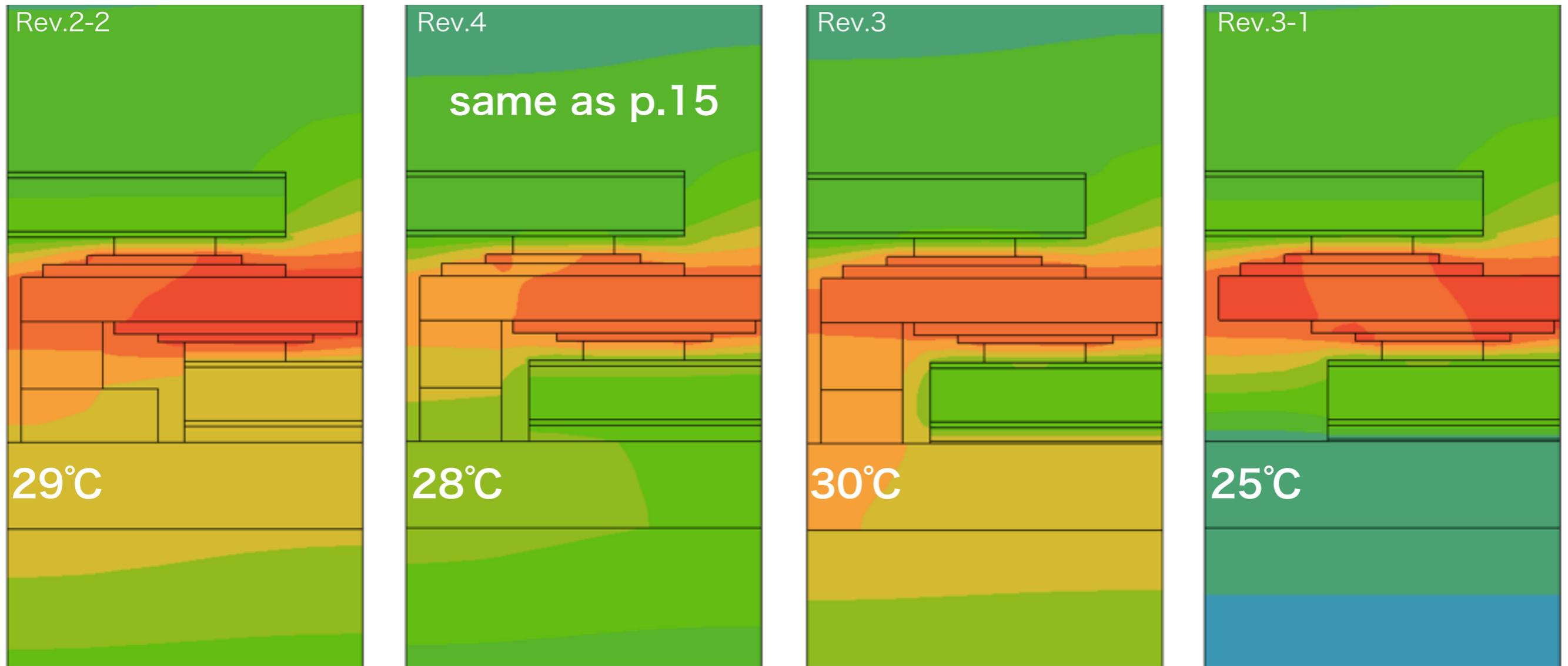
cooling pipe
(fixed to 20°C)

BGA board
connector

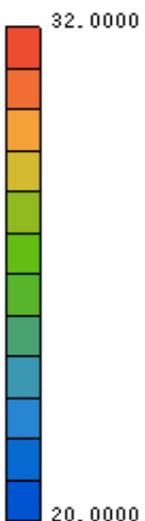
S-ALTRO
(0.94W/chip @ 40Msps)



Comparison btw. different cases



温度



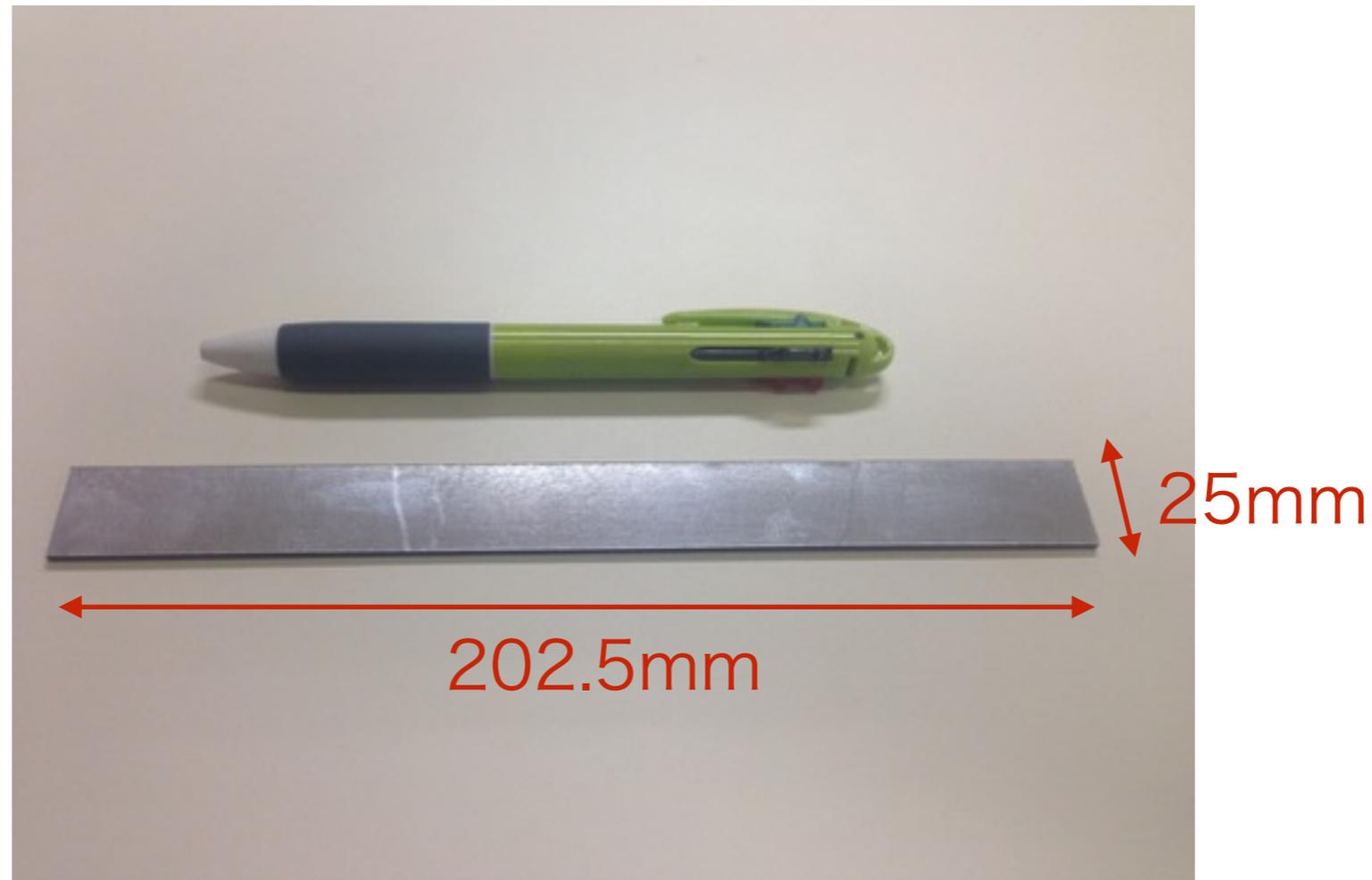
Wider BGA board,
hence narrower TPG

Insulator to block heat
from TPG to pad plane.
This doesn't work at all
because of heat flow
through the connector.

Remove the connector
to show that the
insulator works well
only when thermal
contact btw. MCM and
pad plane is small.

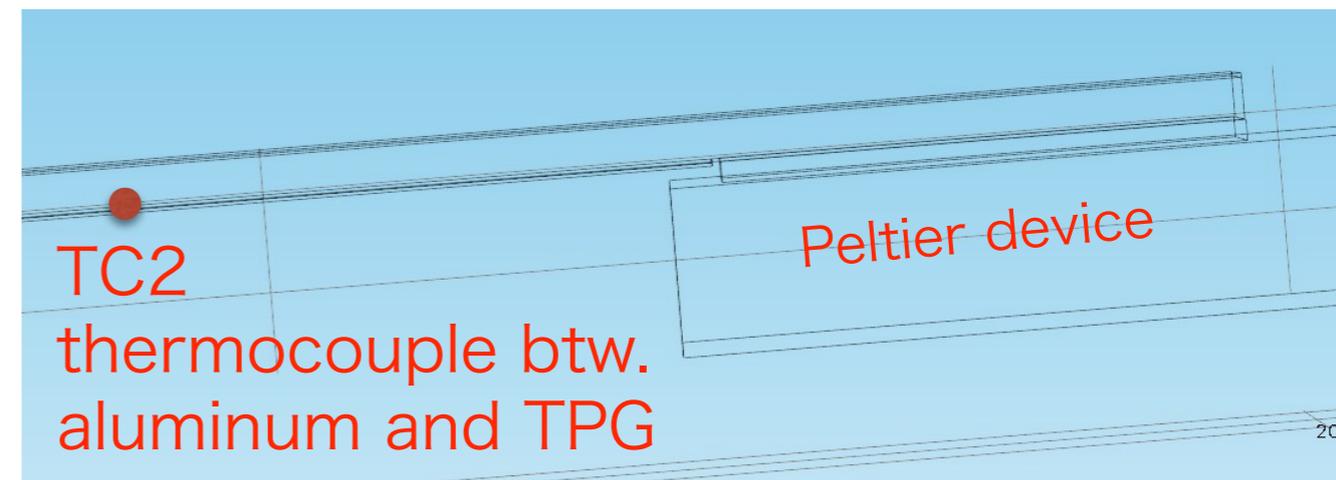
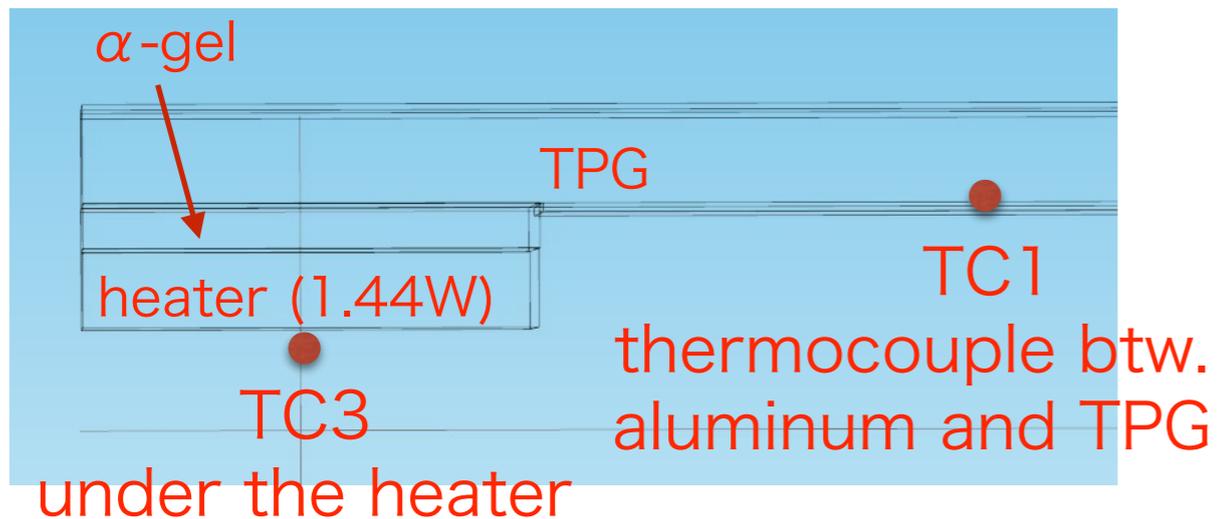
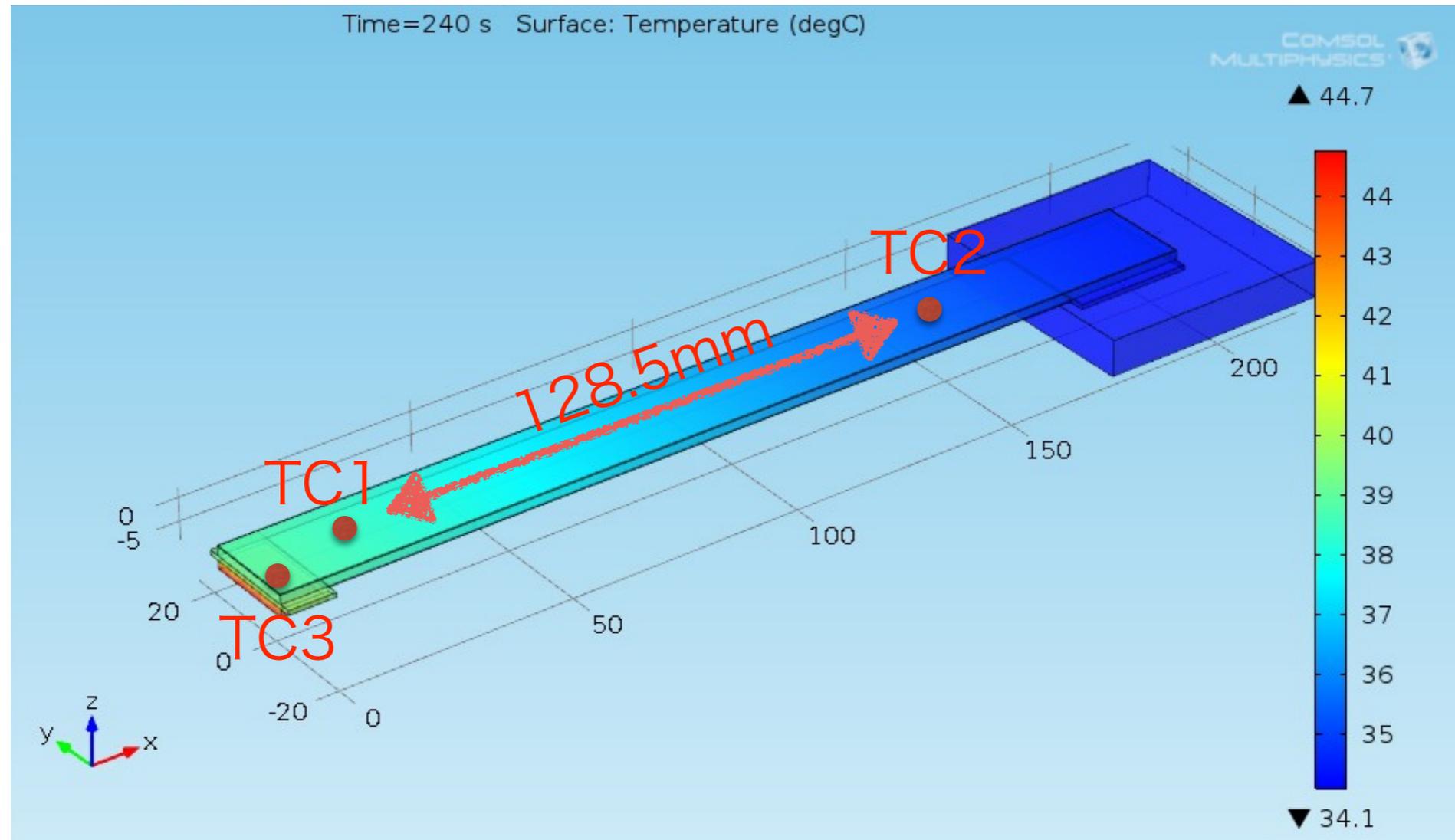
Evaluation of Heat Conductive Plate, TPG

TPG (Thermal pyrolytic graphite) — high heat conductive plate by **MOMENTIVE™**
 $\lambda \sim 1500 \text{ W}/(\text{m} \cdot \text{K})$ in plane and $20 \text{ W}/(\text{m} \cdot \text{K})$ vertically

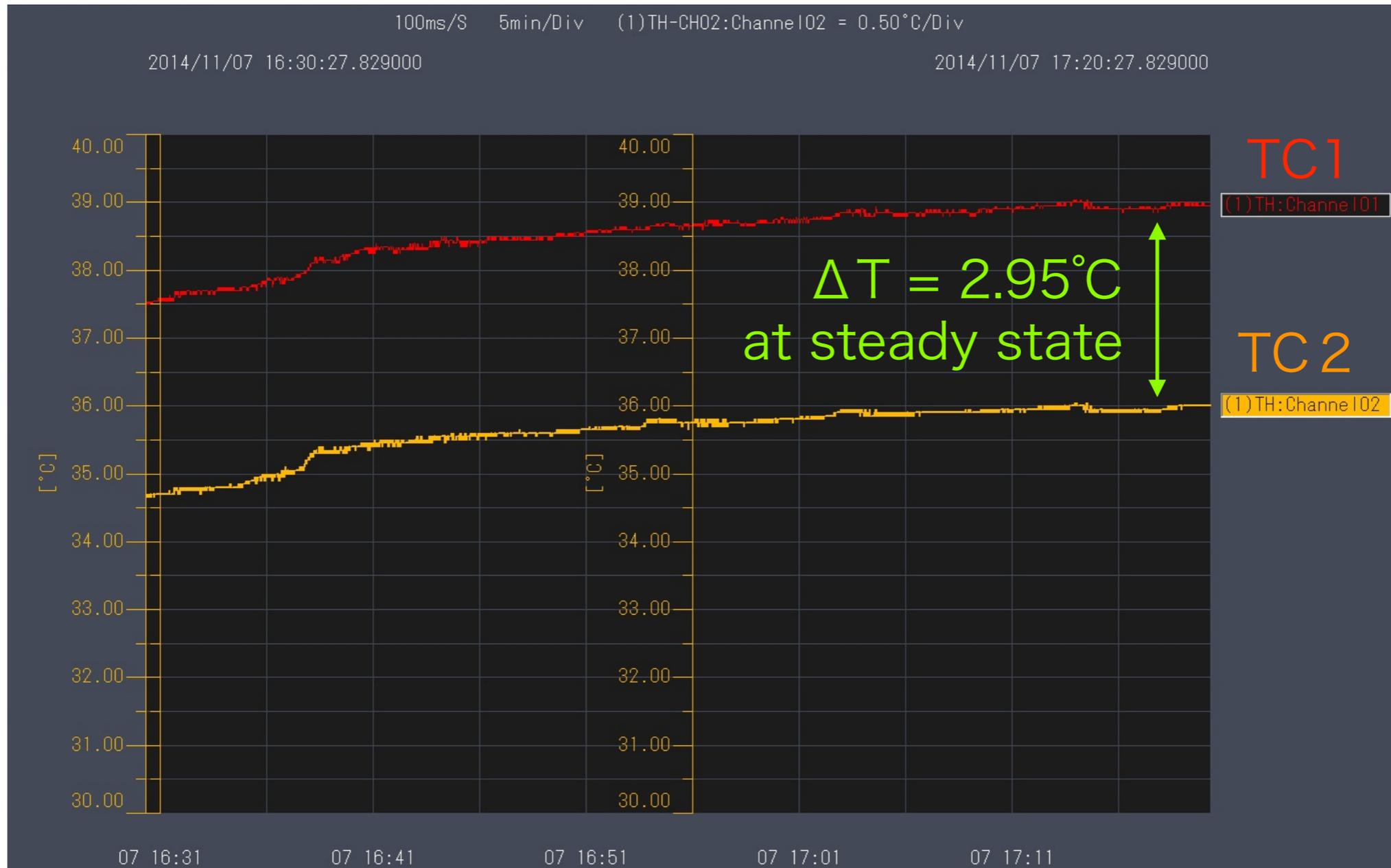


TPG Measurement Setup

A ceramic heater as a heat source, a Peltier device as a heat sink.

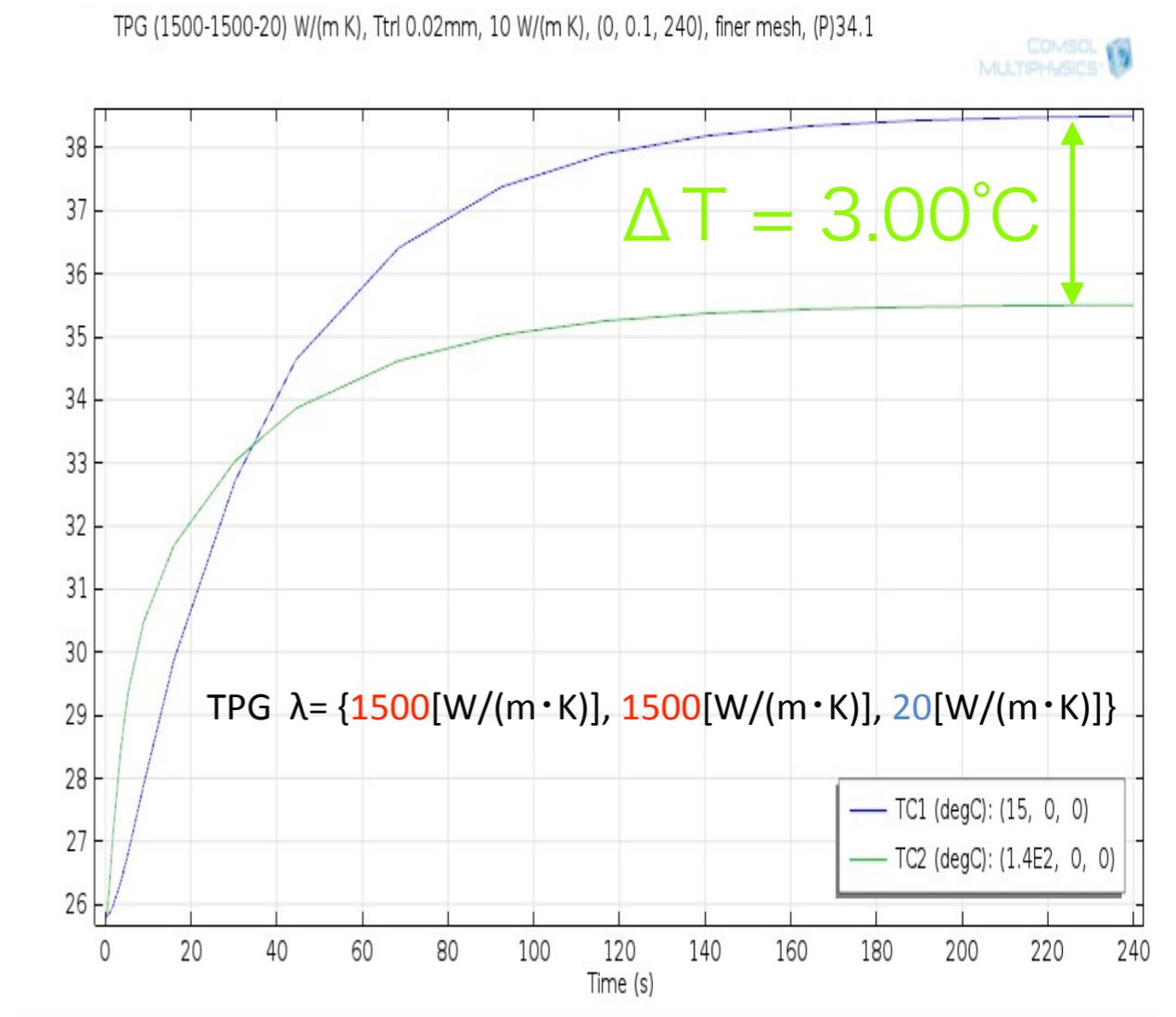
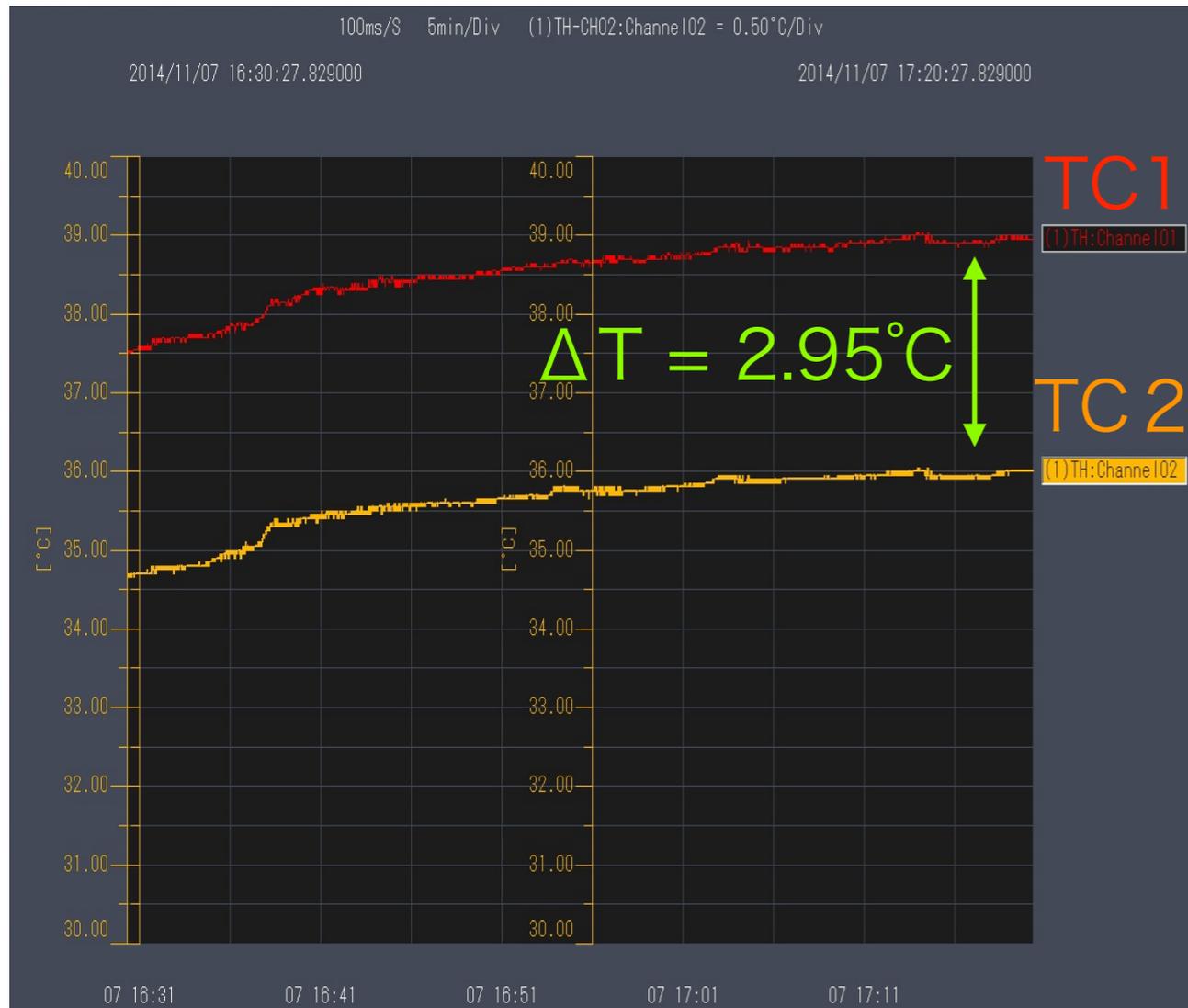


TPG Measurement Results

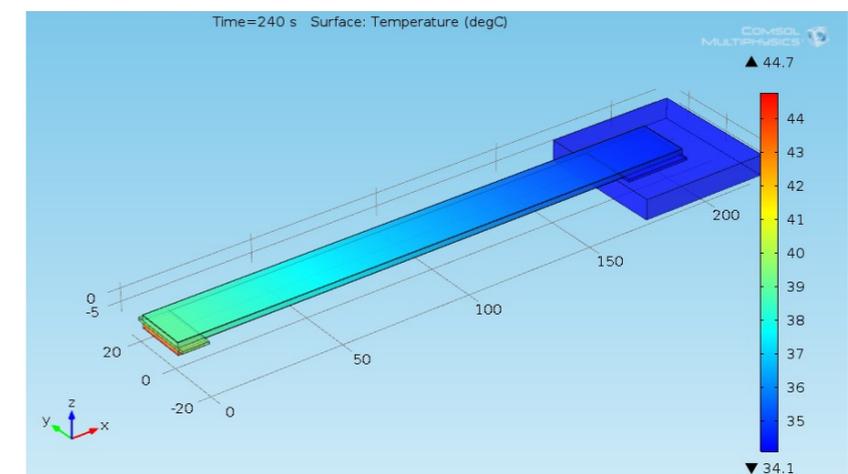


The steady state measurement gives thermal conductivity $\lambda = 1526\text{W}/(\text{m} \cdot \text{K})$, after subtracting the effect of aluminum laminate. The result is well consistent with the specification.

Comparison with Simulation

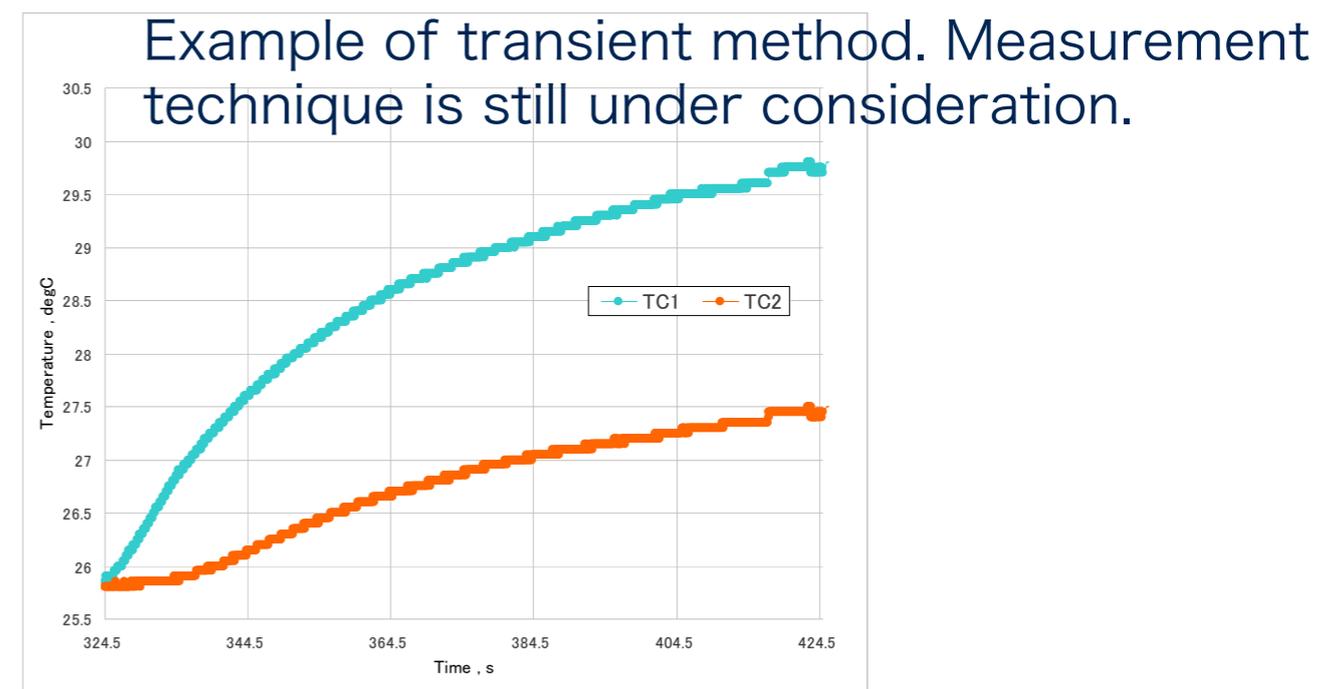
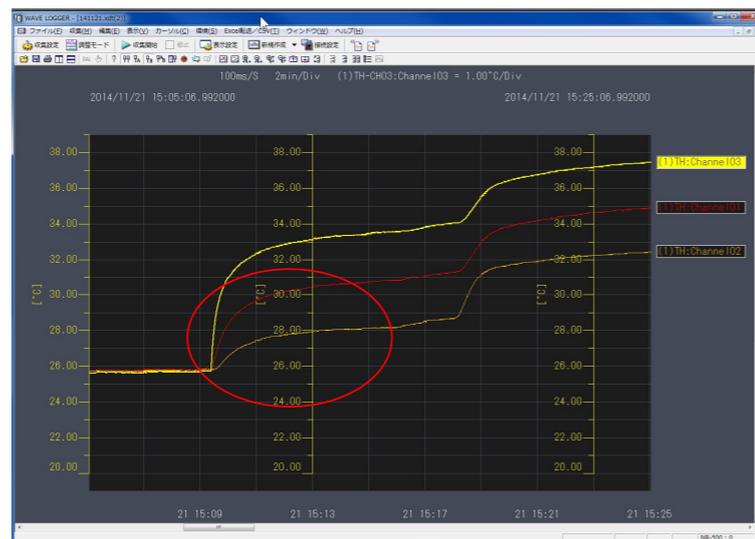


- Well explained by the simulation.



TPG Evaluation Summary and Plan

- Thermal conductivity of TPG was measured with the steady state method. The value can be an input to the module simulation.
- Heat conductivity through the Al, glue and TPG is also important but not given by the specification sheet. It will be measured next.
- Instead of the steady state method, the transient method is also being tried, which is faster to obtain measurement results. This will be valuable to evaluate various alternative materials.



What we know from the module simulation

- For the proposed design, temperature gradient will be about 8°C in the case of 40Msps operation w/o power pulsing.
- If the operation is at 20Msps, $P(\text{chip})$ is 0.67W and the temperature gradient will be $\sim 6^{\circ}\text{C}$.
- Heat flow through the connector is not small. Because of this, pad plane temperature is near the chip temperature. Therefore, the chip at the “operational” temperature is not enough and should be relatively near to the room temperature.
- Via of the BGA board should be as thin as possible. Thermal contact between TPG and chips and the one between TPG and pad plane should be better.
- (mockup test will be performed)

Discussions on final ILC-TPC electronics

- Electronics meeting was held at Bonn on 18/Sep/2014.
Materials can be obtained at
<https://agenda.linearcollider.org/event/6507/>
- Exchanged information with ASIC experts.
- Options:
ASIC process — keep IBM 130nm? move to TSMC 65nm?
Digital filtering rather than analog shaping for baseline correction?
Common Front End (CFE) project for analog part?
Stack two or more different chips?
- Need to determine parameters by the physics aspects
—> temporary values are listed in the next slide.
—> These numbers have to be verified.